IS37SML01G1
IS38SML01G1

1Gb SLC-1b ECC
3.3V SERIAL NAND FLASH MEMORY WITH 104MHZ MULTI I/O SPI INTERFACE

DATA SHEET

1Gb 3.3V SPI-NAND FLASH MEMORY WITH 104MHZ MULTI I/O SPI INTERFACE with 1b ECC

FEATURES

- **Flexible & Efficient Memory Architecture**
  - Organization:
    - Memory Cell Array: (128M + 4M) x 8bit
    - Data Register: (2K + 64) x 8bit
    - Page Size: (2K + 64) Byte
    - Block Erase: (128K + 4K) Byte
    - Memory Cell: 1bit/Memory Cell

- **Highest performance**
  - Frequency : 104MHz
  - Internal ECC Implementation: 1-bit ECC
  - Read Performance
    - Read from Cell to Register with Internal ECC: 100us
  - Write Performance
    - Program time: 400us - typical
    - Block Erase time: 4ms – typical

- **Low Power with Wide Temp. Ranges**
  - Single 3.3V (2.7V to 3.6V) Voltage Supply
  - 10 mA Active Read Current
  - 8 µA Standby Current
  - Temp Grades:
    - Industrial: -40°C to +85°C
    - Extended: -40°C to +105°C
    - Automotive, A1: -40°C to +85°C
    - Automotive, A2: -40°C to +105°C

- **Reliable CMOS Floating Gate Technology**
  - Internal ECC Requirement: **1bit/512Byte**
  - Endurance: 100K Program/Erase cycles
  - Data Retention: 10 years

- **Efficient Read and Program modes**
  - Support SPI-Mode 0 and SPI-Mode 3
  - Bus Width: x1, x2[1], x4
  - Command Register Operation
  - NOP: 4 cycles
  - OTP Operation
  - Bad-Block-Protect
  - Boot Read

- **Advanced Security Protection**
  - Hardware Data Protection
    - Program/Erase Lockout during Power Transitions

- **Industry Standard Pin-out & Packages**
  - M =16-pin SOIC 300mil
  - L = 8-contact WSON 8x6mm

Note:

1. **X2 Program Operation is not defined.**

GENERAL DESCRIPTION

The serial electrical interface follows the industry-standard serial peripheral interface (SPI), providing a cost-effective non- volatile memory storage solution in systems where pin count must be kept to a minimum.
The ISSI IS37/38SML01G1 is a 1Gb SLC SPI-NAND Flash memory device based on the standard parallel NAND Flash, but new command protocols and registers are defined for SPI operation. It is also an alternative to SPI-NOR, offering superior write performance and cost per bit over SPI-NOR.

The command set resembles common SPI-NOR command set, modified to handle NAND-specific functions and new features. New features include user-selectable internal ECC. With internal ECC enabled, ECC code is generated internally when a page is written to memory array. The ECC code is stored in the spare area of each page. When a page is read to the cache register, the ECC code is calculated again and compared with the stored value. Errors are corrected if necessary. The device either outputs corrected data or returns an ECC error status.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. The device contains 1024 blocks, composed by 64 pages consisting in two NAND structure of 32 series connected Flash cells. Each page consists 2112-Byte and is further divided into a 2048-Byte data storage area with a separate 64-Byte spare area. The 64-Byte area is typically used for memory and error management.

The copy back function allows the optimization of defective blocks management: when a page program operation fails, the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase.

The pins serve as the ports for signals. The device has six signal lines plus Vcc and ground (GND, Vss). The signal lines are SCK (serial clock), SI (command and data input), SO (response and data output), and control signals CS#, HOLD#, WP#.

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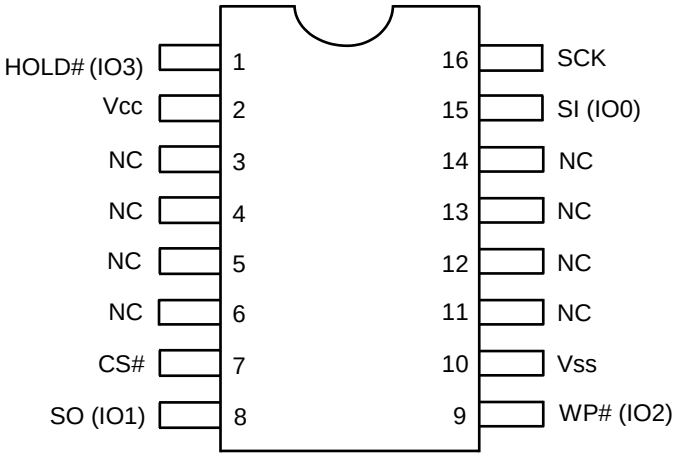
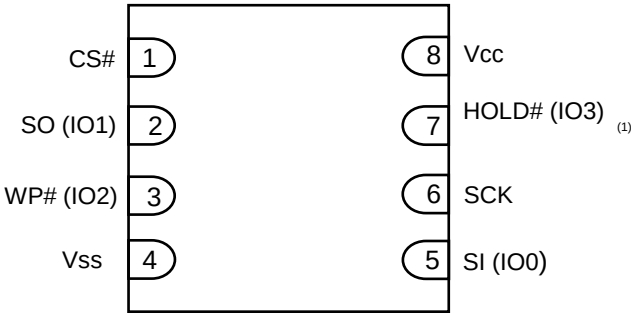
1. PIN CONFIGURATION



16-pin SOIC 300mil



8-contact WSON 8x6mm

2. PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CS#	INPUT	**Chip Select:** The device is activated/deactivated as CS# is driven LOW (1) /HIGH (2). After power-on, the device requires a falling edge on CS# before any command can be written. The device goes to standby mode when no PROGRAM, ERASE, or WRITE STATUS REGISTER operation is in progress.
HOLD# / IO3	INPUT/ OUTPUT	**HOLD#/IO3:** Hold pauses any serial communication with the device without deselecting it.(3) When driven LOW, SO is at high impedance (Hi-Z), and all inputs in SI and SCK are ignored; CS# also should be driven LOW. HOLD# must not be driven during x4 operation.
WP# / IO2	INPUT/ OUTPUT	**Write Protect#/IO2:** WP# is driven LOW to prevent overwriting the block-lock bits (BP0,BP1 and BP2). If block register write disable (BRWD) bit is set. (4) WP# must not be driven during x4 operation.
SCK	INPUT	**Serial Clock:** SCK provides serial interfacing timing. Address, commands, and data in SI are latched on the rising edge of SCK. Output (data out SO) is triggered after the falling edge of SCK. The clock is valid only when the device is active. (5)
SI / IO_0	INPUT/OUTPUT	**Serial Data Input/IO0:** SI transfers data serially into the device. Device latches addresses, commands, and program data in SI on the rising-edge of SCK. SI must not be driven during x2 or x4 READ operation.
SO / IO_1	INPUT/OUTPUT	**Serial Data Output/IO1:** SO transfers data serially out of the device on the falling edge of SCK.. K. SO must not be driven during x2 or x4 PROGRAM operation.
Vcc(6)	POWER	Vcc is the power supply for device.
Vss(6)	GROUND	Ground
NC	Unused	No Connection Not internally connected.

Notes:

1. **CS# places the device in active power mode.**
2. **CS# deselects the device and places SO at high impedance.**
3. **It means HOLD# input doesn't terminate any READ, PROGRAM, or ERASE operation currently in progress.**
4. **If the BRWD bit is set to 1 and WP# is LOW, the block protect bits can't be altered.**
5. **SI and SO can be triggered only when the clock is valid.**
6. **Connect all Vcc and Vss pins of each device to common power supply outputs. Do not leave Vcc or Vss disconnected.**

3. BLOCK DIAGRAM

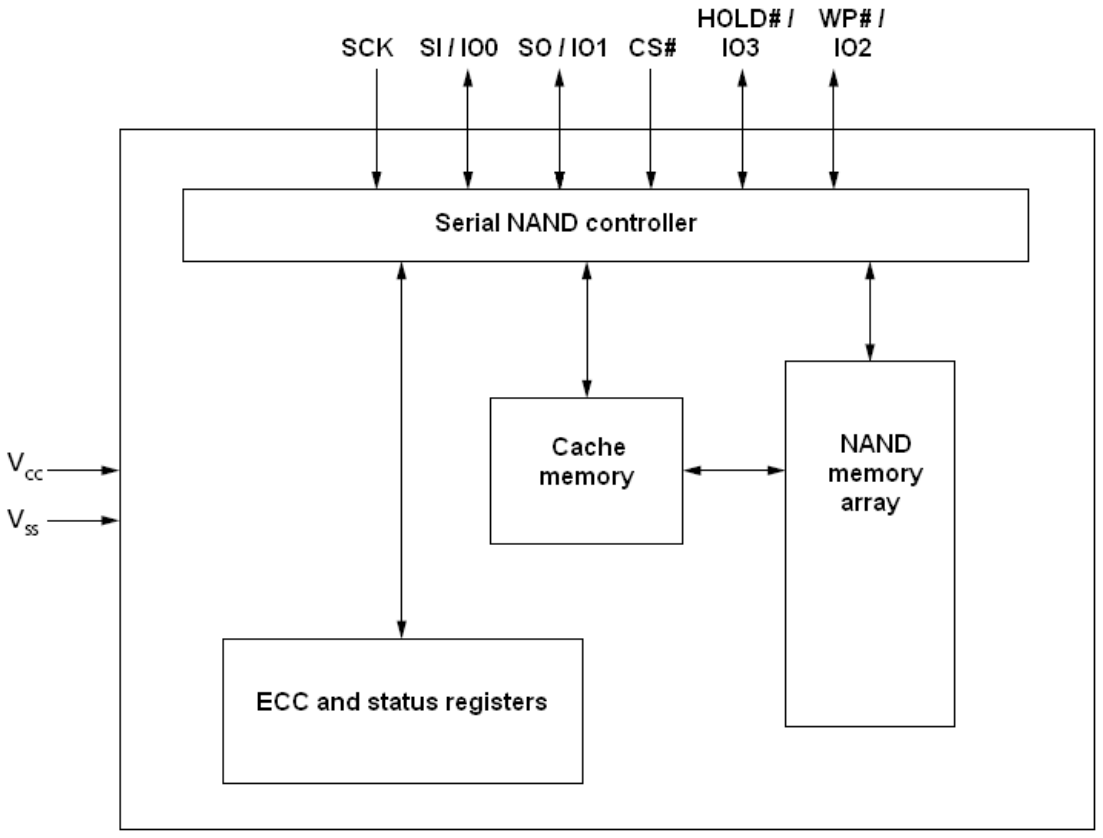


Figure 3.1 Functional Block Diagram

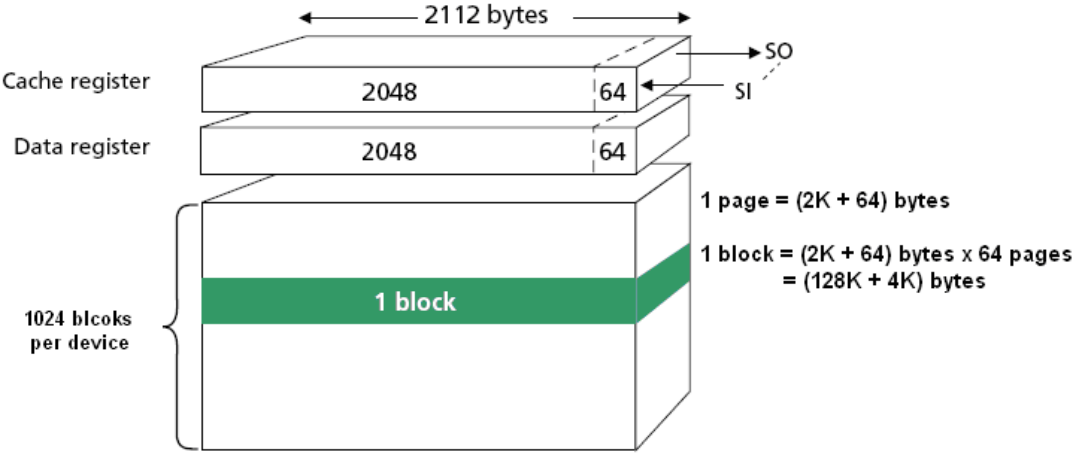


Figure 3.2 Array Organization

4. Command Set

Table 4.1 Command Set

Command	Op Code	Address Bytes	Dummy Bytes	Data Bytes
Block Erase	D8h	3	0	0
Get Feature(1)	0Fh	1	0	1
Set Feature	1Fh	1	0	1
Write Disable	04h	0	0	0
Write Enable	06h	0	0	0
Program Load	02h	2	0	1 to 2112
Program Load x4(2)	32h	2	0	1 to 2112
Program Load Random Data	84h	2	0	1 to 2112
Program Load Random Data x4(2)	34h	2	0	1 to 2112
Program Execute	10h	3	0	0
Page Read	13h	3	0	0
Read from Cache	03h, 0Bh	2	1	1 to 2112
Read from Cache x2	3Bh	2	1	1 to 2112
Read from Cache x4(2)	6Bh	2	1	1 to 2112
Read ID	9Fh	0	1	5
RESET	FFh	0	0	0

Notes:

1. **Refer to Feature Register.**
2. **Command/Address is 1-bit input per clock period, data is 4-bit input/output per clock period.**

5. ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS (1)

Storage Temperature		-65°C to +150°C
Surface Mount Lead Soldering Temperature	Standard Package	240°C 3 Seconds
	Lead-free Package	260°C 3 Seconds
Input Voltage with Respect to Ground on All Pins		-0.6V to +4.6V
All I/O Voltage with Respect to Ground		-0.6V to V_{CC} + 0.3V(< 4.6V)
V_{CC}		-0.6V to +4.6V
Short Circuit Current		5mA
Electrostatic Discharge Voltage (Human Body Model)(2)		-2000V to +2000V

Notes:

1. **Applied conditions greater than those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**
2. **ANSI/ESDA/JEDEC JS-001**

5.2 RECOMMENDED OPERATING CONDITIONS

Part Number	IS37/38SML01G1
Operating Temperature (Industrial Grade)	-40°C to 85°C
Operating Temperature (Extended Grade)	-40°C to 105°C
Operating Temperature (Automotive Grade A1)	-40°C to 85°C
Operating Temperature (Automotive Grade A2)	-40°C to 105°C
V_{CC} Power Supply	2.7V (VMIN) – 3.6V (VMAX); 3.3V (Typ)

5.3 DC CHARACTERISTICS

(Under operating range)

Parameter		Symbol	Test Conditions	Min	Typ.	Max	Unit
Operating Current	Page Read with Serial Access	ICC1	fC=104MHz, CS#=VIL, IOUT=0mA	-	16	20	mA
	Program	ICC2	-	-	16		
	Erase	ICC3	-	-	16		
Stand-by Current (TTL)		ISB1	CS#=VIH, WP#=0V/Vcc	-	-	1	
Stand-by Current (CMOS)		ISB2	CS#=VCC-0.2, WP#=0V/Vcc	-	10	50	uA
Input Leakage Current		ILI	VIN=0 to Vcc (max)	-	-	+/-10	
Output Leakage Current		ILO	VOUT=0 to Vcc (max)	-	-	+/-10	
Input High Voltage		VIH (1)		0.7xVCC	-	Vcc+0.3	V
Input Low Voltage, All inputs		VIL (1)		-0.3	-	0.2xVCC	
Output High Voltage Level		VOH	IOH=-20 uA	0.7xVCC	-	-	
Output Low Voltage Level		VOL	IOL=1mA	-	-	0.15xVCC	

Notes:

1. VIL can undershoot to - 2V and VIH can overshoot to Vcc + 2V for durations of 20 ns or less.
2. Typical value are measured at Vcc=3.3V, TA=25℃. Not 100% tested.

5.4 VALID BLOCK

Description	Requirement
Minimum / Maximum number of Valid block number	1004 / 1024
Bad Block Mark	Non FFh
Mark Location	Column 2048 of page 0 and page 1

Notes:

1. The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment and is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/512Byte ECC.

5.5 AC MEASUREMENT CONDITION

Symbol	Parameter	Min	Max	Units
CL	Output Load	1 TTL GATE and CL = 15pF		pF
TR,TF	Input Rise and Fall Times	-	2.4	ns
VIN	Input Pulse Voltages	0.2Vcc to 0.8 V_{CC}		V

5.6 AC PIN CAPACITANCE (TA = 25°C, VCC=3.3V, 1MHZ)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	-	-	8	pF
$C_{I/O}$	Input /Output Capacitance	$V_{I/O}$ = 0V	-	-	8	pF

Note:
1. These parameters are characterized and not 100% tested.

5.7 READ/PROGRAM/ERASE PERFORMANCNE

(Industrial: T_A=-40 to 85℃, Automotive, A1: T_A=-40 to 85℃, Vcc=2.7V ~ 3.6V)

Parameter	Symbol	Min	Typ	Max	Unit
Average Program Time	tPROG	-	400	900	us
Number of Partial Program Cycles in the Same Page	NOP	-	-	4	cycle
Block Erase Time	tBERS	-	4	10	ms
Data Transfer from Cell to Register with Internal ECC	tRD	-	-	100	us

5.8 GENERAL TIMING CHARACTERISTICS

Parameter	Symbol	Min	Max
Clock frequency	f_C		104MHz
Hold# non-active hold time relative to SCK	t_{CD}	4.5ns	
Hold# hold time relative to SCK	t_{CH}	4.5ns	
Command deselect time	t_{CS}	100ns	
CS# setup time	t_{CSS}	5ns	
CS# hold time	t_{CSH}	5ns	
The last valid Clock low to CS# high	t_{CSCL}	5ns	
Output disable time	t_{DIS}		20ns
Hold# non-active setup time relative to SCK	t_{HC}	4.5ns	
Hold# setup time relative to SCK	t_{HD}	4.5ns	
Data input setup time	t_{SUDAT}	2ns	
Data input hold time	t_{HDDAT}	3ns	
Output hold time	t_{HO}	0ns	
Hold# to output Hi-Z	t_{HZ}		7ns
Hold# to output Low-Z	t_{LZ}		7ns
Clock low to output valid	t_V		8ns
Clock high time	t_{WH}	4.5ns	
Clock low time	t_{WL}	4.5ns	
Clock rise time (slew rate)	t_{CRT}	0.1V/ns	
Clock fall time (slew rate)	t_{CFT}	0.1V/ns	
WP# setup time	t_{WPS}	20ns	
WP# hold time	t_{WPH}	100ns	
Resetting time during Idle/Read/Program/Erase	t_{RST}		5/5/10/500us

Note:
1. For the first RESET condition after power up, tRST will be 1ms MAX.

6. Operations and Timing Diagrams

6.1 READ OPERATIONS AND SERIAL OUTPUT

The command sequence is as follows:

- 13h (PAGE READ to cache)
- 0Fh (GET FEATURE command to read the status)
- 0Bh or 03h (READ FROM CACHE x1)/ 3Bh (x2) / 6Bh (x4)

PAGE READ command requires 24-bit address with 8 dummy and a 16-bit row address. After row address is registered, the device starts the transfer from the main array to the cache register, and is busy for t_{RD} time. During this time, GET FEATURE command can be issued to monitor the status of the operation. Following a status of successful completion, READ FROM CACHE command must be issued to read the data out of the cache.

READ FROM CACHE command requires 16-bit address with 4 dummy bits and 12-bit column address for the starting byte. The starting byte can be 0 to 2111, but after the end of the cache register is reached, the data does not wrap around and SO goes to a Hi-Z state.

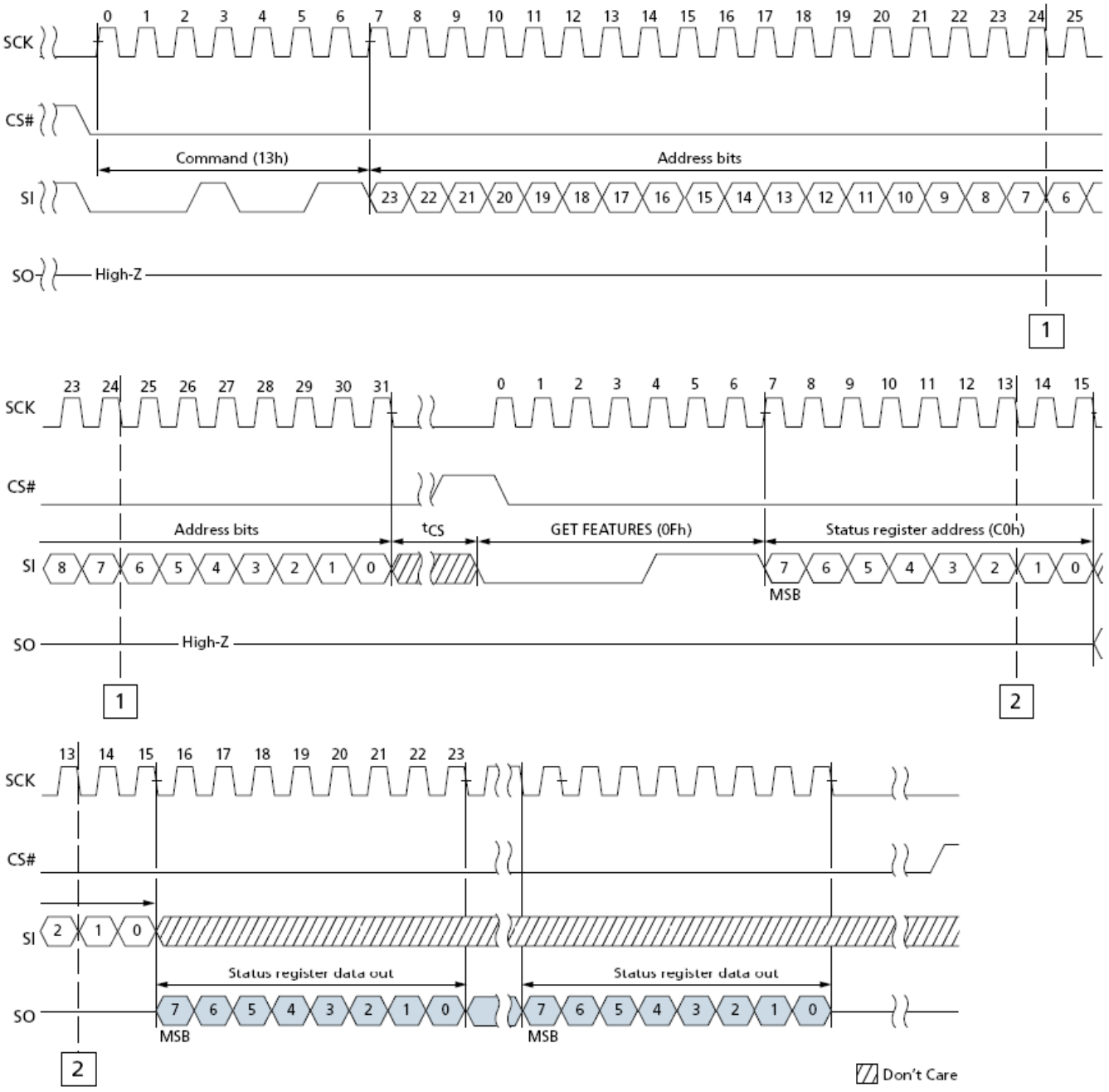


Figure 6.1 PAGE READ (13h) Timing

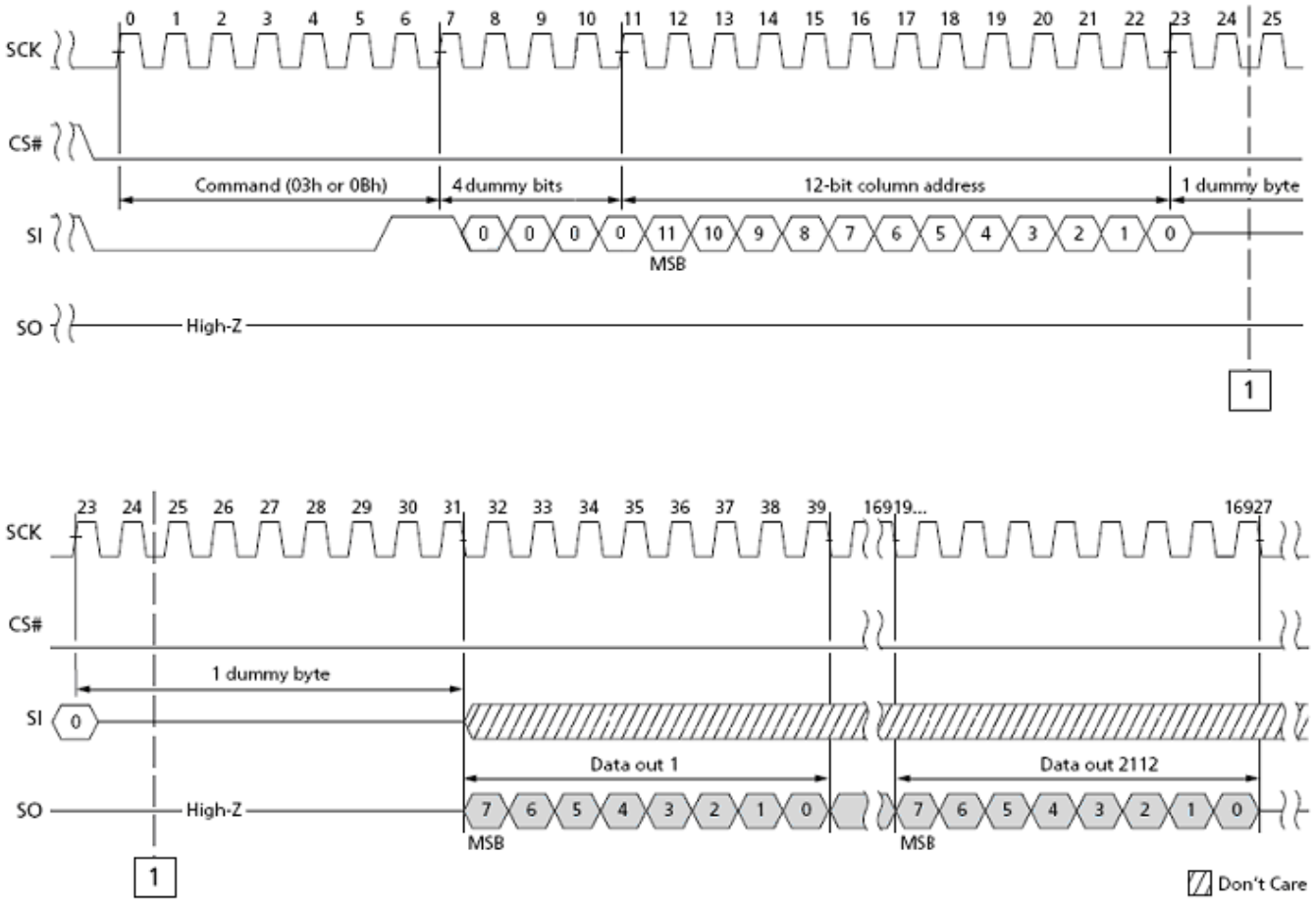


Figure 6.2 READ FROM CACHE (03h or 0Bh) Timing

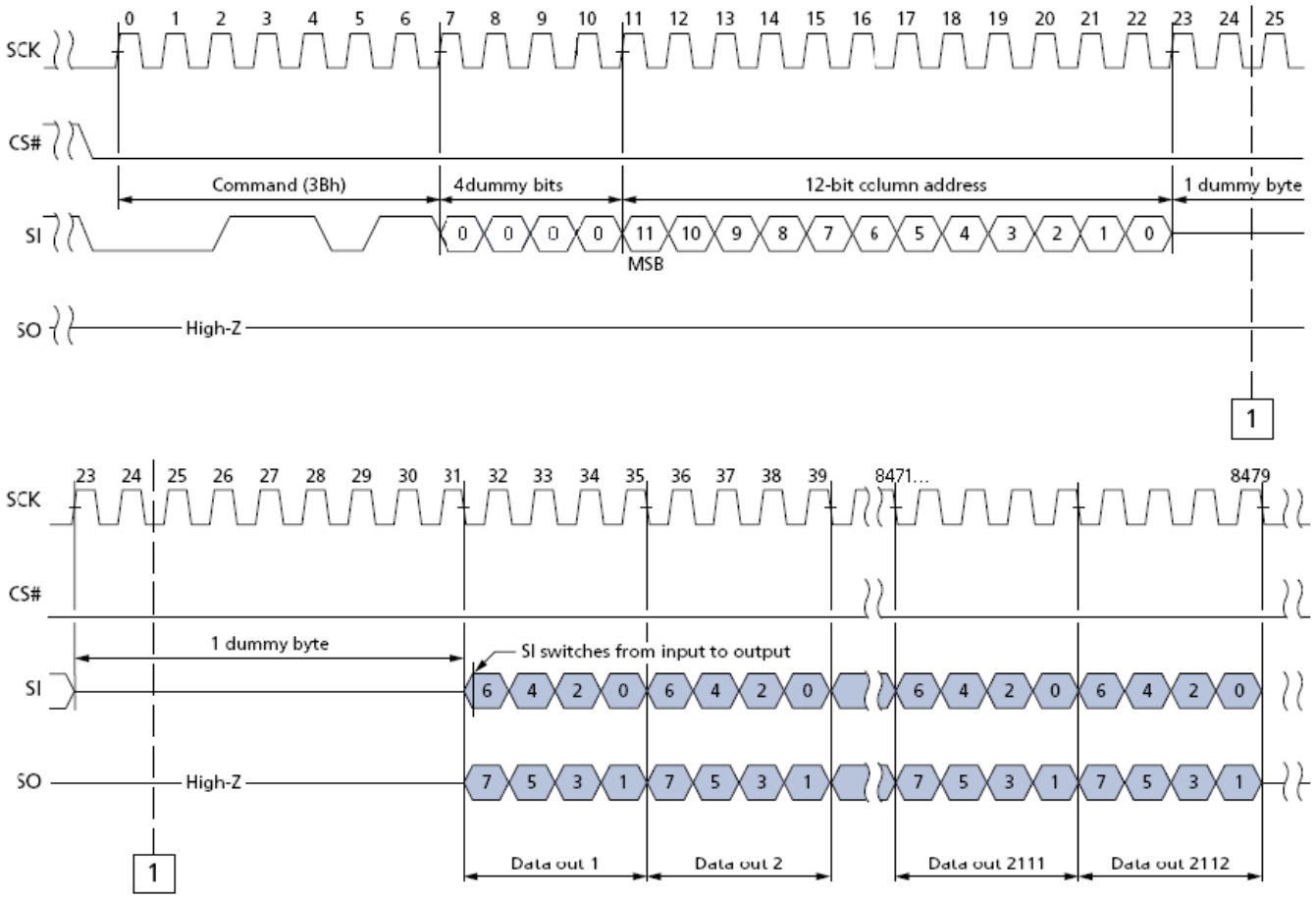


Figure 6.3 READ FROM CACHE x2 (3Bh) Timing

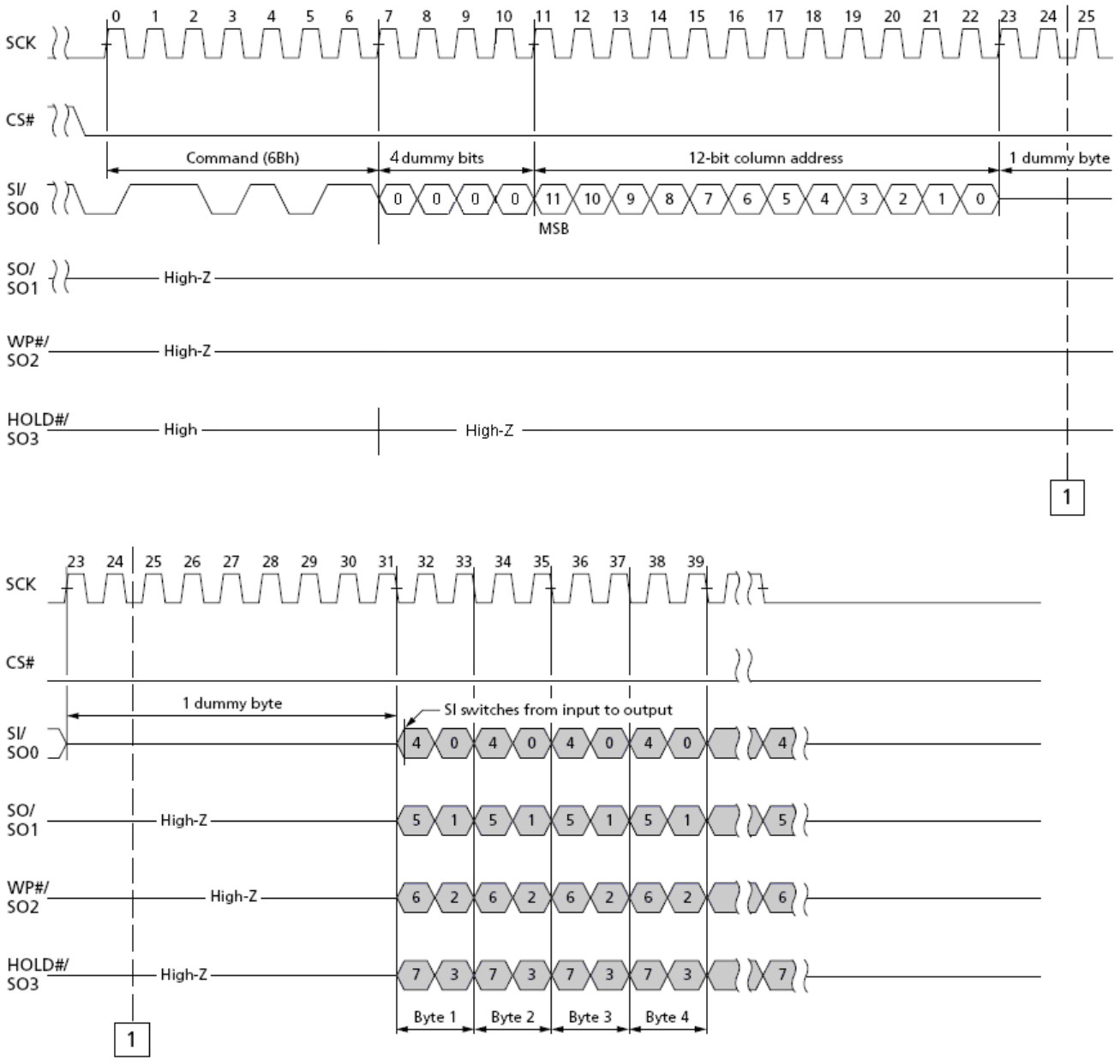


Figure 6.4 READ FROM CACHE x4 (6Bh) Timing

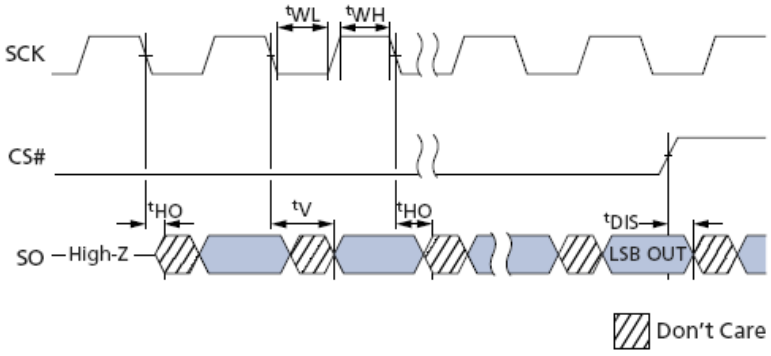


Figure 6.5 SERIAL OUTPUT Timing

6.2 PROGRAM OPERATIONS AND SERIAL INPUT

6.2.1 Page Program

The command sequence is as follows:

- 06h (WRITE ENABLE)
- 02h (PROGRAM LOAD x1) / 32h (x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

The page program operation sequence programs 1 byte to 2112 bytes of data within a page. WRITE ENABLE command is not issued (WEL bit is not set), then the rest of the program sequence is ignored. PROGRAM LOAD command requires 16-bit address with 4 dummy and a 12-bit column address, then the data bytes to be loaded into cache register. Only four partial page programs are allowed on a single page. If more than 2112 bytes are loaded, then those additional bytes are ignored by the cache register.

After the data is loaded, PROGRAM EXECUTE command must be issued to transfer the data from cache register to main array, and is busy for t_{PROG} time. PROGRAM EXECUTE command requires 24-bit address with 8 dummy bits and a 16-bit row address.

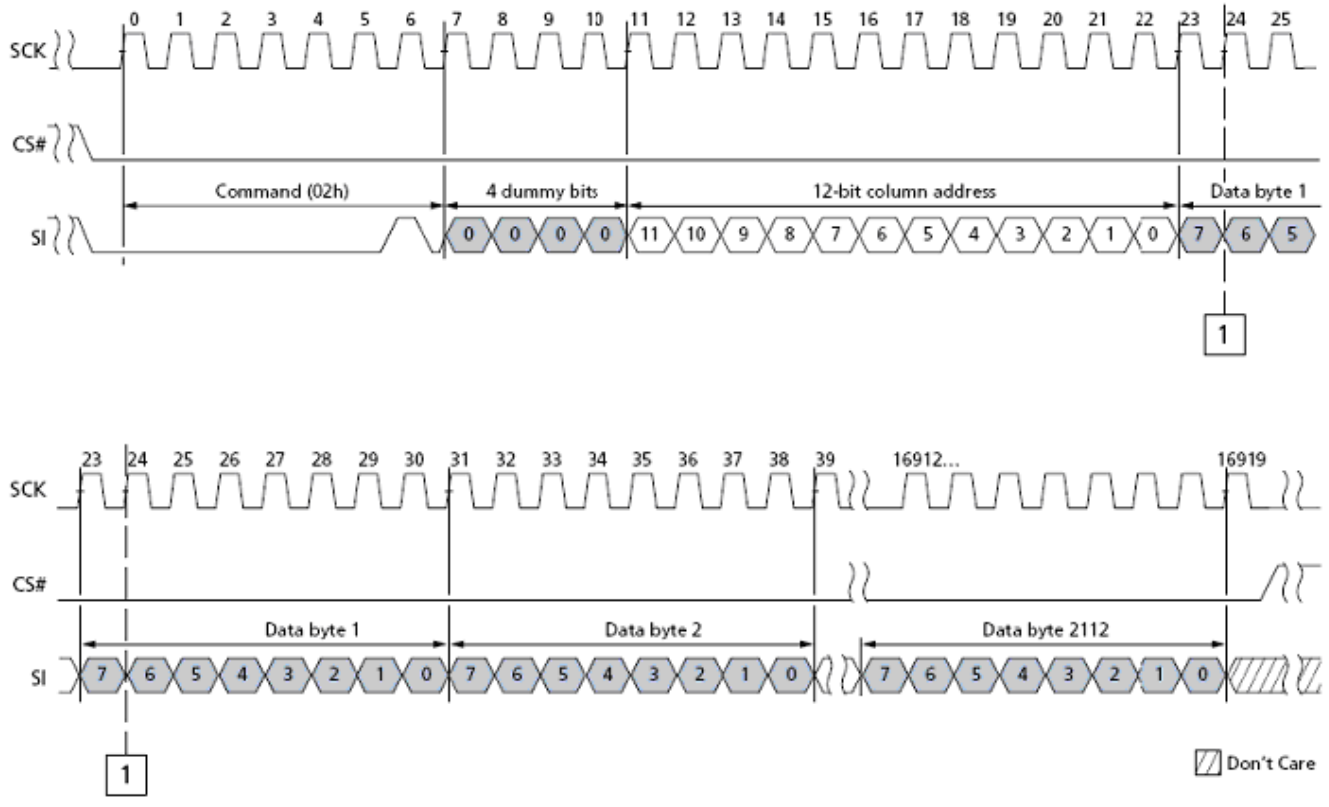


Figure 6.6 PROGRAM LOAD (02h) Timing

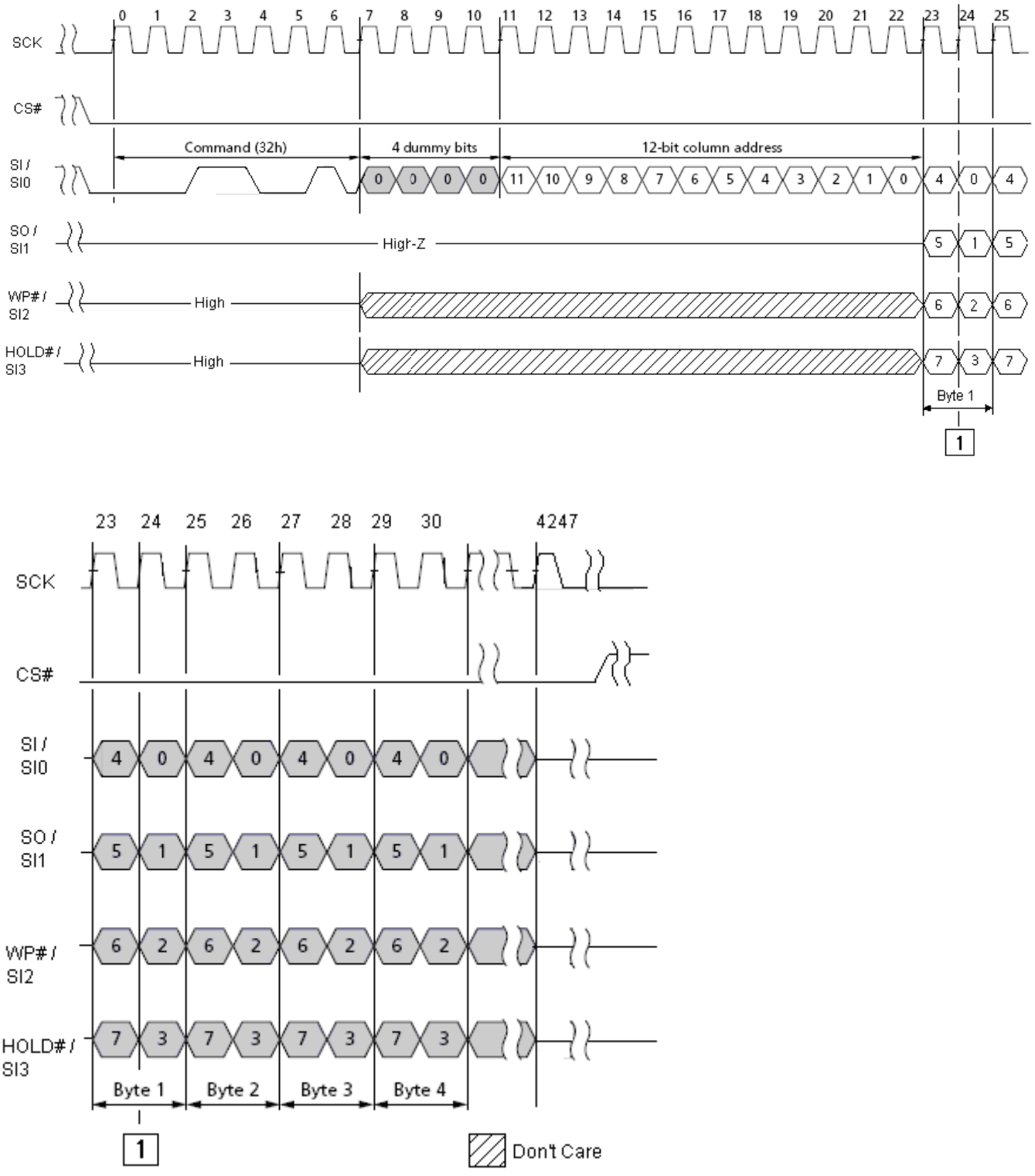
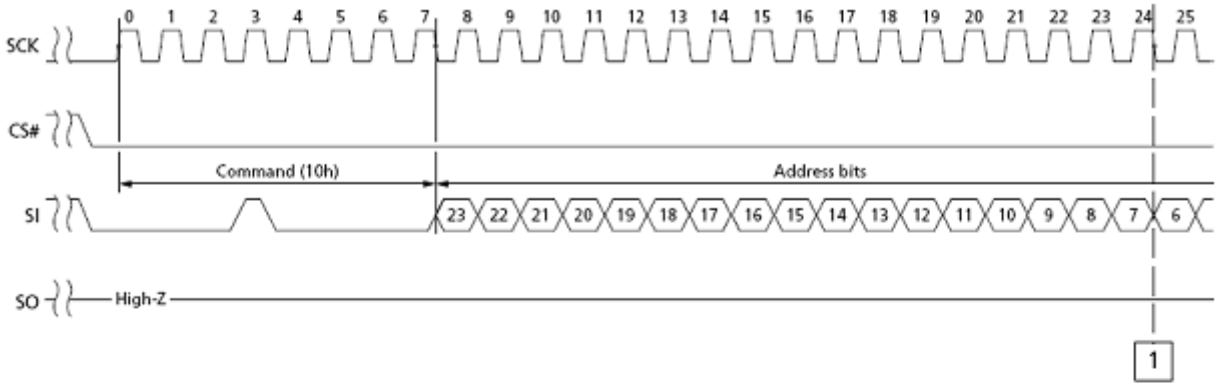
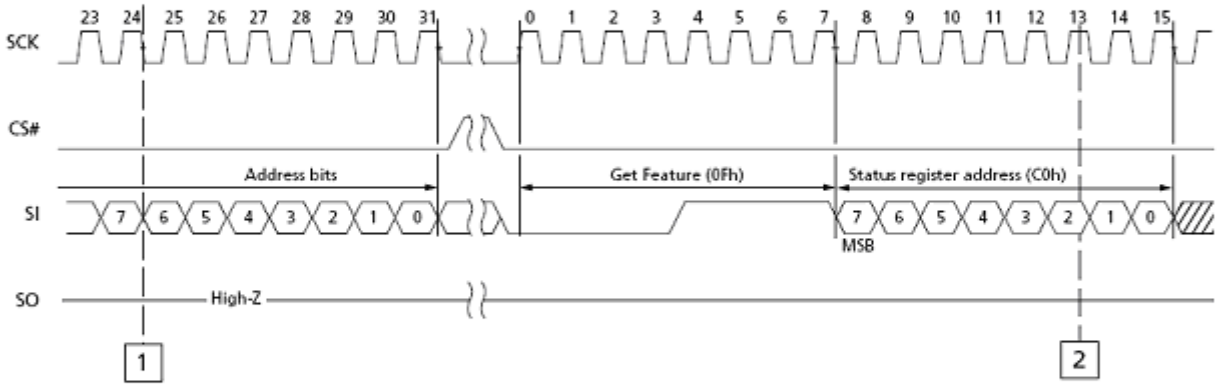
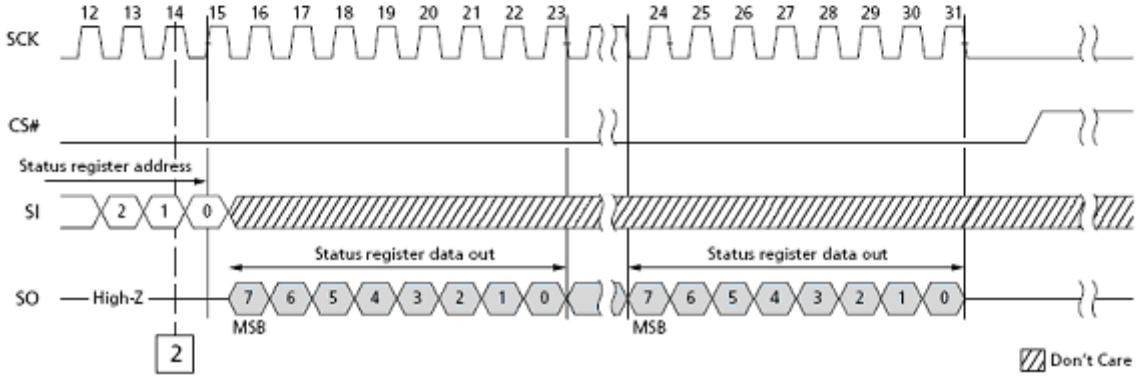


Figure 6.7 PROGRAM LOAD x4 (32h) Timing


SCK
CS#
SI
SO
Command (10h)
Address bits
High-Z
1


SCK
CS#
SI
SO
Address bits
Get Feature (0Fh)
Status register address (C0h)
MSB
High-Z
1
2


SCK
CS#
SI
SO
Status register address
Status register data out
Status register data out
High-Z
MSB
MSB
2
Don't Care

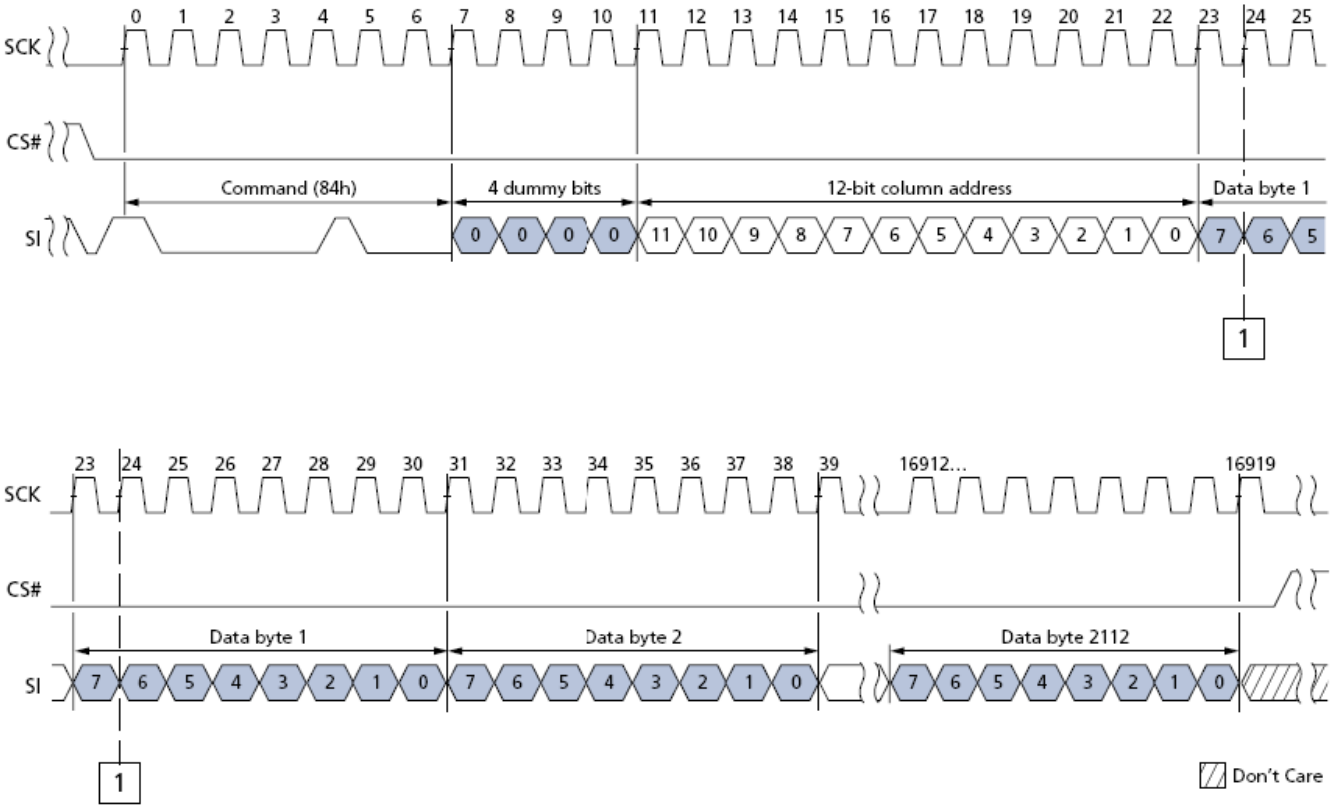


Figure 6.8 PROGRAM EXECUTE (10h) Timing

6.2.2 Random Data Program

The command sequence is as follows:

- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA x1) / 34h (x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

The random data program operation sequence programs or replaces data in a page with existing data. PROGRAM LOAD RANDOM DATA command requires 16-bit address with 4 dummy bits and a 12-bit column address. New data is loaded in the column address provided. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA command must be issued with a new column address. After the data is loaded, PROGRAM EXECUTE command can be issued to start the programming operation.

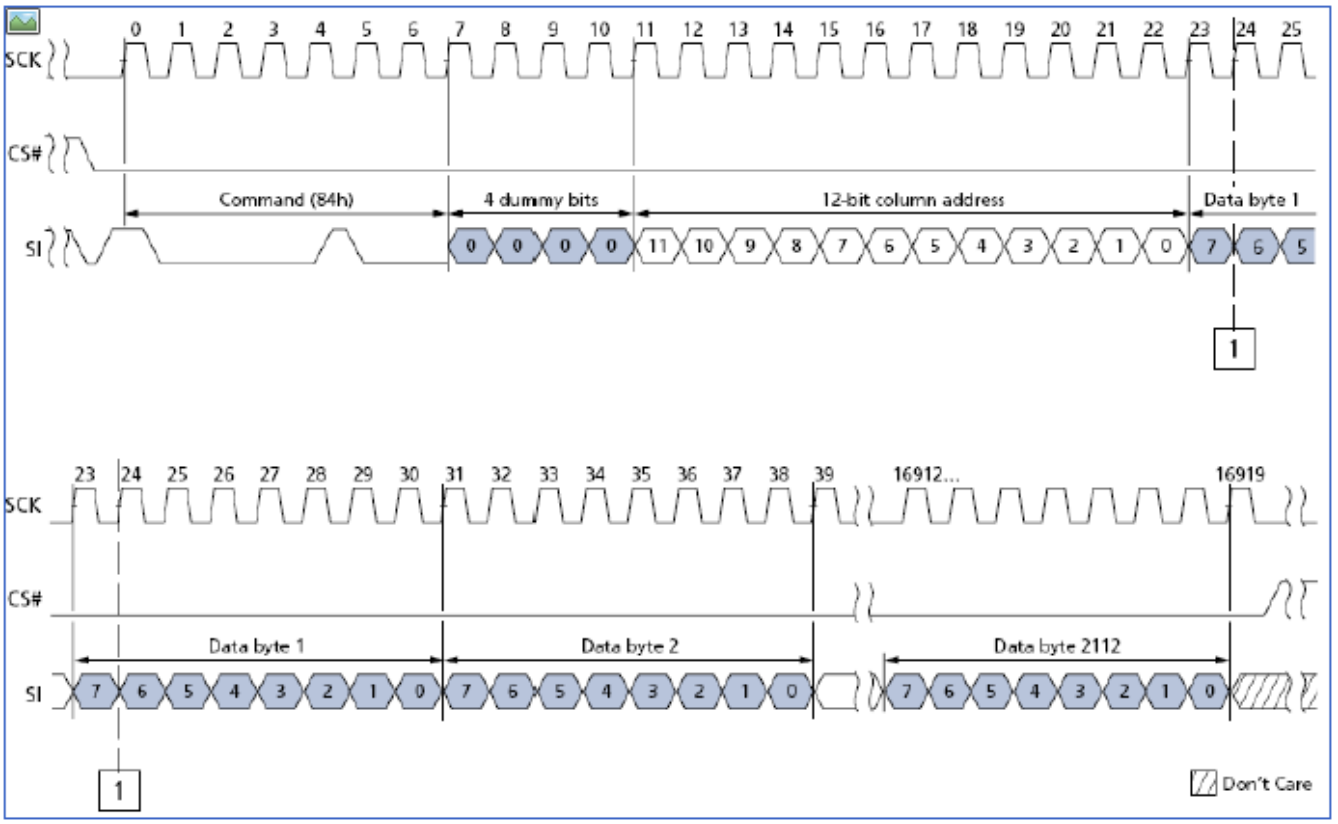


Figure 6.9 PROGRAM LOAD RANDOM DATA (84h) Timing

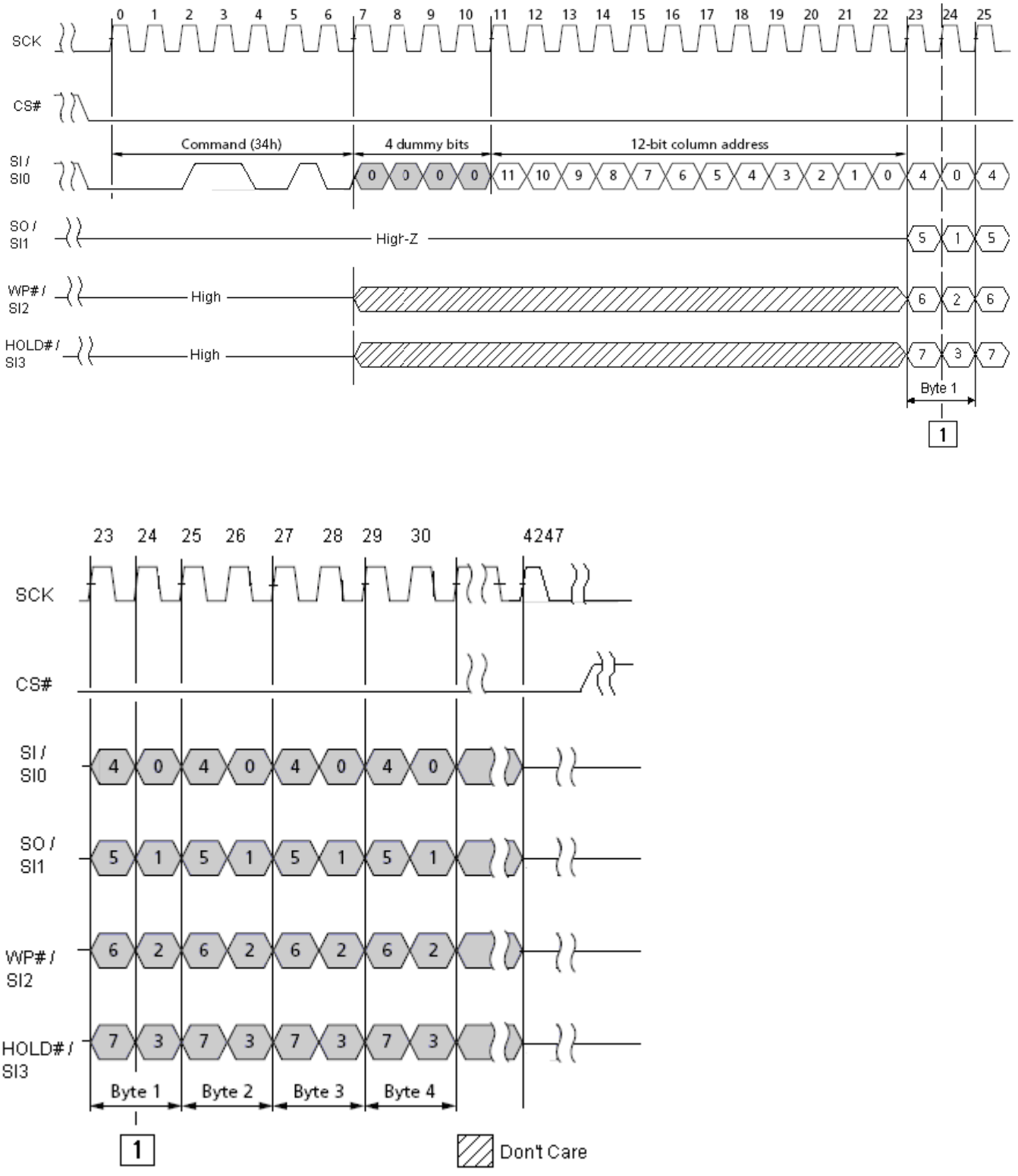
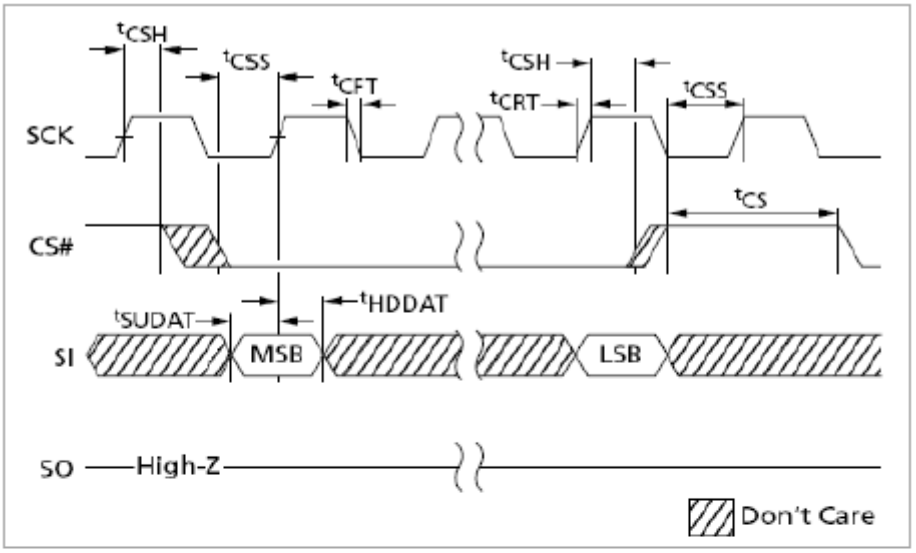


Figure 6.10 PROGRAM LOAD RANDOM DATA x4 (34h) Timing



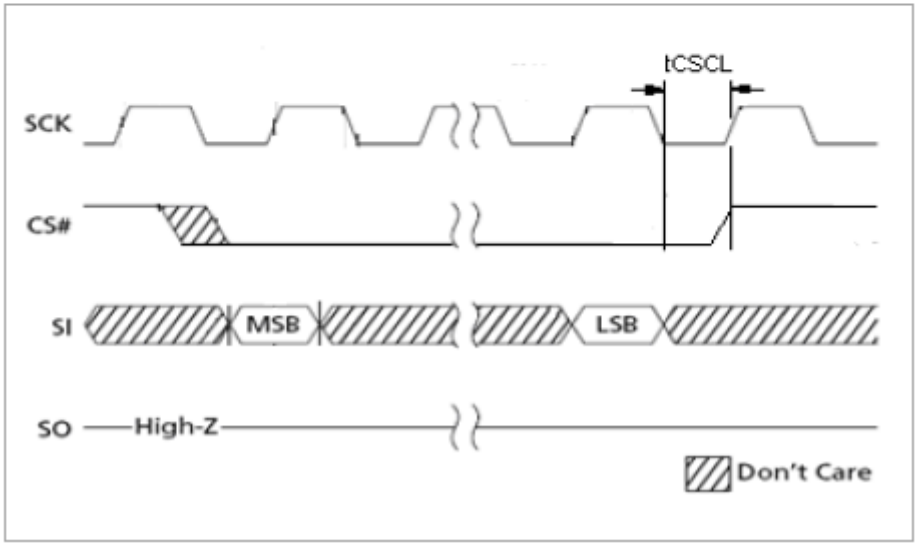


Figure 6.11 Serial Input and tCSCL Timing

6.3 INTERNAL DATA MOVE

The command sequence is as follows:

- 13h (PAGE READ to cache)
- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA x1) / 34h(x4); this is OPTIONAL in sequence
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

The INTERNAL DATA MOVE operation sequence programs or replaces data in a page with existing data. Prior to performing an INTERNAL DATA MOVE operation, the target page content must be read into the cache register. PAGE READ command must be followed with a WRITE ENABLE command to change the contents of memory array.

6.4 ERASE OPERATION

The command sequence is as follows:

- 06h (WRITE ENABLE)
- D8h (BLOCK ERASE)
- 0Fh (GET FEATURE command to read the status)

BLOCK ERASE command requires 24-bit address with 8 dummy bits and a 16-bit row address. If WRITE ENABLE command is not issued (WEL bit is not set), then the rest of the erase sequence is ignored. After the row address is registered, the control logic automatically controls the timing and the erase-verify operations, and the device is busy for t_{BERS} time. BLOCK ERASE command operates on one block at a time.

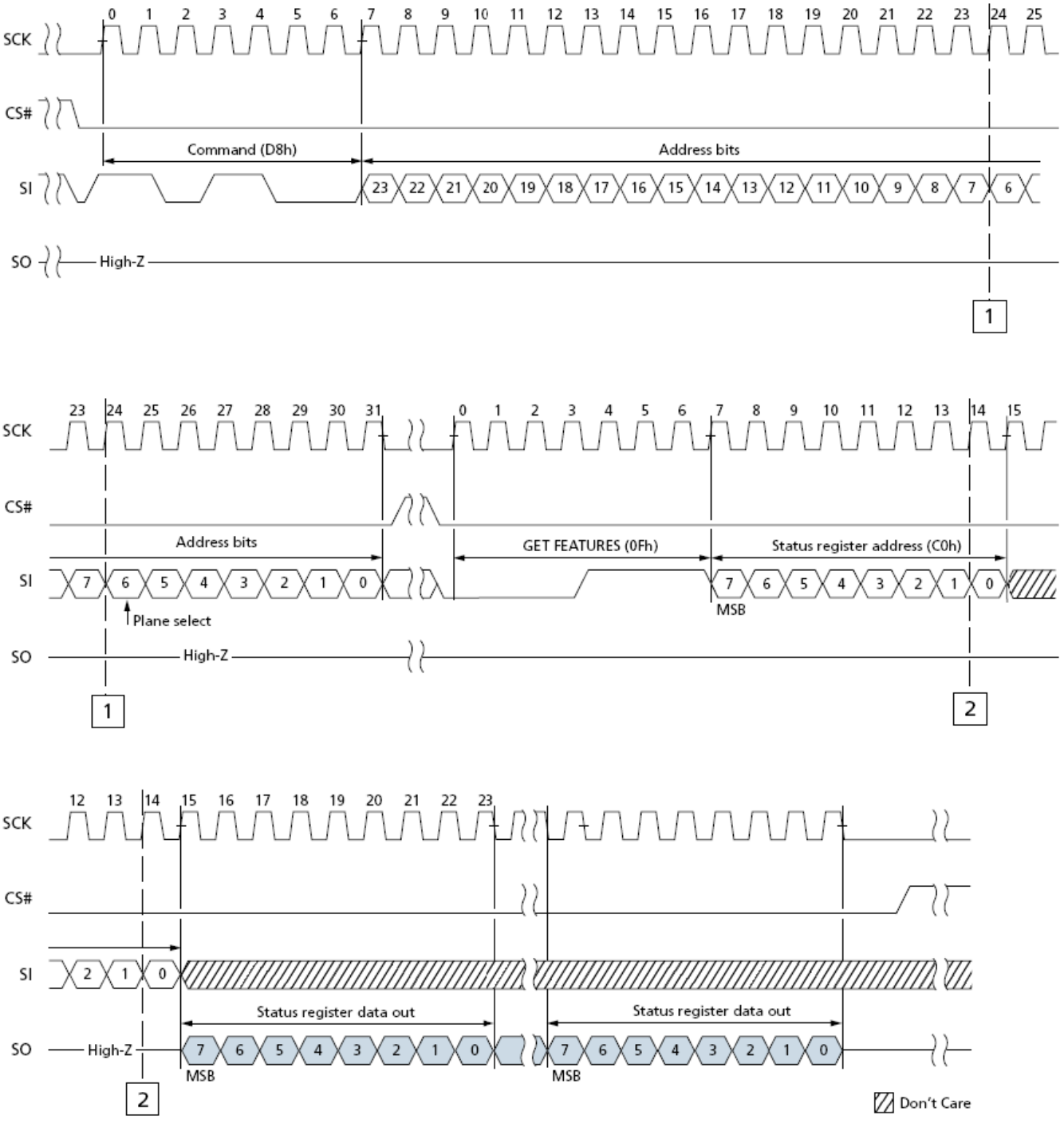


Figure 6.12 BLOCK ERASE (D8h) Timing

6.5 READ ID

The device contains a product identification mode, initiated by writing 9Fh to the command register. Five read cycles sequentially output the manufacturer code (C8h) and the device code and 3rd, 4th, 5th cycle ID respectively after a dummy byte. The command register remains in Read ID mode until further commands are issued to it.

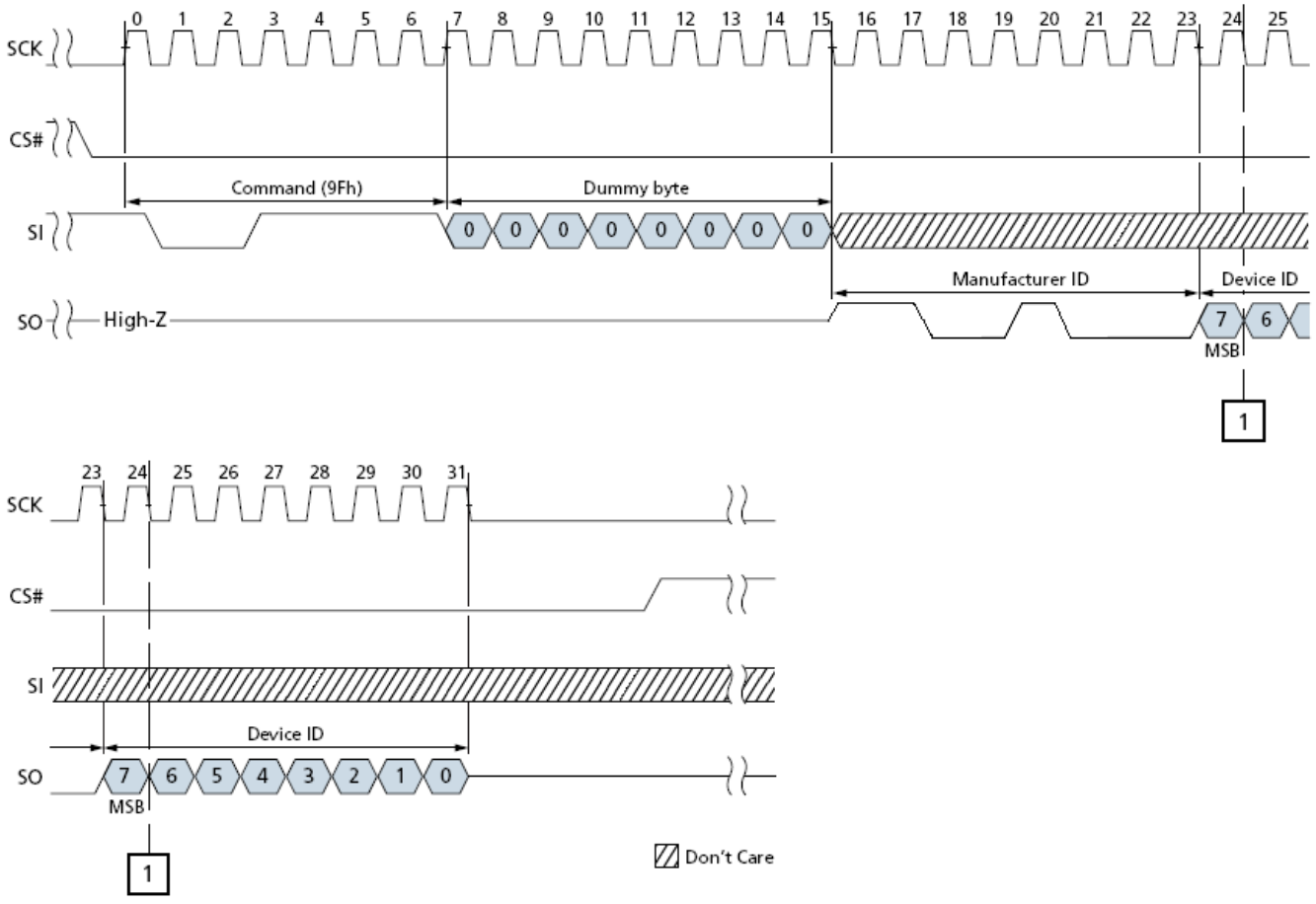


Figure 6.13 Read ID Timing

Part No.	1st Cycle (Maker Code)	2nd Cycle (Device Code)	3rd Cycle	4th Cycle	5th Cycle
IS37/38SML01G1	C8h	21h	7Fh	7Fh	7Fh

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	JEDEC Maker Code Continuation Code, 7Fh
4th Byte	JEDEC Maker Code Continuation Code, 7Fh
5th Byte	JEDEC Maker Code Continuation Code, 7Fh

Table 6.1 ID Definition Table

6.6 WP# TIMING

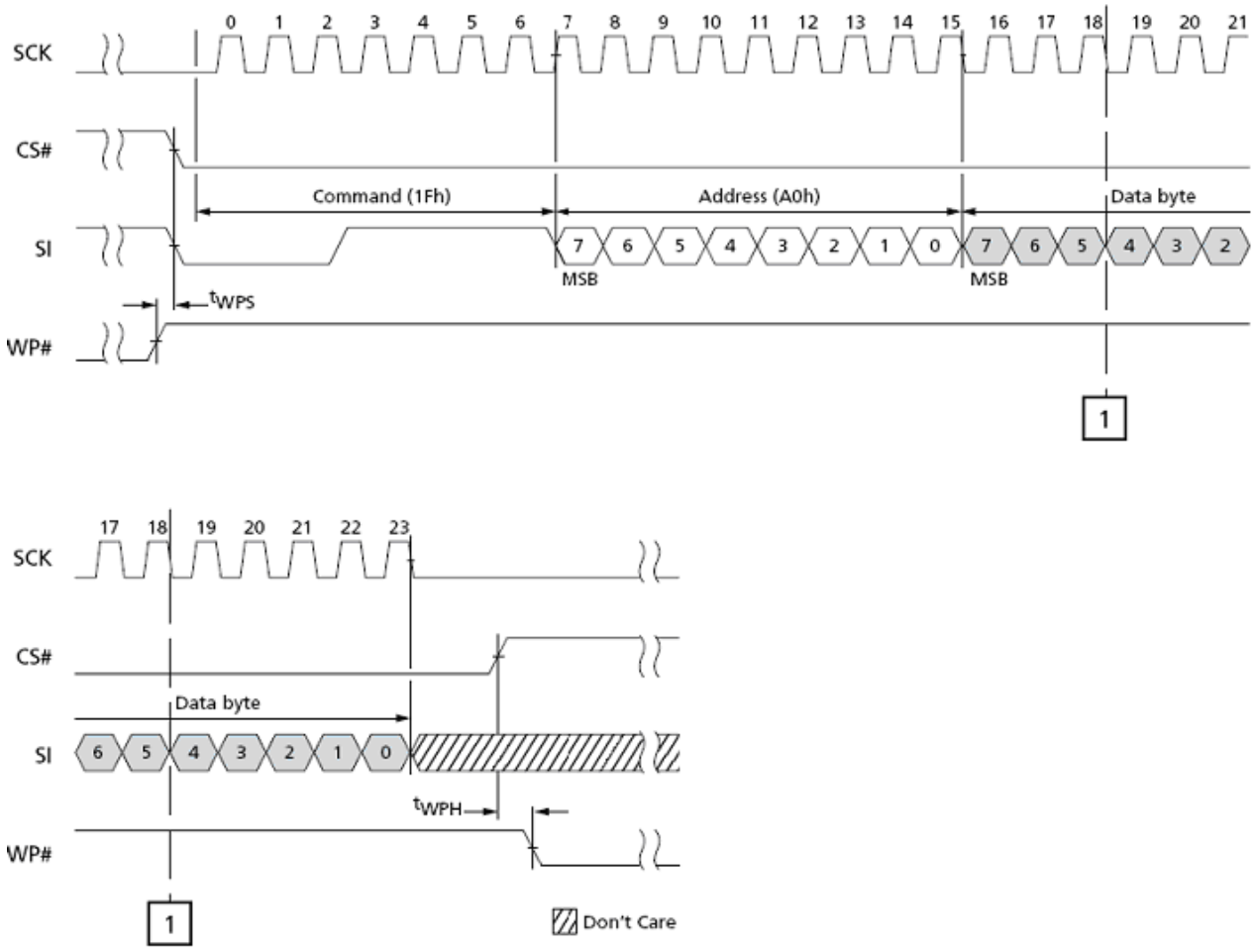


Figure 6.14 WP# Timing

6.7 HOLD# TIMING

HOLD# input provides a method to pause serial communication with the device but doesn't terminate any READ, PROGRAM, or ERASE operation currently in progress.

Hold mode starts at the falling edge of HOLD# provided SCK is also Low. If SCK is High when HOLD# goes Low, hold mode begins after the next falling edge of SCK. Similarly, hold mode is exited at the rising edge of HOLD# provided SCK is also Low. If SCK is High, hold mode ends after the next falling edge of SCK.

During hold mode, SO is Hi-Z, and SCK inputs are ignored.

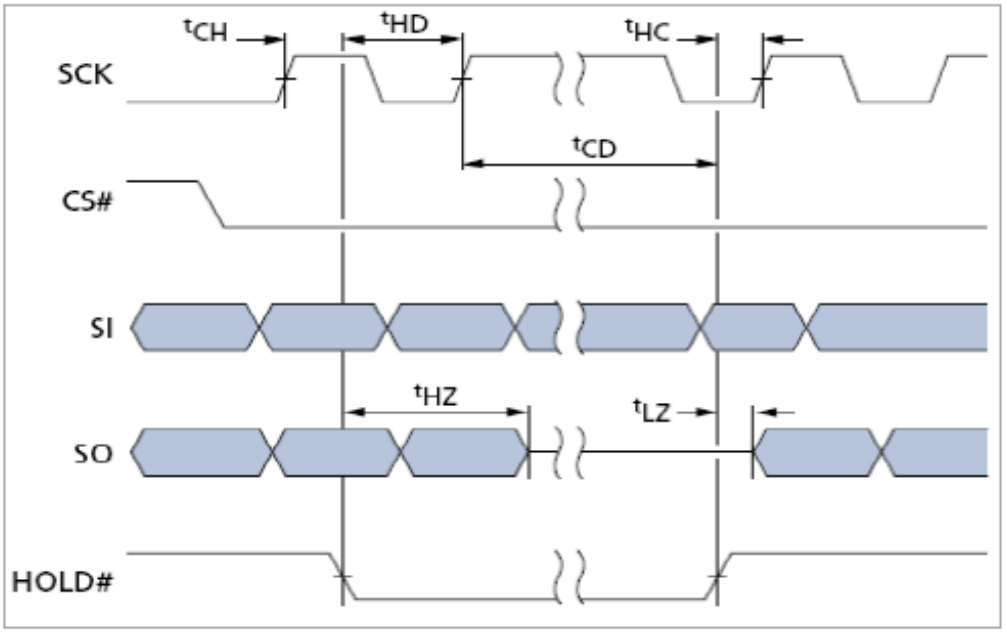


Figure 6.15 HOLD# Timing

6.8 POWER-UP

During power transitions, the device can be selected after tVCE. CS# = HIGH is recommended until the end of tVCE.

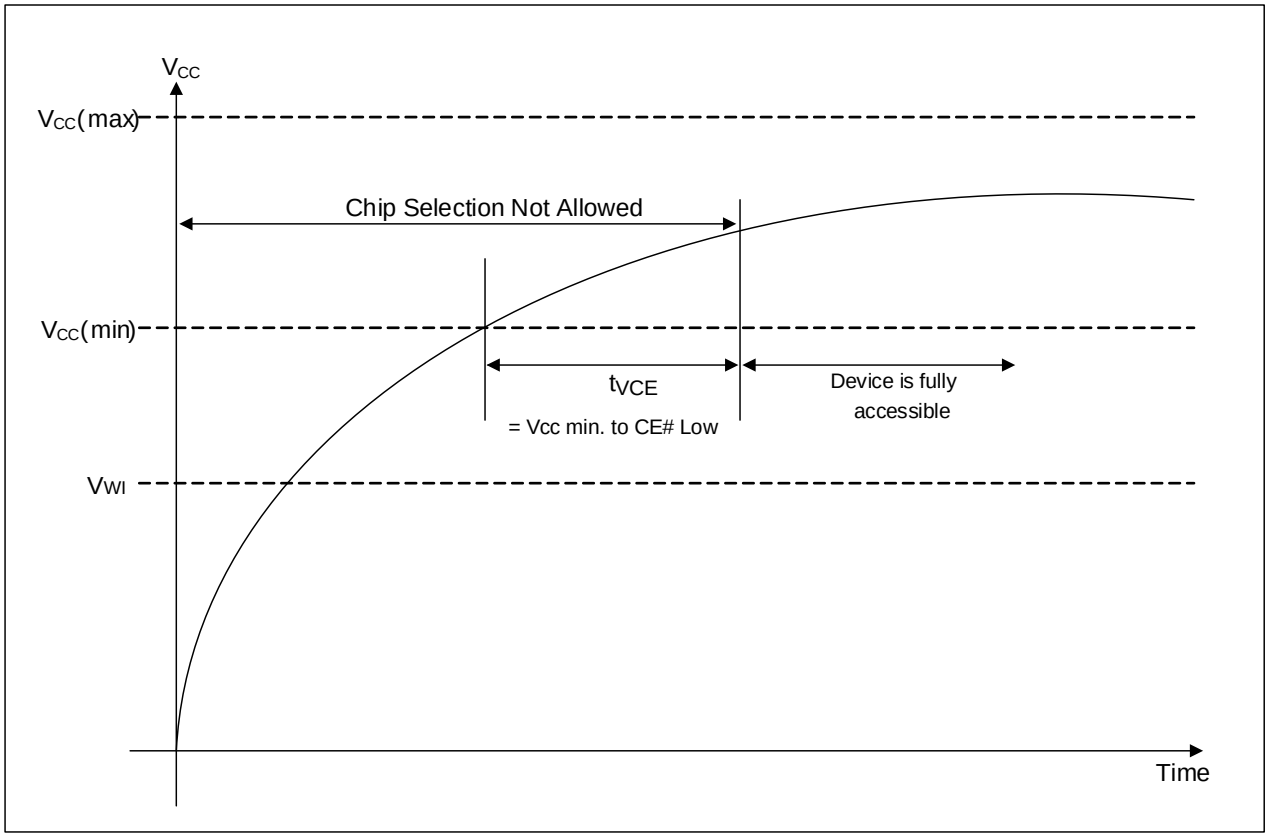


Figure 6.16 Power-Up Timing

Symbol	Parameter	Min.	Max	Unit
tVCE(1)	Vcc(min) to CE# Low	1250		us
V_{WI}(1)	Write Inhibit Voltage		2.5	V

Note: 1.These parameters are characterized and not 100% tested.

Table 6.2 Power Up Timing Table

Table 6.1 ID Definition Table

7. BUS/FEATURE OPERATION AND ERROR MANAGEMENT

7.1 BUS OPERATION

SPI NAND supports two SPI modes:

(Mode 0) CPOL (clock polarity) = 0, CPHA (clock phase) = 0
(Mode 1) CPOL (clock polarity) = 1, CPHA (clock phase) = 1

Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes.

When CS# is High, keep SCK at Vss (Mode 0) or Vcc (Mode 3). Do not begin toggling SCK until after CS# is driven Low.

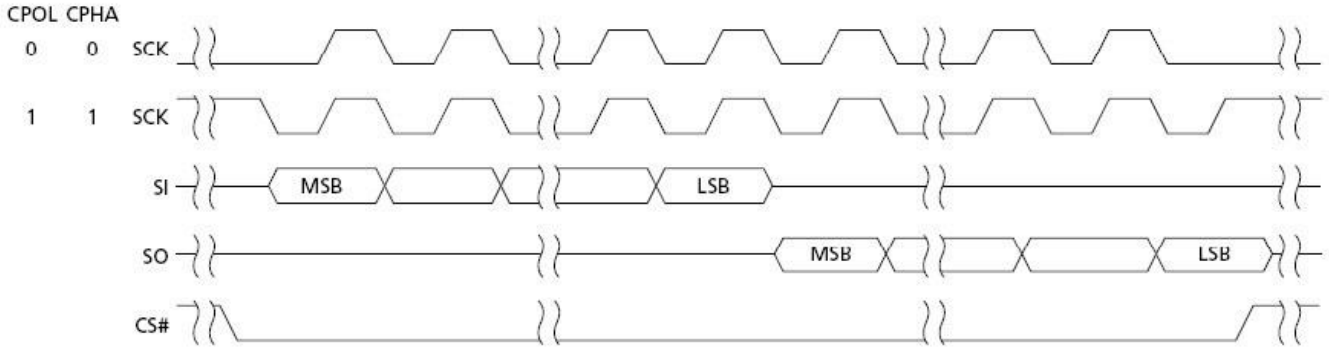


Figure 7.1 SPI Modes Timing

7.2 FEATURE OPERATIONS

The GET FEATURE (0Fh) and SET FEATURE (1Fh) commands are used to alter the device behavior from the default power-on behavior. These commands use a 1-Byte feature address to determine which feature is to be read or modified.

When a feature is set, it remains active until the device is power cycled or the feature is written to.

Unless otherwise specified in the below Table, once the device is set, it remains set, even if a RESET (FFh) command is issued.

Table 7.1 Feature Settings

Register	Address	Data Bits							
		7	6	5	4	3	2	1	0
Block Lock[1]	A0h	BRWD	Reserved	BP2	BP1	BP0	Reserved	Reserved	Reserved
OTP	B0h	OTP Protect	OTP Enable	Reserved	ECC Enable[2]	Reserved	Reserved	Reserved	Reserved
Status	C0h	Reserved	Reserved	ECC_S1	ECC_S0	P_Fail	E_Fail	WEL[3]	OIP
Output Driver	D0h[4]	Reserved	DRV_S1	DRV_S0	Reserved	Reserved	Reserved	Reserved	Reserved

Notes:

1. **38h is the default data byte value for Block Lock Register after power-up.**
2. **1-bit internal ECC for all READ and PROGRAM operations can be enabled (ECC enable = 1) or disabled (ECC disable = 0); (10h) is the default data byte value for OTP Register after power-up.**
3. **WEL = 0 is the default data bit value for Status Register after power-up.**
4. **(20h) is the default data byte value for Output Driver Register after power-up**

Table 7.2 Block Protect Bits of Block Lock Register

BP2 (5)	BP1 (4)	BP0 (3)	Protected Rows
0	0	0	None; all unlocked
0	0	1	Upper 1/64 locked
0	1	0	Upper 1/32 locked
0	1	1	Upper 1/16 locked
1	0	0	Upper 1/8 locked
1	0	1	Upper 1/4 locked
1	1	0	Upper 1/2 locked
1	1	1	All locked (default)

Table 7.3 OTP Status Bits of OTP Register

OTP Protect Bit (7)	OTP Enable Bit (6)	State
0	0	Normal operation (read array)
0	1	Access OTP space
1	0	Not applicable
1	1	Lock the OTP area

Table 7.4 Driver Strength Bits of Output Driver Register

DRV_S1	DRV_S0	Driver Strength
0	0	100%
0	1	75%
1	0	50%
1	1	25%

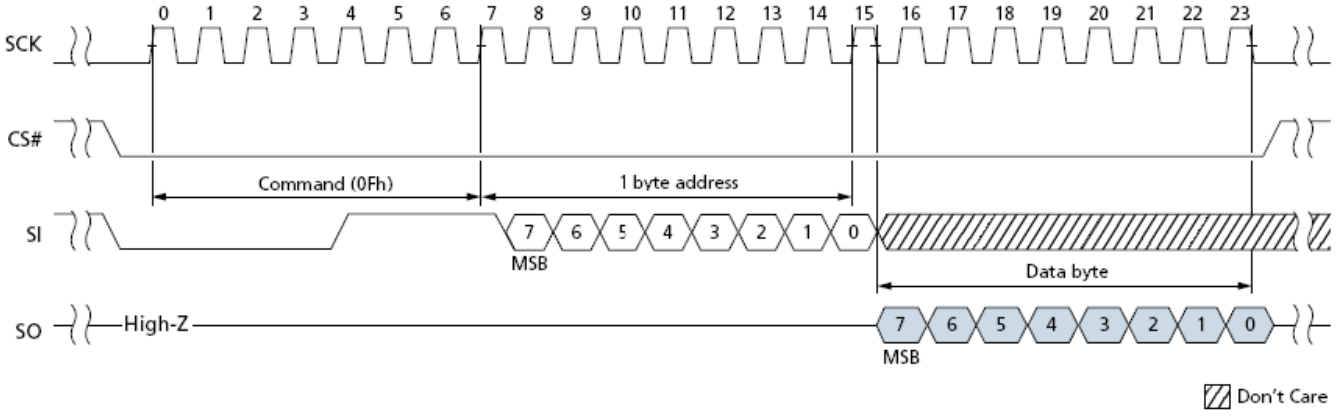


Figure 7.2 GET FEATURE (0Fh) Timing

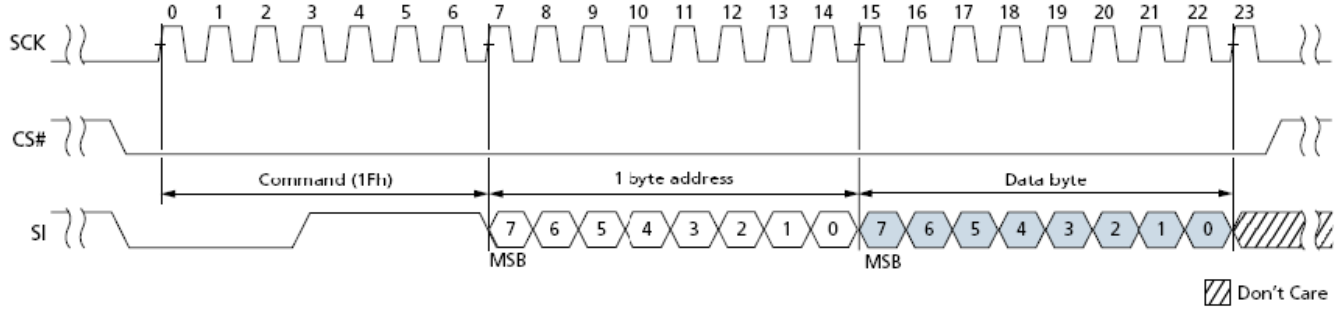


Figure 7.2 SET FEATURE (1Fh) Timing

7.3 ARRAY WRITE ENABLE / DISABLE

The WRITE ENABLE (06h) command sets the WEL bit (in status register) to 1. This required in the following WRITE operations that change the contents of the memory array. PAGE PROGRAM, BLOCK ERASE, and OTP PROGRAM.

Contrarily, the WRITE DISABLE (04h) command sets the WEL bit to 0. This disables PAGE PROGRAM, BLOCK ERASE, and OTP PROGRAM.

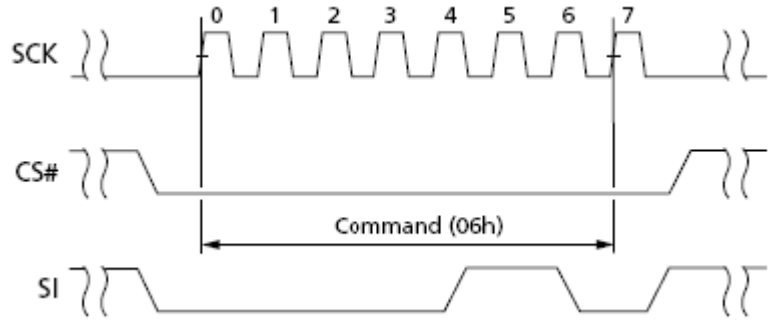


Figure 7.3 WRITE ENABLE (06h) Timing

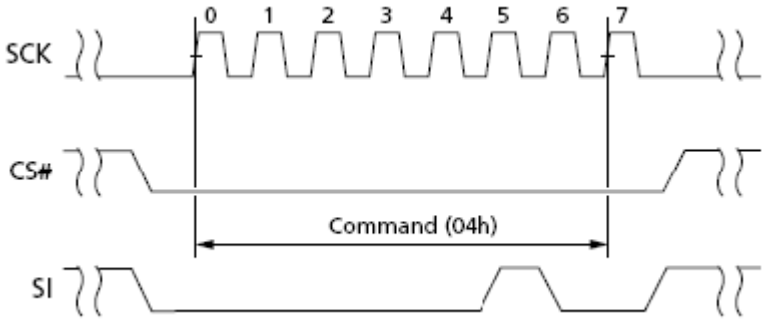


Figure 7.4 WRITE DISABLE (04h) Timing

7.4 STATUS REGISTER

Software can read status register during the NAND device operation by issuing GET FEATURE (0Fh) command, followed by the feature address C0h. The status register will output the status of the operation.

Refer to Table 7.1, Table 7.5 and Table 7.6.

Table 7.5 Bits of Status Register

Bit	Name	Mode	DESCRIPTION
[5:4]	ECC_S1, ECC_S0	R	ECC_S1 and ECC_S0 are set to 00h either following a RESET, or at the beginning of the READ. Then updated after the device completes a valid READ operation. ECC_S1/S0 are invalid if ECC is disabled. After power-up, ECC_S1 and ECC_S2 are set to reflect the contents of block 0, page 0.
[3]	Program Fail	R	P_Fail is set to “1” as a program failure has occurred. P_Fail = “1” will also be set if the user attempts to program an invalid address or a locked region. P_Fail is set to “0” during the PROGRAM EXECUTE command sequence or the RESET command.
[2]	Erase Fail	R	E_Fail is set to “1” as an erase failure has occurred. E_Fail = “1” will also be set if the user attempts to erase a locked region, or if ERASE operation fails. E_Fail is set to “0” during the BLOCK ERASE command sequence or the RESET command.
[1]	Write Enable Latch	W	WEL must be set to ‘1” to indicate the current status of the write enable latch, prior to issuing PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing WRITE ENABLE command. WEL is disabled (WEL=”0”) by issuing the WRITE DISABLE command.
[0]	Operation In Progress	R	OIP is set to “1” when the device is busy; it means a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, or RESET command is executing. OIP is cleared to “0” as the interface is in ready state.

Table 7.6 ECC Status Bits of Status Register

ECCS1 (5)	ECCS0 (4)	Description
0	0	No errors
0	1	1-bit error detected and corrected
1	0	2-bit errors detected and not corrected
1	1	Reserved

7.5 ERROR MANAGEMENT

7.5.1 MASK OUT INITIAL INVALID BLOCKS

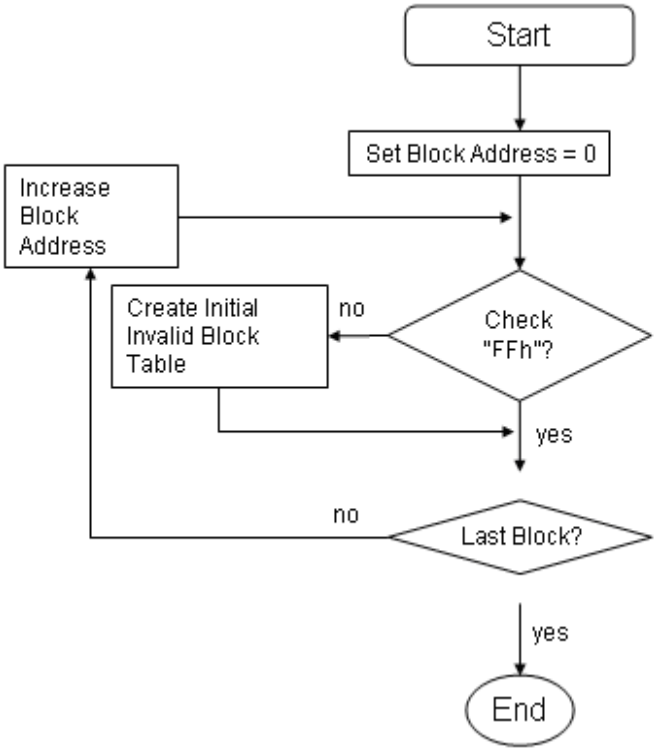
Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by ISSI. The information regarding the initial invalid blocks is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping.

The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/512Byte ECC.

7.5.2 IDENTIFYING INITIAL INVALID BLOCKS

Unpredictable behavior may result from programming or erasing the defective blocks. Figure 7.5 below illustrates an algorithm for searching factory-mapped defects, and the algorithm needs to be executed prior to any erase or program operations.

A host controller has to scan blocks from block 0 to the last block using page read command and check the data at the column address of 2,048 of page 0 and page 1. If the read data is not FFh, the block is interpreted as an invalid block. Do not erase or program factory-marked bad blocks. The host controller must be able to recognize the initial invalid block information and to create a corresponding table to manage block replacement upon erase or program error when additional invalid blocks develop with Flash memory usage.



Check “FFh” at column address 2048 of the first page and the second page

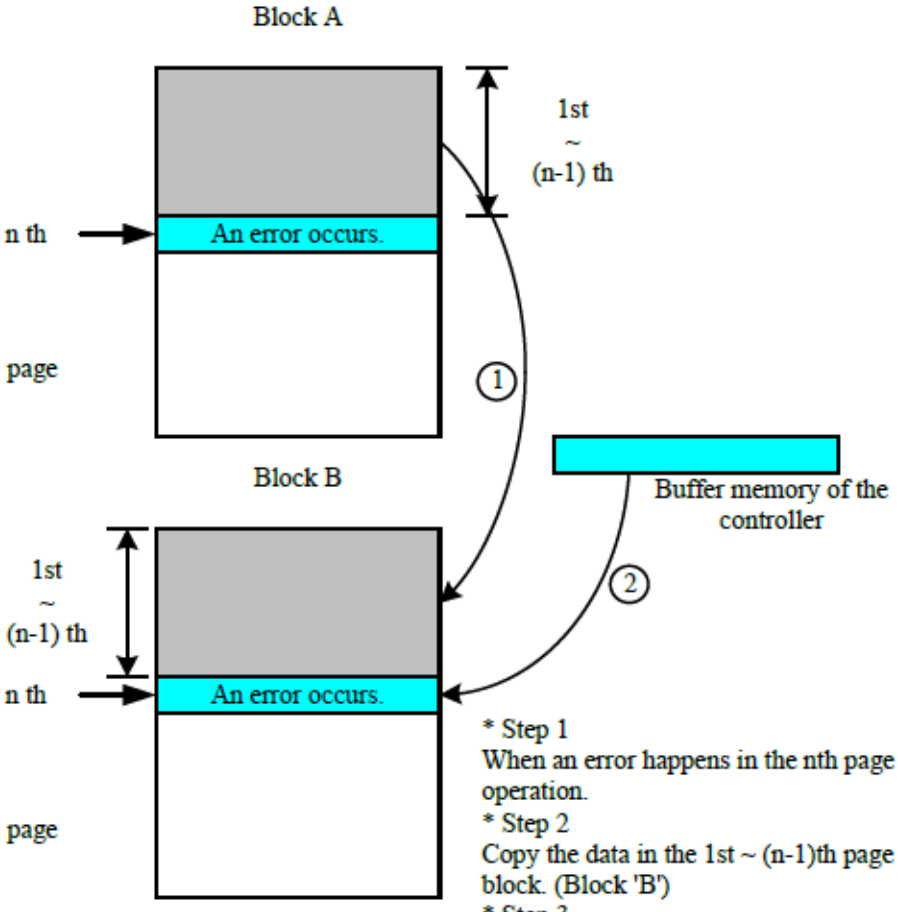
```
For (i=0; i<Num_of_LUs; i++)
{
   For (j=0; j<Blocks_Per_LU; j++)
   {
      Defect_Block_Found=False;

      Read_Page(lu=i, block=j, page=0);
      If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)  Defect_Block_Found=True;

      Read_Page(lu=i, block=j, 1);
      If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)  Defect_Block_Found=True;

      If (Defect_Block_Found)  Mark_Block_as_Defective(lu=i, block=j);
   }
  }
```

Figure 7.5 Algorithm for Bad Block Scanning

7.5.3 BLOCK REPLACEMENT

Within its lifetime, number of invalid blocks may increase with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of failure after ERASE or PROGRAM in status register, block replacement should be done. Because PROGRAM status fail during a page program does not affect the data of other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block.

In case of READ, ECC must be employed. To improve the efficiency of memory space, it is recommended that read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The additional block failure rate does not include those reclaimed blocks.



* Step 1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step 2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step 3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'
* Step 4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

Figure 7.6 Blcok Replacement

7.5.4 ECC PROTECTION

ECC is enabled after device power-up, so the default PROGRAM and READ commands operate with internal ECC in the active state.

During a PROGRAM operation, the device calculates an ECC code on the 2KB page in the cache register, before the page is written to the NAND Flash array. The ECC code is stored in the spare area of the page in array.

During a READ operation, the page data is read from the array to the cache register, where ECC code is calculated and compared with the ECC code value read from the array. If a single-bit data error is discovered, the error is corrected in the cache register and only the corrected data is on the output pins.

Table 7.7 ECC Protection

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
1FFh (511)	000h (0)	Yes	Main 0	User data 0[1]
3FFh (1023)	200h (512)	Yes	Main 1	User data 1[1]
5FFh (1535)	400h (1024)	Yes	Main 2	User data 2[1]
7FFh (2047)	600h (1536)	Yes	Main 3	User data 3[1]
800h (2048)	800h (2048)	No		Reserved
803h (2051)	801h (2049)	No		ECC for main 0[2]
807h (2055)	804h (2052)	Yes		ECC for spare 0[2]
80Fh (2063)	808h (2056)	Yes	Spare 0	User meta data 0[1]
810h (2064)	810h (2064)	No		Reserved
813h (2067)	811h (2065)	No		ECC for main 1[2]
817h (2071)	814h (2068)	Yes		ECC for spare 1[2]
81Fh (2079)	818h (2072)	Yes	Spare 1	User meta data 1[1]
820h (2080)	820h (2080)	No		Reserved
823h (2083)	821h (2081)	No		ECC for main 2[2]
827h (2087)	824h (2084)	Yes		ECC for spare 2[2]
82Fh (2095)	828h (2088)	Yes	Spare 2	User meta data 2[1]
830h (2096)	830h (2096)	No		Reserved
833h (2099)	831h (2097)	No		ECC for main 3[2]
837h (2103)	834h (2100)	Yes		ECC for spare 3[2]
83Fh (2111)	838h (2104)	Yes	Spare 3	User meta data 3[1]
FFFh (4095)	840h (2112)	No		Reserved

Notes:

1. **The user area must be programmed within a single partial-page programming operations so NAND Flash device can calculate the proper ECC bytes.**
2. **When internal ECC is enabled, these areas are prohibited to be programming.**

7.6 ADDRESSING FOR PROGRAMMING OPERATION

Within a block, the page must be programmed consecutively from the LSB (Least Significant Bit) page of the block to MSB (Most Significant Bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed.

Therefore, LSB page doesn't need to be page 0.

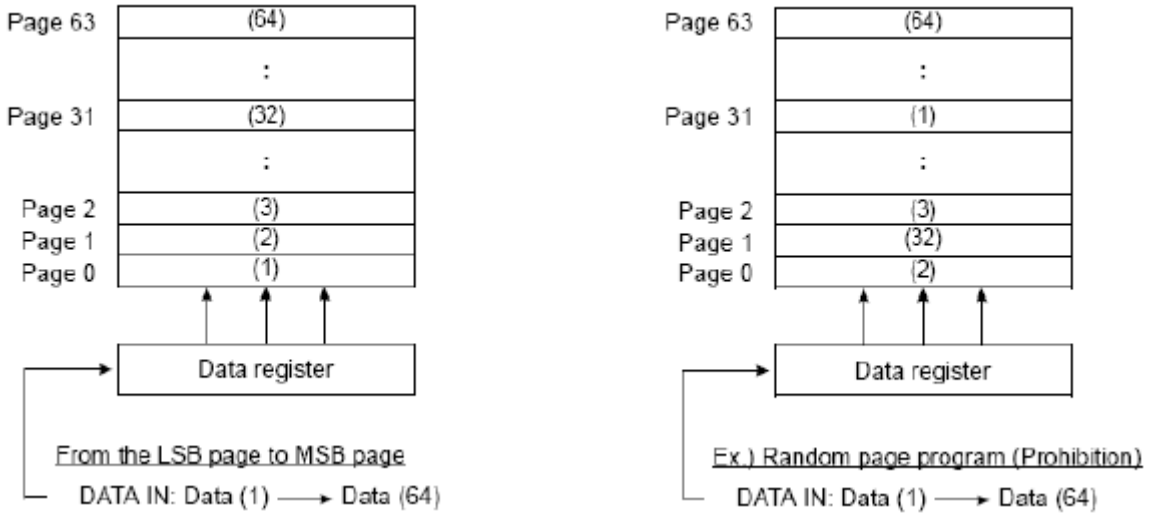
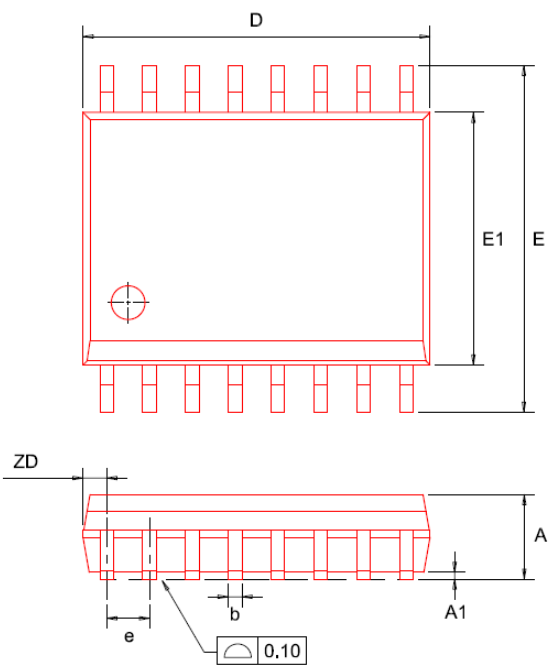


Figure 7.7 Addressing for Program Operation

8. PACKAGE TYPE INFORMATION

8.1 16-LEAD PLASTIC SMALL OUTLINE PACKAGE (300 MILS BODY WIDTH) (M)



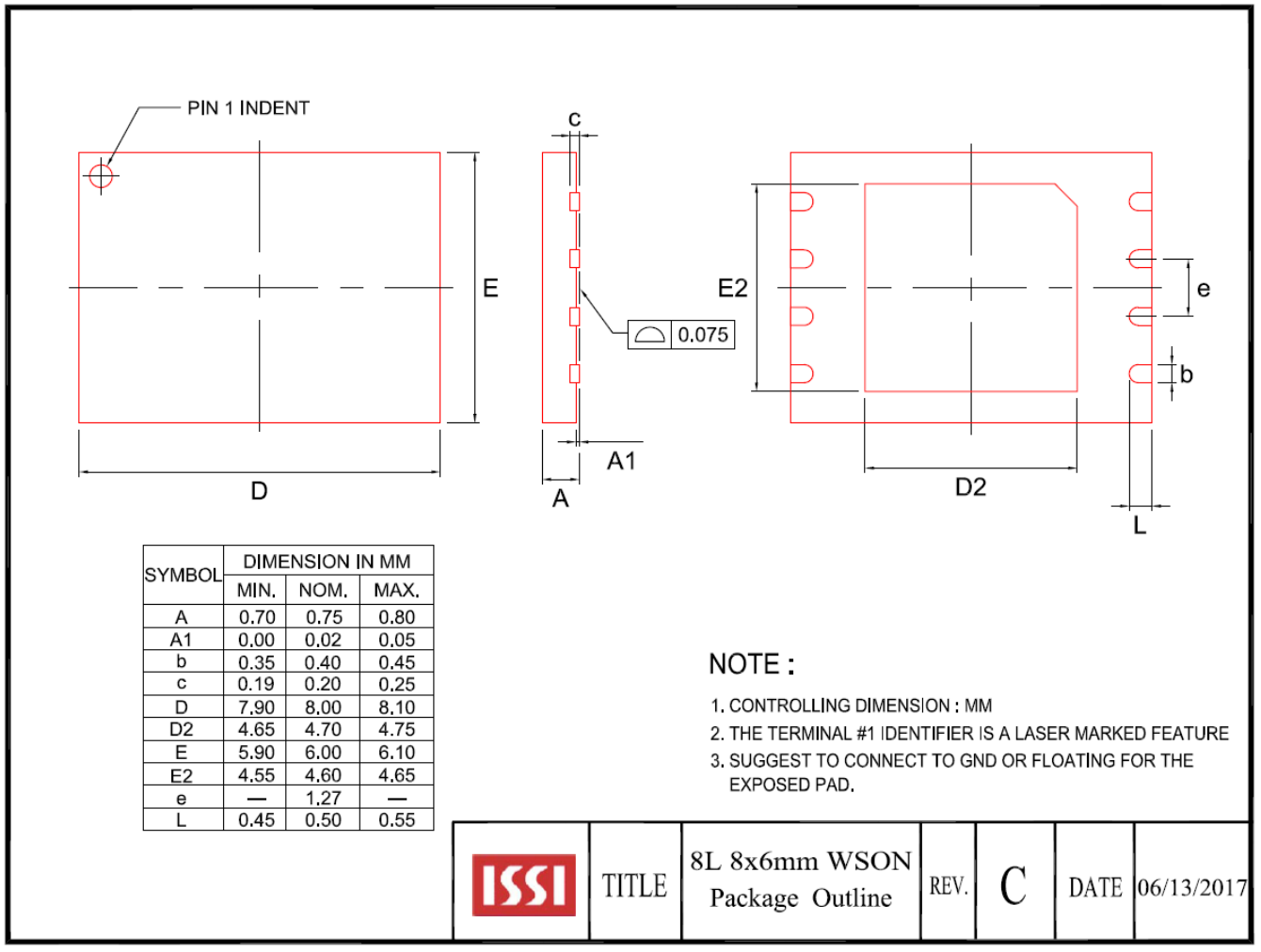
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	2.65
A1	0.10	—	0.30
b	0.31	—	0.51
D	10.08	10.31	10.49
E	10.01	10.31	10.64
E1	7.39	7.49	7.59
e	1.27 BSC.		
L	0.38	0.81	1.27
L2	0.25 BSC.		
ZD	0.705 BSC.		
Θ	0°	—	8°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

ISSI	TITLE	16L 300mil SOP Package Outline	REV.	A	DATE	06/26/2015

8.2 8-CONTACT ULTRA-THIN SMALL OUTLINE NO-LEAD (WSON) PACKAGE 8X6MM (L)



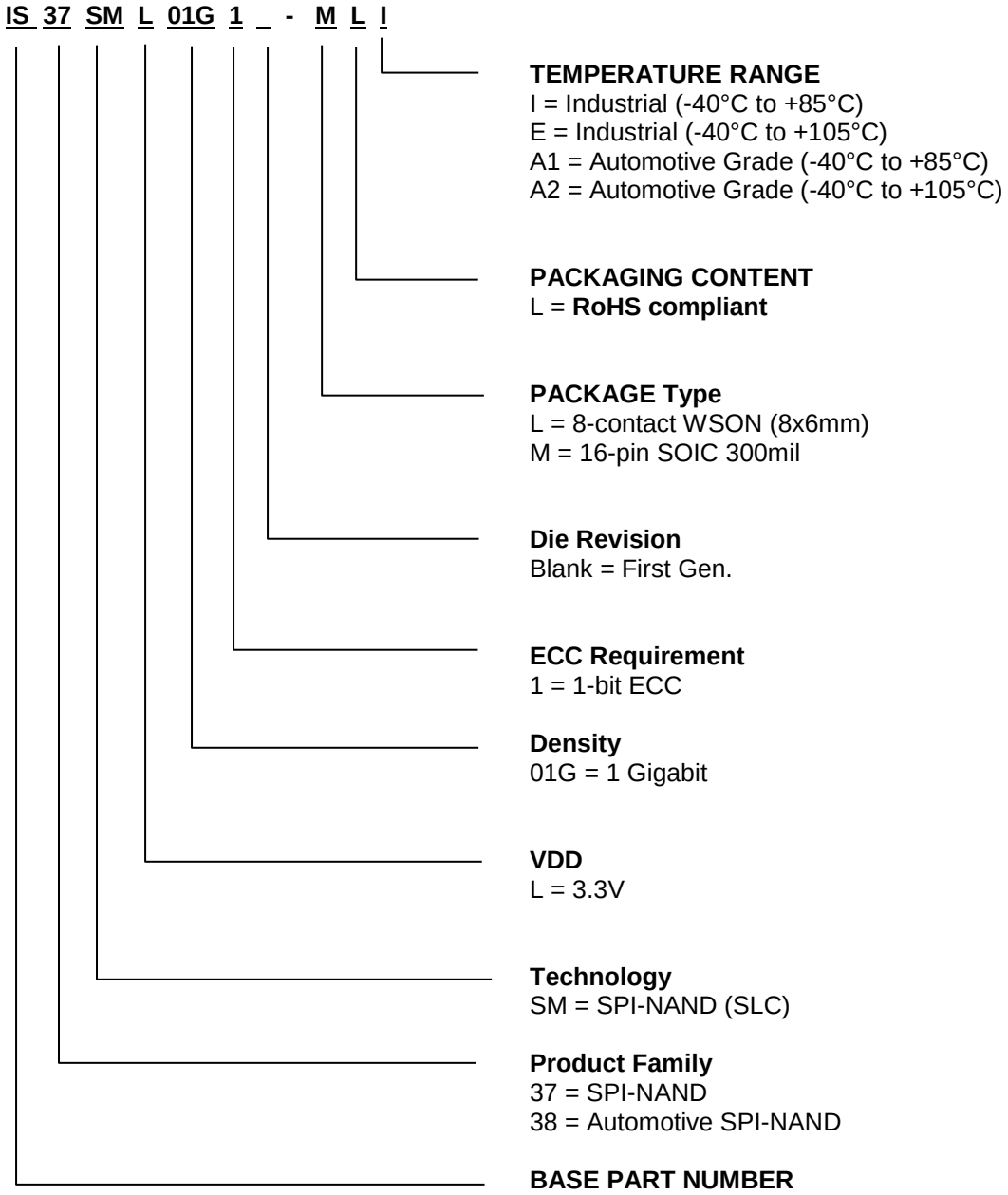
SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.35	0.40	0.45
c	0.19	0.20	0.25
D	7.90	8.00	8.10
D2	4.65	4.70	4.75
E	5.90	6.00	6.10
E2	4.55	4.60	4.65
e	—	1.27	—
L	0.45	0.50	0.55

NOTE :

1. CONTROLLING DIMENSION : MM
2. THE TERMINAL #1 IDENTIFIER IS A LASER MARKED FEATURE
3. SUGGEST TO CONNECT TO GND OR FLOATING FOR THE EXPOSED PAD.

	TITLE	8L 8x6mm WSON Package Outline	REV.	C	DATE	06/13/2017

9. ORDERING INFORMATION – Valid Part Numbers



Note:
1. Call Factory for other package options available.

VDD	Density	Bus	Temp. Grade	Order Part Number	Package
3.3V	1Gb	X8	Industrial	IS37SML01G1-MLI	16-pin SOIC 300mil
				IS37SML01G1-LLI	8-contact WSON 8x6mm
			Automotive (A1)	IS38SML01G1-MLA1	16-pin SOIC 300mil
				IS38SML01G1-LLA1	8-contact WSON 8x6mm
			Extended	IS37SML01G1-MLE	16-pin SOIC 300mil
				IS37SML01G1-LLE	8-contact WSON 8x6mm
			Automotive (A2)	IS38SML01G1-MLA2	16-pin SOIC 300mil
				IS38SML01G1-LLA2	8-contact WSON 8x6mm

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