IS42S16100H
IS45S16100H

Long-term Support
World Class Quality

512K Words x 16 Bits x 2 Banks
16Mb SYNCHRONOUS DYNAMIC RAM

OCTOBER 2016

FEATURES

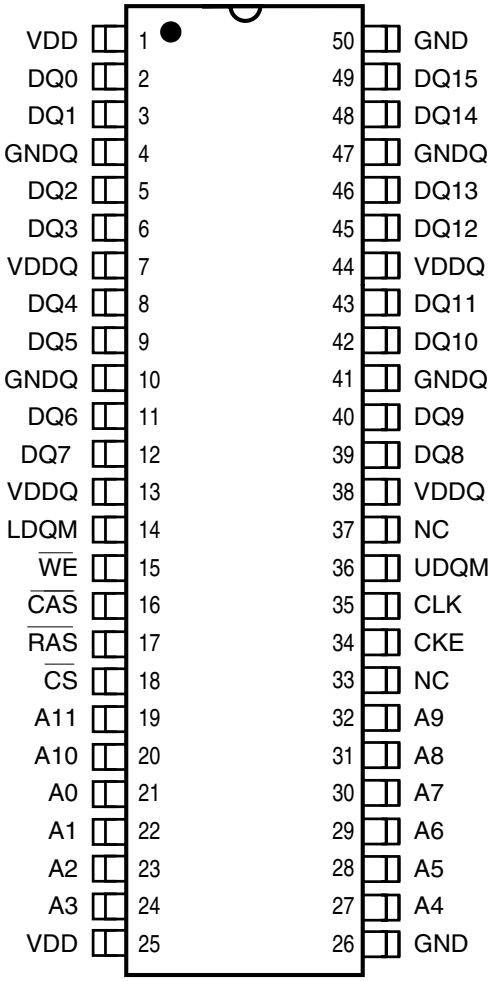
- Clock frequency: 200, 166, 143 MHz
- Fully synchronous; all signals referenced to a positive clock edge
- Two banks can be operated simultaneously and independently
- Dual internal bank controlled by A11 (bank select)
- Single 3.3V power supply
- LVTTL interface
- Programmable burst length
  – (1, 2, 4, 8, full page)
- Programmable burst sequence: Sequential/Interleave
- 2048 refresh cycles every 32ms (Com, Ind, A1 grade) or 16ms (A2 grade)
- Random column address every clock cycle
- Programmable $\overline{\text{CAS}}$ latency (2, 3 clocks)
- Burst read/write and burst read/single write operations capability
- Burst termination by burst stop and precharge command
- Byte controlled by LDQM and UDQM
- Packages: 400-mil 50-pin TSOP-II and 60-ball TF-BGA
- Temperature Grades:
  Commercial (0°C to +70°C)
  Industrial (-40°C to +85°C)
  Automotive A1 (-40°C to +85°C)
  Automotive A2 (-40°C to +105°C)

DESCRIPTION

ISSI's 16Mb Synchronous DRAM IS42/4516100H is organized as a 524,288-word x 16-bit x 2-bank for improved performance. The synchronous DRAMs achieve high-speed data transfer using pipeline architecture. All inputs and outputs signals refer to the rising edge of the clock input.

PIN CONFIGURATIONS

50-Pin TSOP (Type II)



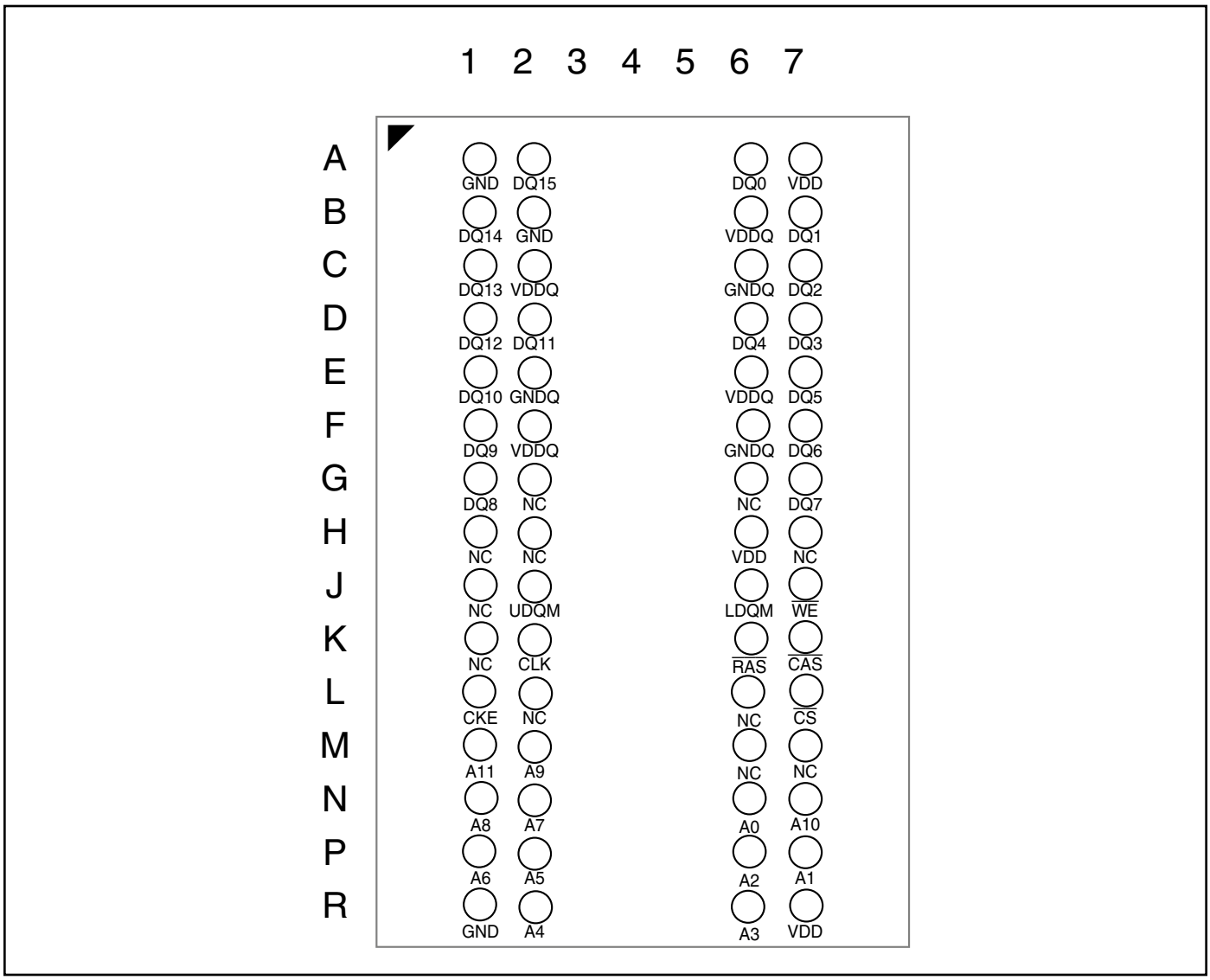
PIN DESCRIPTIONS

A0-A10	Row Address Input
A11	Bank Select Address
A0-A7	Column Address Input
DQ0 to DQ15	Data DQ
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command

$\overline{CAS}$	Column Address Strobe Command
$\overline{WE}$	Write Enable
LDQM	Lower Bye, Input/Output Mask
UDQM	Upper Bye, Input/Output Mask
VDD	Power
GND	Ground
VDDQ	Power Supply for DQ Pin
GNDQ	Ground for DQ Pin
NC	No Connection

PIN CONFIGURATION

PACKAGE CODE: B 60 BALL TF-BGA (Top View) (10.1 mm x 6.4 mm Body, 0.65 mm Ball Pitch)



PIN DESCRIPTIONS

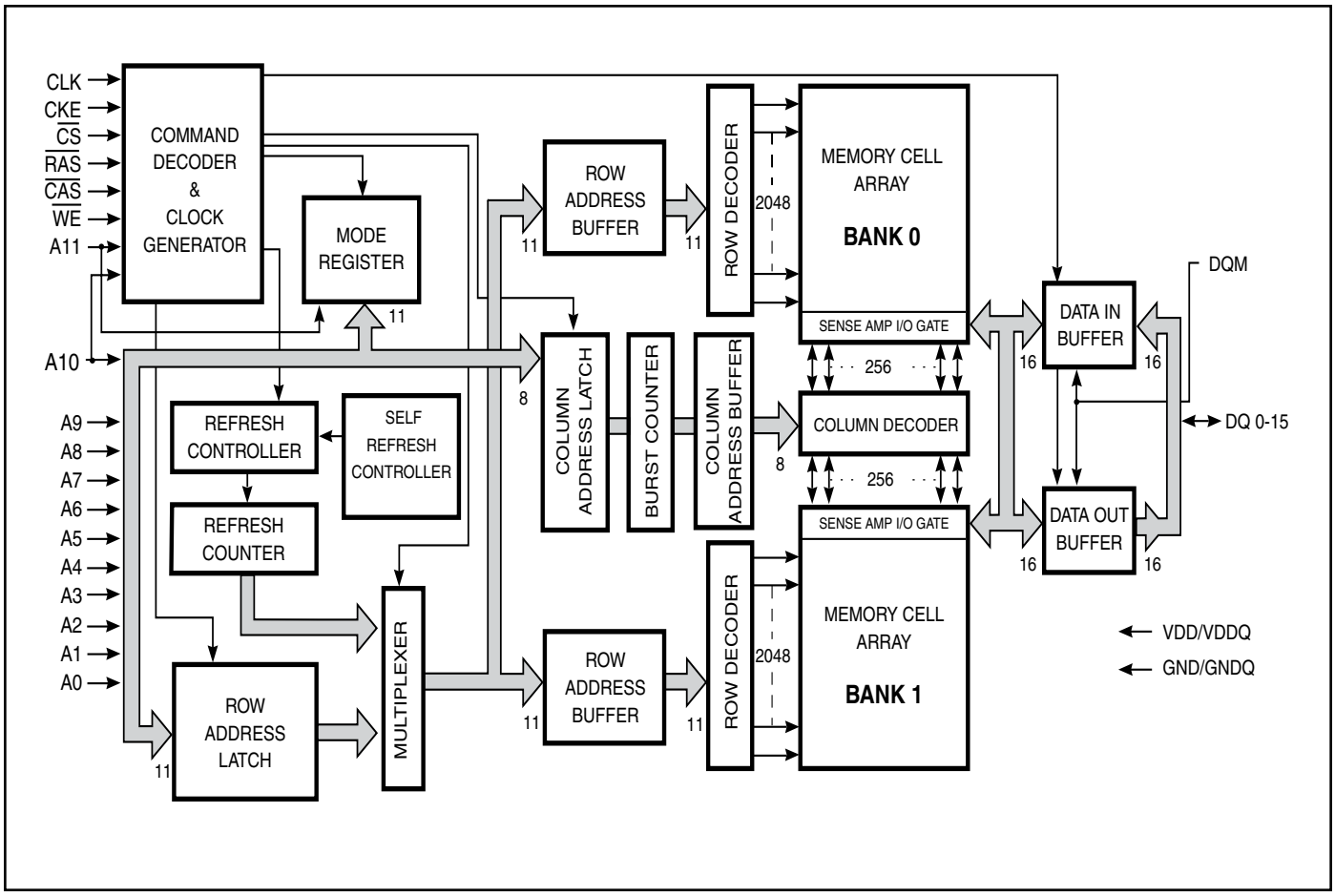
A0-A10	Row Address Input
A0-A7	Column Address Input
A11	Bank Select Address
DQ0 to DQ15	Data I/O
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command

$\overline{WE}$	Write Enable
LDQM, UDQM	x16 Input/Output Mask
V_{DD}	Power
GND	Ground
V_{DDQ}	Power Supply for I/O Pin
GND_Q	Ground for I/O Pin
NC	No Connection

PIN FUNCTIONS

TSOP Pin No.	Symbol	Type	Function (In Detail)
20 to 24 27 to 32	A0-A10	Input Pin	A0 to A10 are address inputs. A0-A10 are used as row address inputs during active command input and A0-A7 as column address inputs during read or write command input. A10 is also used to determine the precharge mode during other commands. If A10 is LOW during precharge command, the bank selected by A11 is precharged, but if A10 is HIGH, both banks will be precharged. When A10 is HIGH in read or write command cycle, the precharge starts automatically after the burst access. These signals become part of the OP CODE during mode register set command input.
19	A11	Input Pin	A11 is the bank selection signal. When A11 is LOW, bank 0 is selected and when high, bank 1 is selected. This signal becomes part of the OP CODE during mode register set command input.
16	$\overline{CAS}$	Input Pin	$\overline{CAS}$, in conjunction with the $\overline{RAS}$ and $\overline{WE}$, forms the device command. See the "Command Truth Table" item for details on device commands.
34	CKE	Input Pin	The CKE input determines whether the CLK input is enabled within the device. When is CKE HIGH, the next rising edge of the CLK signal will be valid, and when LOW, invalid. When CKE is LOW, the device will be in either the power-down mode, the clock suspend mode, or the self refresh mode. The CKE is an asynchronous input.
35	CLK	Input Pin	CLK is the master clock input for this device. Except for CKE, all inputs to this device are acquired in synchronization with the rising edge of this pin.
18	$\overline{CS}$	Input Pin	The $\overline{CS}$ input determines whether command input is enabled within the device. Command input is enabled when $\overline{CS}$ is LOW, and disabled with $\overline{CS}$ is HIGH. The device remains in the previous state when $\overline{CS}$ is HIGH.
2, 3, 5, 6, 8, 9, 11 12, 39, 40, 42, 43, 45, 46, 48, 49	DQ0 to DQ15	DQ Pin	DQ0 to DQ15 are DQ pins. DQ through these pins can be controlled in byte units using the LDQM and UDQM pins.
14, 36	LDQM, UDQM	Input Pin	LDQM and UDQM control the lower and upper bytes of the DQ buffers. In read mode, LDQM and UDQM control the output buffer. When LDQM or UDQM is LOW, the corresponding buffer byte is enabled, and when HIGH, disabled. The outputs go to the HIGH impedance state when LDQM/UDQM is HIGH. This function corresponds to $\overline{OE}$ in conventional DRAMs. In write mode, LDQM and UDQM control the input buffer. When LDQM or UDQM is LOW, the corresponding buffer byte is enabled, and data can be written to the device. When LDQM or UDQM is HIGH, input data is masked and cannot be written to the device.
17	$\overline{RAS}$	Input Pin	$\overline{RAS}$, in conjunction with $\overline{CAS}$ and $\overline{WE}$, forms the device command. See the "Command Truth Table" item for details on device commands.
15	$\overline{WE}$	Input Pin	$\overline{WE}$, in conjunction with $\overline{RAS}$ and $\overline{CAS}$, forms the device command. See the "Command Truth Table" item for details on device commands.
7, 13, 38, 44	VDDQ	Power Supply Pin	VDDQ is the output buffer power supply.
1, 25	VDD	Power Supply Pin	VDD is the device internal power supply.
4, 10, 41, 47	GNDQ	Power Supply Pin	GNDQ is the output buffer ground.
26, 50	GND	Power Supply Pin	GND is the device internal ground.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters		Rating	Unit
$V_{DD\ MAX}$	Maximum Supply Voltage		–1.0 to +4.6	V
$V_{DDQ\ MAX}$	Maximum Supply Voltage for Output Buffer		–1.0 to +4.6	V
V_{IN}	Input Voltage		–1.0 to +4.6	V
V_{OUT}	Output Voltage		–1.0 to +4.6	V
$P_{D\ MAX}$	Allowable Power Dissipation		1	W
I_{CS}	Output Shorted Current		50	mA
T_{OPR}	Operating Temperature	Commerical	0 to +70	°C
		Industrial	-40 to +85	°C
		A1	-40 to +85	°C
		A2	-40 to +105	°C
T_{STG}	Storage Temperature		–55 to +150	°C

DC RECOMMENDED OPERATING CONDITION(2)

(At T_A = 0°C to +70°C for Commercial temperature, T_A = -40°C to +85°C for Industrial and A1 temperature, T_A = -40°C to +105°C for A2 temperature)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}, V_{DDQ}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage(3)	2.0	—	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage(4)	-0.3	—	+0.8	V

CAPACITANCE CHARACTERISTICS(1,2) (At T_A = 0 to +25°C, VDD = VDDQ = 3.3 ± 0.3V, f = 1 MHz)

Symbol	Parameter	Typ.	Max.	Unit
$C_{IN}1$	Input Capacitance: A0-A11	—	4	pF
$C_{IN}2$	Input Capacitance: (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, LDQM, UDQM)	—	4	pF
CI/O	Data Input/Output Capacitance: DQ0-DQ15	—	5	pF

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are referenced to GND.
3. V_{IH} (max) = V_{DDQ} + 1.2V with a pulse width ≤ 3 ns.
4. V_{IL} (min) = V_{DDQ} - 1.2V with a pulse width ≤ 3 ns.

DC ELECTRICAL CHARACTERISTICS (Recommended Operation Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition			Speed	Min.	Max.	Unit
I_{IL}	Input Leakage Current	0V ≤ V_{IN} ≤ VDD, with pins other than the tested pin at 0V				–5	5	µA
I_{OL}	Output Leakage Current	Output is disabled, 0V ≤ V_{OUT} ≤ VDD				–5	5	µA
V_{OH}	Output High Voltage Level	I_{OUT} = –2 mA				2.4	—	V
V_{OL}	Output Low Voltage Level	I_{OUT} = +2 mA				—	0.4	V
I_{CC1}	Operating Current(1,2)	One Bank Operation,	$\overline{CAS}$ latency = 3	Com.	-5	—	60	mA
		Burst Length=1		Com.	-6	—	55	
		t_{RC} ≥ t_{RC} (min.)		Com.	-7	—	50	
		I_{OUT} = 0mA		Ind, A1	-6	—	60	
				A2	-6	—	65	
				Ind, A1	-7	—	55	
				A2	-7	—	60	
I_{CC2P}	Precharge Standby Current	CKE ≤ V_{IL} (MAX)	t_{CK} = 15ns	Com	—	—	3	mA
				Ind, A1	—	—	4	
I_{CC2PS}	(In Power-Down Mode)		t_{CK} = ∞	Com	—	—	2	mA
				Ind, A1	—	—	3.5	
				A2	—	—	3.5	
I_{CC3N}	Active Standby Current	CKE ≥ V_{IH} (MIN)	t_{CK} = 15ns		—	—	40	mA
I_{CC3NS}	(In Non Power-Down Mode)		t_{CK} = ∞	Com	—	—	30	mA
				Ind, A1	—	—	30	
				A2	—	—	30	
I_{CC4}	Operating Current	t_{CK} = t_{CK} (MIN)	$\overline{CAS}$ latency = 3	Com	-5	—	80	mA
	(In Burst Mode)(1)	I_{OUT} = 0mA		Com	-6	—	70	
				Ind, A1	-6	—	80	
				A2	-6	—	90	
				Com	-7	—	60	
				Ind, A1	-7	—	70	
				A2	-7	—	80	
			$\overline{CAS}$ latency = 2	Com	-5	—	80	mA
				Com	-6	—	70	
				Ind, A1	-6	—	80	
				A2	-6	—	90	
				Com	-7	—	60	
				Ind, A1	-7	—	70	
				A2	-7	—	80	

Notes:

1. These are the values at the minimum cycle time. Since the currents are transient, these values decrease as the cycle time increases. Also note that a bypass capacitor of at least 0.01 µF should be inserted between V_{DD} and GND for each memory chip to suppress power supply voltage noise (voltage drops) due to these transient currents.
2. I_{CC1} and I_{CC4} depend on the output load. The maximum values for I_{CC1} and I_{CC4} are obtained with the output open state.

DC ELECTRICAL CHARACTERISTICS (Recommended Operation Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition			Speed	Min.	Max.	Unit
I_{CC5}	Auto-Refresh Current	$t_{RC} = t_{RC}$ (MIN)	$\overline{CAS}$ latency = 3	Com.	-5	—	50	mA
				Com.	-6	—	45	
				Ind, A1	-6	—	50	
				A2	-6	—	55	
				Com	-7	—	40	
				Ind, A1	-7	—	45	
				A2	-7	—	50	
			$\overline{CAS}$ latency = 2	Com	-5	—	50	mA
				Com	-6	—	45	
				Ind, A1	-6	—	50	
				A2	-6	—	55	
				Com	-7	—	40	
				Ind, A1	-7	—	45	
				A2	-7	—	50	
I_{CC6}	Self-Refresh Current	CKE ≤ 0.2V			—	—	2	mA

Notes:

1. These are the values at the minimum cycle time. Since the currents are transient, these values decrease as the cycle time increases. Also note that a bypass capacitor of at least 0.01 µF should be inserted between V_{DD} and GND for each memory chip to suppress power supply voltage noise (voltage drops) due to these transient currents.
2. I_{CC1} and I_{CC4} depend on the output load. The maximum values for I_{CC1} and I_{CC4} are obtained with the output open state.

AC CHARACTERISTICS[1,2,3]

Symbol	Parameter		-5 Min.	-5 Max.	-6 Min.	-6 Max.	-7 Min.	-7 Max.	Units
$t_{CK}3$	Clock Cycle Time	$\overline{CAS}$ Latency = 3	5	—	6	—	7	—	ns
$t_{CK}2$		$\overline{CAS}$ Latency = 2	8	—	8	—	8	—	ns
$t_{AC}3$	Access Time From CLK[4]	$\overline{CAS}$ Latency = 3	—	5	—	5.5	—	5.5	ns
$t_{AC}2$		$\overline{CAS}$ Latency = 2	—	6	—	6	—	6	ns
t_{CHI}	CLK HIGH Level Width		2	—	2.5	—	2.5	—	ns
t_{CL}	CLK LOW Level Width		2	—	2.5	—	2.5	—	ns
$t_{OH}3$	Output Data Hold Time	$\overline{CAS}$ Latency = 3	2	—	2.0	—	2.0	—	ns
$t_{OH}2$		$\overline{CAS}$ Latency = 2	2.5	—	2.5	—	2.5	—	ns
t_{LZ}	Output LOW Impedance Time		0	—	0	—	0	—	ns
$t_{HZ}3$	Output HIGH Impedance Time[5]	$\overline{CAS}$ Latency = 3	—	5	—	5.5	—	5.5	ns
$t_{HZ}2$		$\overline{CAS}$ Latency = 2	—	6	—	6	—	6	ns
t_{DS}	Input Data Setup Time		2	—	2	—	2	—	ns
t_{DH}	Input Data Hold Time		1	—	1	—	1	—	ns
t_{AS}	Address Setup Time		2	—	2	—	2	—	ns
t_{AH}	Address Hold Time		1	—	1	—	1	—	ns
t_{CKS}	CKE Setup Time		2	—	2	—	2	—	ns
t_{CKH}	CKE Hold Time		1	—	1	—	1	—	ns
t_{CKA}	CKE to CLK Recovery Delay Time		1CLK+3	—	1CLK+3	—	1CLK+3	—	ns
t_{CS}	Command Setup Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)		2	—	2	—	2	—	ns
t_{CH}	Command Hold Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)		1	—	1	—	1	—	ns
t_{RC}	Command Period (REF to REF / ACT to ACT)		50	—	54	—	63	—	ns
t_{RAS}	Command Period (ACT to PRE)		35	100,000	36	100,000	42	100,000	ns
t_{RP}	Command Period (PRE to ACT)		15	—	18	—	21	—	ns
t_{RCD}	Active Command To Read / Write Command Delay Time		15	—	18	—	21	—	ns
t_{RRD}	Command Period (ACT [0] to ACT[1])		10	—	12	—	14	—	ns
$t_{DPL}3$	Input Data To Precharge Command Delay time	$\overline{CAS}$ Latency = 3	2CLK	—	2CLK	—	2CLK	—	ns
$t_{DPL}2$		$\overline{CAS}$ Latency = 2	2CLK	—	2CLK	—	2CLK	—	ns
$t_{DAL}3$	Input Data To Active / Refresh Command Delay time (During Auto-Precharge)	$\overline{CAS}$ Latency = 3	2CLK+t_{RP}	—	2CLK+t_{RP}	—	2CLK+t_{RP}	—	ns
$t_{DAL}2$		$\overline{CAS}$ Latency = 2	2CLK+t_{RP}	—	2CLK+t_{RP}	—	2CLK+t_{RP}	—	ns
t_{XSR}	Exit Self-Refresh to Active Time		55	—	60	—	70	—	ns
t_T	Transition Time		0.3	1.2	0.3	1.2	0.3	1.2	ns
t_{REF}	Refresh Cycle Time (2048) for temperature $T_A \leq 85^oC$		—	32	—	32	—	32	ms
t_{REF}	Refresh Cycle Time (2048) for temperature $T_A > 85^oC$ (A2 only)[6]		—	—	—	—	—	16	ms

Notes:

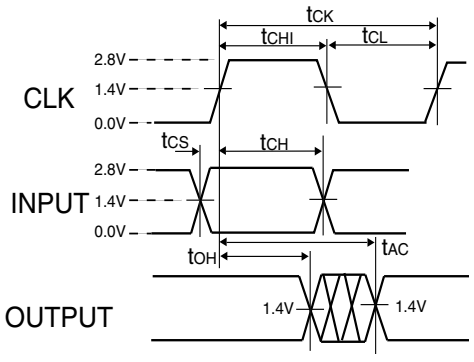
1. When power is first applied, memory operation should be started 100 µs after V_{DD} and V_{DDQ} reach their stipulated voltages. Also note that the power-on sequence must be executed before starting memory operation.
2. Measured with t_T = 1 ns. If clock rising time is longer than 1ns, (t_T/2 - 0.5)ns should be added to the parameter.
3. The reference level is 1.4 V when measuring input signal timing. Rise and fall times are measured between V_{IH} (min.) and V_{IL} (max.).
4. Access time is measured at 1.4V with the load shown in the figure below.
5. The time t_{HZ} (max.) is defined as the time required for the output voltage to transition by ± 200 mV from V_{OH} (min.) or V_{OL} (max.) when the output is in the high impedance state.
6. Self-Refresh Mode is not supported for A2 grade with $T_A > 85^oC$.

OPERATING FREQUENCY / LATENCY RELATIONSHIPS (CAS Latency = 3)

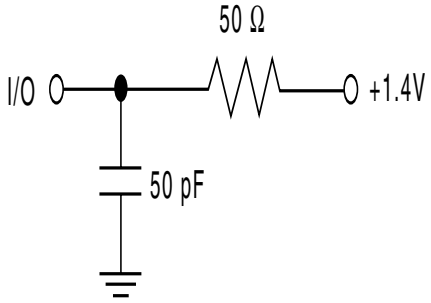
SYMBOL	PARAMETER	-5	-6	-7	UNITS
—	Clock Cycle Time	5	6	7	ns
—	Operating Frequency	200	166	143	MHz
t_{CAC}	$\overline{CAS}$ Latency	3	3	3	cycle
t_{RCD}	Active Command To Read/Write Command Delay Time	3	3	3	cycle
t_{RAC}	$\overline{RAS}$ Latency (t_{RCD} + t_{CAC})	6	6	6	cycle
t_{RC}	Command Period (REF to REF / ACT to ACT)	10	9	9	cycle
t_{RAS}	Command Period (ACT to PRE)	7	6	6	cycle
t_{RP}	Command Period (PRE to ACT)	3	3	3	cycle
t_{RRD}	Command Period (ACT[0] to ACT [1])	2	2	2	cycle
t_{CCD}	Column Command Delay Time (RE AD, READA, WRIT, WRITA)	1	1	1	cycle
t_{DPL}	Input Data To Precharge Command Delay Time	2	2	2	cycle
t_{DAL}	Input Data To Active/Refresh Command Delay Time (During Auto-Precharge)	5	5	5	cycle
t_{RBD}	Burst Stop Command To Output in HIGH-Z Delay Time (Read)	3	3	3	cycle
t_{WBD}	Burst Stop Command To Input in Invalid Delay Time (Write)	0	0	0	cycle
t_{RQL}	Precharge Command To Output in HIGH-Z Delay Time (Read)	3	3	3	cycle
t_{WDL}	Precharge Command To Input in Invalid Delay Time (Write)	0	0	0	cycle
t_{PQL}	Last Output To Auto-Precharge Start Time (Read)	–2	–2	–2	cycle
t_{QMD}	DQM To Output Delay Time (Read)	2	2	2	cycle
t_{DMD}	DQM To Input Delay Time (Write)	0	0	0	cycle
t_{MCD}	Mode Register Set To Command Delay Time	2	2	2	cycle

AC TEST CONDITIONS (Input/Output Reference Level: 1.4V)

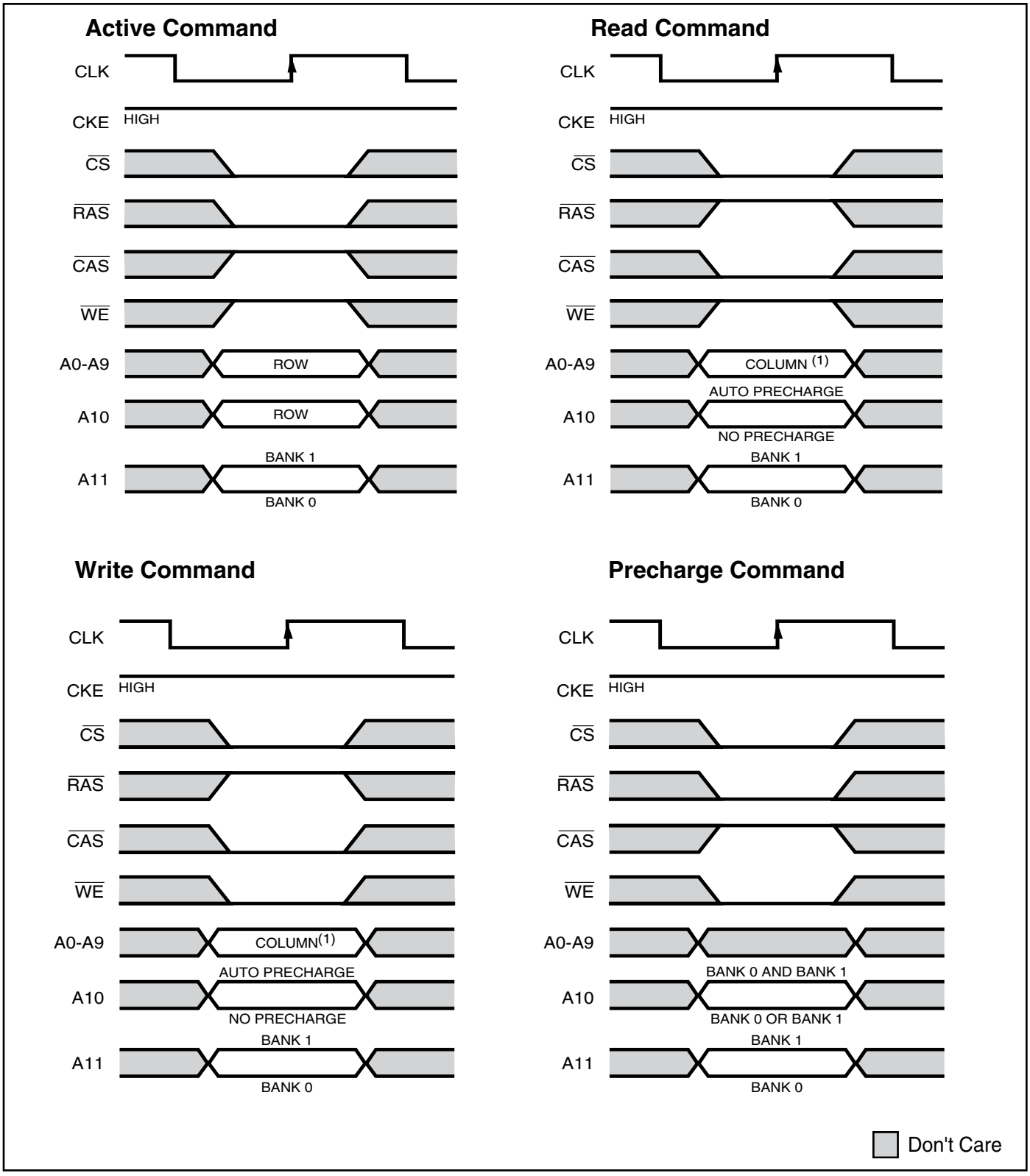
Input



Output Load



COMMANDS

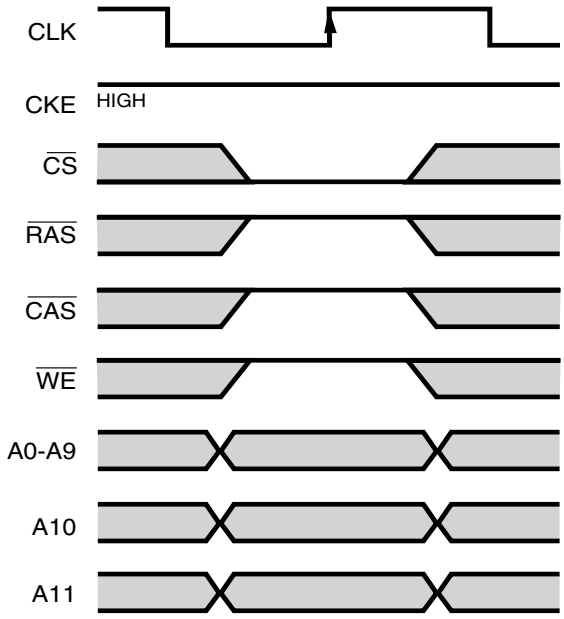


Notes:

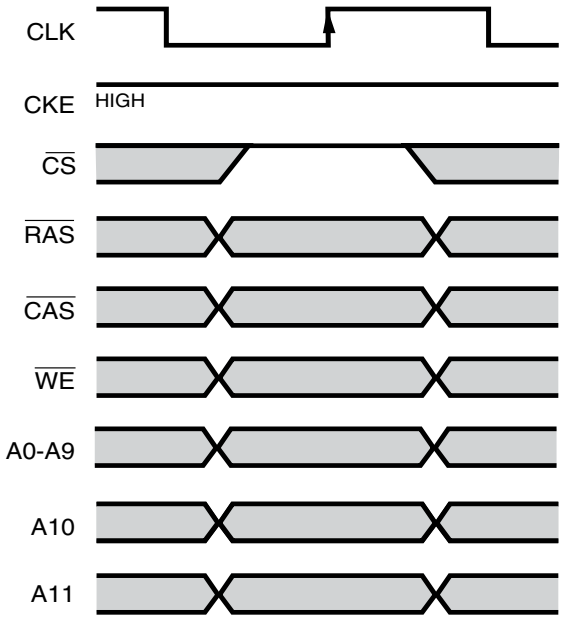
1. A8-A9 = Don't Care.

COMMANDS (cont.)

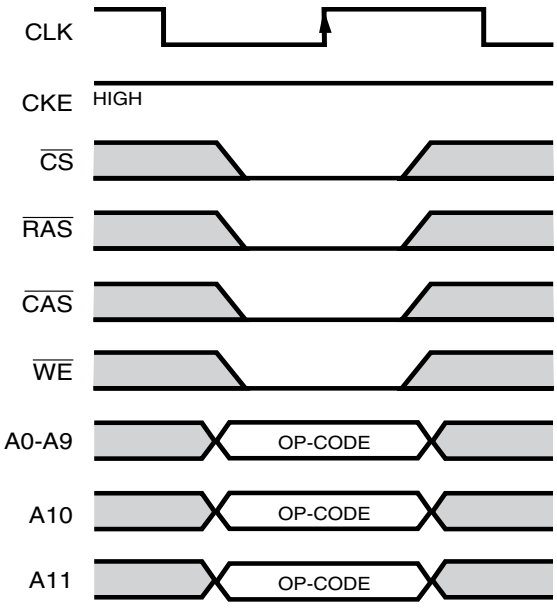
No-Operation Command



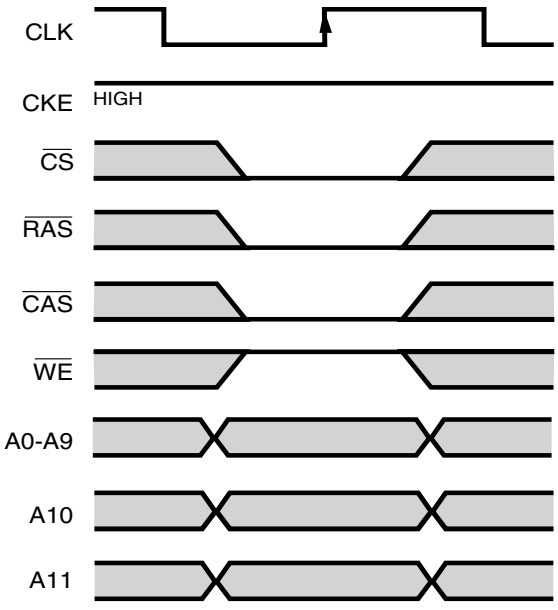
Device Deselect Command



Mode Register Set Command



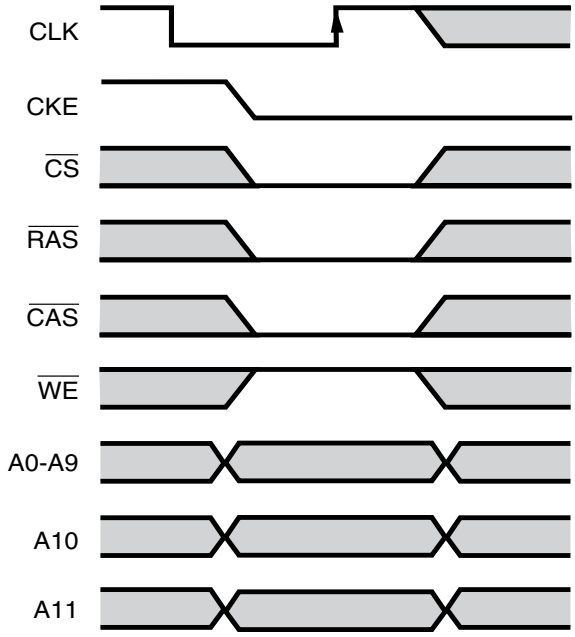
Auto-Refresh Command



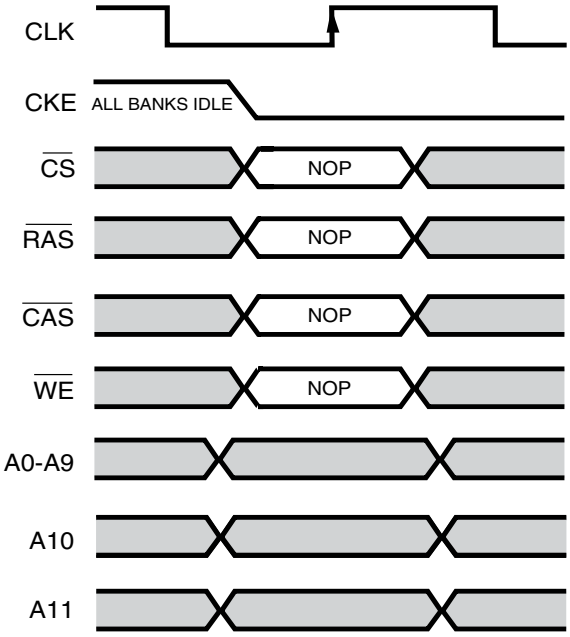
Don't Care

COMMANDS (cont.)

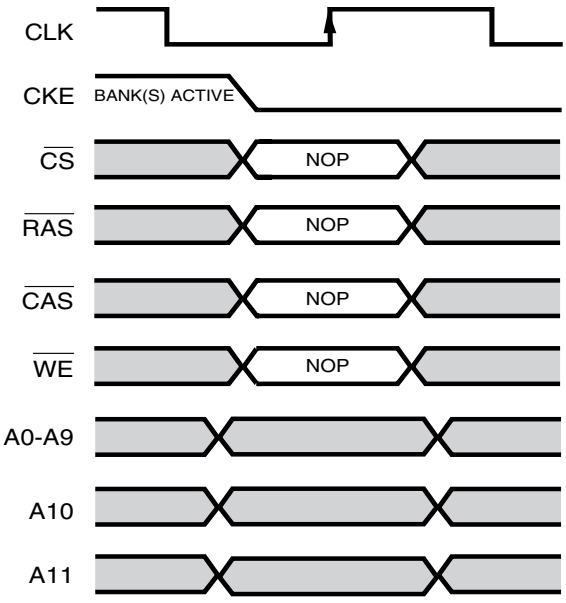
Self-Refresh Command



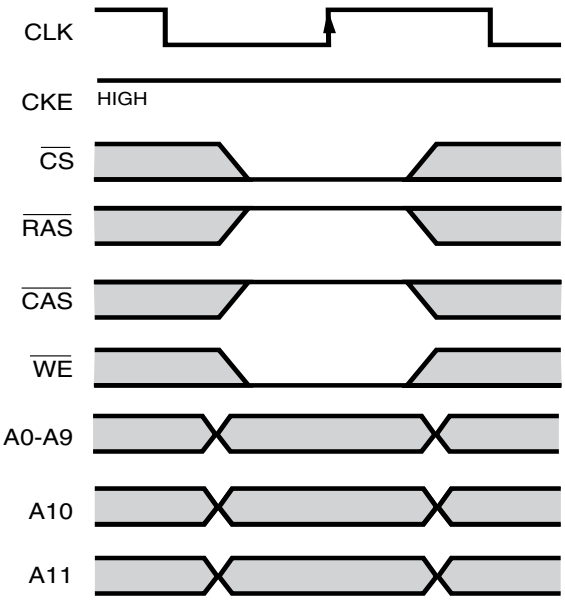
Power Down Command



Clock Suspend Command



Burst Stop Command



Mode Register Set Command

($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = LOW)

The IS42/4516100H product incorporates a register that defines the device operating mode. This command functions as a data input pin that loads this register from the pins A0 to A11. When power is first applied, the stipulated power-on sequence should be executed and then the IS42/4516100H should be initialized by executing a mode register set command.

Note that the mode register set command can be executed only when both banks are in the idle state (i.e. deactivated).

Another command cannot be executed after a mode register set command until after the passage of the period t_{MCD}, which is the period required for mode register set command execution.

Active Command

($\overline{CS}$, $\overline{RAS}$ = LOW, $\overline{CAS}$, $\overline{WE}$= HIGH)

The IS42/4516100H includes two banks of 2048 rows each. This command selects one of the two banks according to the A11 pin and activates the row selected by the pins A0 to A10.

This command corresponds to the fall of the $\overline{RAS}$ signal from HIGH to LOW in conventional DRAMs.

Precharge Command

($\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ = LOW, $\overline{CAS}$ = HIGH)

This command starts precharging the bank selected by pins A10 and A11. When A10 is HIGH, both banks are precharged at the same time. When A10 is LOW, the bank selected by A11 is precharged. After executing this command, the next command for the selected bank(s) is executed after passage of the period t_{RP}, which is the period required for bank precharging.

This command corresponds to the $\overline{RAS}$ signal from LOW to HIGH in conventional DRAMs

Read Command

($\overline{CS}$, $\overline{CAS}$ = LOW, $\overline{RAS}$, $\overline{WE}$ = HIGH)

This command selects the bank specified by the A11 pin and starts a burst read operation at the start address specified by pins A0 to A9. Data is output following $\overline{CAS}$ latency.

The selected bank must be activated before executing this command.

When the A10 pin is HIGH, this command functions as a read with auto-precharge command. After the burst read completes, the bank selected by pin A11 is precharged. When the A10 pin is LOW, the bank selected by the A11 pin remains in the activated state after the burst read completes.

Write Command

($\overline{CS}$, $\overline{CAS}$, $\overline{WE}$ = LOW, $\overline{RAS}$ = HIGH)

When burst write mode has been selected with the mode register set command, this command selects the bank specified by the A11 pin and starts a burst write operation at the start address specified by pins A0 to A9. This first data must be input to the DQ pins in the cycle in which this command.

The selected bank must be activated before executing this command.

When A10 pin is HIGH, this command functions as a write with auto-precharge command. After the burst write completes, the bank selected by pin A11 is precharged. When the A10 pin is low, the bank selected by the A11 pin remains in the activated state after the burst write completes.

After the input of the last burst write data, the application must wait for the write recovery period (t_{DPL}, t_{DAL}) to elapse according to $\overline{CAS}$ latency.

Auto-Refresh Command

($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ = LOW, $\overline{WE}$, CKE = HIGH)

This command executes the auto-refresh operation. The row address and bank to be refreshed are automatically generated during this operation.

Both banks must be placed in the idle state before executing this command.

The stipulated period (t_{RC}) is required for a single refresh operation, and no other commands can be executed during this period.

The device goes to the idle state after the internal refresh operation completes.

This command must be executed periodically according to t_{REF} specification (AC Characteristics).

This command corresponds to CBR auto-refresh in conventional DRAMs.

Self-Refresh Command

($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, CKE = LOW, $\overline{WE}$ = HIGH)

This command executes the self-refresh operation. The row address to be refreshed, the bank, and the refresh interval are generated automatically internally during this operation. The self-refresh operation is started by dropping the CKE pin from HIGH to LOW. The self-refresh operation continues as long as the CKE pin remains LOW and there is no need for external control of any other pins. The self-refresh operation is terminated by raising the CKE pin from LOW to HIGH. The next command cannot be executed until the device internal recovery period (t_{XSR}) has elapsed. After the self-refresh, since it is impossible to determine the address of the last row to be refreshed, an auto-refresh should immediately be performed for all addresses (4096 cycles).

Both banks must be placed in the idle state before executing this command.

Burst Stop Command

($\overline{CS}$, $\overline{WE}$, = LOW, $\overline{RAS}$, $\overline{CAS}$ = HIGH)

The command forcibly terminates burst read and write operations. When this command is executed during a burst read operation, data output stops after the $\overline{CAS}$ latency period has elapsed.

No Operation

($\overline{CS}$, = LOW, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = HIGH)

This command has no effect on the device.

Device Deselect Command

($\overline{CS}$ = HIGH)

This command does not select the device for an object of operation. In other words, it performs no operation with respect to the device.

Power-Down Command

(CKE = LOW)

When both banks are in the idle (inactive) state, or when at least one of the banks is not in the idle (inactive) state, this command can be used to suppress device power dissipation by reducing device internal operations to the absolute minimum. Power-down mode is started by dropping the CKE pin from HIGH to LOW. Power-down mode continues as long as the CKE pin is held low. All pins other than the CKE pin are invalid and none of the other commands can be executed in this mode. The power-down operation is terminated by raising the CKE pin from LOW to HIGH. The next command cannot be executed until the recovery period (t_{CKA}) has elapsed.

Since this command differs from the self-refresh command described above in that the refresh operation is not performed automatically internally, the refresh operation must be performed within the refresh period (t_{REF}). Thus the maximum time that power-down mode can be held is just under the refresh cycle time.

Clock Suspend

(CKE = LOW)

This command can be used to stop the device internal clock temporarily during a read or write cycle. Clock suspend mode is started by dropping the CKE pin from HIGH to LOW. Clock suspend mode continues as long as the CKE pin is held LOW. All input pins other than the CKE pin are invalid and none of the other commands can be executed in this mode. Also note that the device internal state is maintained. Clock suspend mode is terminated by raising the CKE pin from LOW to HIGH, at which point device operation restarts. The next command cannot be executed until the recovery period (t_{CKA}) has elapsed.

Since this command differs from the self-refresh command described above in that the refresh operation is not performed automatically internally, the refresh operation must be performed within the refresh period (t_{REF}). Thus the maximum time that clock suspend mode can be held is just under the refresh cycle time.

COMMAND TRUTH TABLE[1,2]

Symbol	Command	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A11	A10	A9-A0	I/On
MRS	Mode Register Set[3,4]	H	X	L	L	L	L	X	OP CODE			X
REF	Auto-Refresh[5]	H	H	L	L	L	H	X	X	X	X	HIGH-Z
SREF	Self-Refresh[5,6]	H	L	L	L	L	H	X	X	X	X	HIGH-Z
PRE	Precharge Selected Bank	H	X	L	L	H	L	X	BS	L	X	X
PALL	Precharge Both Banks	H	X	L	L	H	L	X	X	H	X	X
ACT	Bank Activate[7]	H	X	L	L	H	H	X	BS	Row	Row	X
WRIT	Write	H	X	L	H	L	L	X	BS	L	Column[18]	X
WRITA	Write With Auto-Precharge[8]	H	X	L	H	L	L	X	BS	H	Column[18]	X
READ	Read[8]	H	X	L	H	L	H	X	BS	L	Column[18]	X
READA	Read With Auto-Precharge[8]	H	X	L	H	L	H	X	BS	H	Column[18]	X
BST	Burst Stop[9]	H	X	L	H	H	L	X	X	X	X	X
NOP	No Operation	H	X	L	H	H	H	X	X	X	X	X
DESL	Device Deselect	H	X	H	X	X	X	X	X	X	X	X
SBY	Clock Suspend / Standby Mode	L	X	X	X	X	X	X	X	X	X	X
ENB	Data Write / Output Enable	H	X	X	X	X	X	L	X	X	X	Active
MASK	Data Mask / Output Disable	H	X	X	X	X	X	H	X	X	X	HIGH-Z

DQM TRUTH TABLE[1,2]

Symbol	Command	CKE n-1	CKE n	DQM UPPER	DQM LOWER
ENB	Data Write / Output Enable	H	X	L	L
MASK	Data Mask / Output Disable	H	X	H	H
ENBU	Upper Byte Data Write / Output Enable	H	X	L	X
ENBL	Lower Byte Data Write / Output Enable	H	X	X	L
MASKU	Upper Byte Data Mask / Output Disable	H	X	H	X
MASKL	Lower Byte Data Mask / Output Disable	H	X	X	H

CKE TRUTH TABLE[1,2]

Symbol	Command	Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A9-A0
SPND	Start Clock Suspend Mode	Active	H	L	X	X	X	X	X	X	X
—	Clock Suspend	Other States	L	L	X	X	X	X	X	X	X
—	Terminate Clock Suspend Mode	Clock Suspend	L	H	X	X	X	X	X	X	X
REF	Auto-Refresh	Idle	H	H	L	L	L	H	X	X	X
SELF	Start Self-Refresh Mode	Idle	H	L	L	L	L	H	X	X	X
SELFX	Terminate Self-Refresh Mode	Self-Refresh	L	H	L	H	H	H	X	X	X
			L	H	H	X	X	X	X	X	X
PDWN	Start Power-Down Mode	Idle	H	L	L	H	H	H	X	X	X
			H	L	H	X	X	X	X	X	X
—	Terminate Power-Down Mode	Power-Down	L	H	X	X	X	X	X	X	X

OPERATION COMMAND TABLE[1,2]

Current State	Command	Operation	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A9-A0
Idle	DESL	No Operation or Power-Down[12]	H	X	X	X	X	X	X
	NOP	No Operation or Power-Down[12]	L	H	H	H	X	X	X
	BST	No Operation or Power-Down	L	H	H	L	X	X	X
	READ / READA	Illegal	L	H	L	H	V	V	V[18]
	WRIT/WRITA	Illegal	L	H	L	L	V	V	V[18]
	ACT	Row Active	L	L	H	H	V	V	V[18]
	PRE/PALL	No Operation	L	L	H	L	V	V	X
	REF/SELF	Auto-Refresh or Self-Refresh[13]	L	L	L	H	X	X	X
	MRS	Mode Register Set	L	L	L	L	OP CODE		
Row Active	DESL	No Operation	H	X	X	X	X	X	X
	NOP	No Operation	L	H	H	H	X	X	X
	BST	No Operation	L	H	H	L	X	X	X
	READ/READA	Read Start[17]	L	H	L	H	V	V	V[18]
	WRIT/WRITA	Write Start[17]	L	H	L	L	V	V	V[18]
	ACT	Illegal[10]	L	L	H	H	V	V	V[18]
	PRE/PALL	Precharge[15]	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Read	DESL	Burst Read Continues, Row Active When Done	H	X	X	X	X	X	X
	NOP	Burst Read Continues, Row Active When Done	L	H	H	H	X	X	X
	BST	Burst Interrupted, Row Active After Interrupt	L	H	H	L	X	X	X
	READ/READA	Burst Interrupted, Read Restart After Interrupt[16]	L	H	L	H	V	V	V[18]
	WRIT/WRITA	Burst Interrupted Write Start After Interrupt[11,16]	L	H	L	L	V	V	V[18]
	ACT	Illegal[10]	L	L	H	H	V	V	V[18]
	PRE/PALL	Burst Read Interrupted, Precharge After Interrupt	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Write	DESL	Burst Write Continues, Write Recovery When Done	H	X	X	X	X	X	X
	NOP	Burst Write Continues, Write Recovery When Done	L	H	H	H	X	X	X
	BST	Burst Write Interrupted, Row Active After Interrupt	L	H	H	L	X	X	X
	READ/READA	Burst Write Interrupted, Read Start After Interrupt[11,16]	L	H	L	H	V	V	V[18]
	WRIT/WRITA	Burst Write Interrupted, Write Restart After Interrupt[16]	L	H	L	L	V	V	V[18]
	ACT	Illegal[10]	L	L	H	H	V	V	V[18]
	PRE/PALL	Burst Write Interrupted, Precharge After Interrupt	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Read With Auto-Precharge	DESL	Burst Read Continues, Precharge When Done	H	X	X	X	X	X	X
	NOP	Burst Read Continues, Precharge When Done	L	H	H	H	X	X	X
	BST	Illegal	L	H	H	L	X	X	X
	READ/READA	Illegal	L	H	L	H	V	V	V[18]
	WRIT/WRITA	Illegal	L	H	L	L	V	V	V[18]
	ACT	Illegal[10]	L	L	H	H	V	V	V[18]
	PRE/PALL	Illegal[10]	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		

OPERATION COMMAND TABLE(1,2)

Current State	Command	Operation	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A9-A0
Write With Auto-Precharge	DESL	Burst Write Continues, Write Recovery And Precharge When Done	H	X	X	X	X	X	X
	NOP	Burst Write Continues, Write Recovery And Precharge	L	H	H	H	X	X	X
	BST	Illegal	L	H	H	L	X	X	X
	READ/READA	Illegal	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Illegal	L	H	L	L	V	V	V(18)
	ACT	Illegal(10)	L	L	H	H	V	V	V(18)
	PRE/PALL	Illegal(10)	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OPCODE		
Row Precharge	DESL	No Operation, Idle State After t_{RP} Has Elapsed	H	X	X	X	X	X	X
	NOP	No Operation, Idle State After t_{RP} Has Elapsed	L	H	H	H	X	X	X
	BST	No Operation, Idle State After t_{RP} Has Elapsed	L	H	H	L	X	X	X
	READ/READA	Illegal(10)	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Illegal(10)	L	H	L	L	V	V	V(18)
	ACT	Illegal(10)	L	L	H	H	V	V	V(18)
	PRE/PALL	No Operation, Idle State After t_{RP} Has Elapsed(10)	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Immediately Following Row Active	DESL	No Operation, Row Active After t_{RCD} Has Elapsed	H	X	X	X	X	X	X
	NOP	No Operation, Row Active After t_{RCD} Has Elapsed	L	H	H	H	X	X	X
	BST	No Operation, Row Active After t_{RCD} Has Elapsed	L	H	H	L	X	X	X
	READ/READA	Illegal(10)	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Illegal(10)	L	H	L	L	V	V	V(18)
	ACT	Illegal(10,14)	L	L	H	H	V	V	V(18)
	PRE/PALL	Illegal(10)	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Write Recovery	DESL	No Operation, Row Active After t_{DPL} Has Elapsed	H	X	X	X	X	X	X
	NOP	No Operation, Row Active After t_{DPL} Has Elapsed	L	H	H	H	X	X	X
	BST	No Operation, Row Active After t_{DPL} Has Elapsed	L	H	H	L	X	X	X
	READ/READA	Read Start	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Write Restart	L	H	L	L	V	V	V(18)
	ACT	Illegal(10)	L	L	H	H	V	V	V(18)
	PRE/PALL	Illegal(10)	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		

OPERATION COMMAND TABLE(1,2)

Current State	Command	Operation	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A9-A0
Write Recovery	DESL	No Operation, Idle State After t_{DAL} Has Elapsed	H	X	X	X	X	X	X
With Auto-	NOP	No Operation, Idle State After t_{DAL} Has Elapsed	L	H	H	H	X	X	X
Precharge	BST	No Operation, Idle State After t_{DAL} Has Elapsed	L	H	H	L	X	X	X
	READ/READA	Illegal(10)	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Illegal(10)	L	H	L	L	V	V	V(18)
	ACT	Illegal(10)	L	L	H	H	V	V	V(18)
	PRE/PALL	Illegal(10)	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Refresh	DESL	No Operation, Idle State After t_{RP} Has Elapsed	H	X	X	X	X	X	X
	NOP	No Operation, Idle State After t_{RP} Has Elapsed	L	H	H	H	X	X	X
	BST	No Operation, Idle State After t_{RP} Has Elapsed	L	H	H	L	X	X	X
	READ/READA	Illegal	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Illegal	L	H	L	L	V	V	V(18)
	ACT	Illegal	L	L	H	H	V	V	V(18)
	PRE/PALL	Illegal	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		
Mode Register	DESL	No Operation, Idle State After t_{MCD} Has Elapsed	H	X	X	X	X	X	X
Set	NOP	No Operation, Idle State After t_{MCD} Has Elapsed	L	H	H	H	X	X	X
	BST	No Operation, Idle State After t_{MCD} Has Elapsed	L	H	H	L	X	X	X
	READ/READA	Illegal	L	H	L	H	V	V	V(18)
	WRIT/WRITA	Illegal	L	H	L	L	V	V	V(18)
	ACT	Illegal	L	L	H	H	V	V	V(18)
	PRE/PALL	Illegal	L	L	H	L	V	V	X
	REF/SELF	Illegal	L	L	L	H	X	X	X
	MRS	Illegal	L	L	L	L	OP CODE		

Notes:

1. H: HIGH level input, L: LOW level input, X: "Don't Care" input, V: Valid data input
2. All input signals are latched on the rising edge of the CLK signal.
3. Both banks must be placed in the inactive (idle) state in advance.
4. The state of the A0 to A11 pins is loaded into the mode register as an OP code.
5. The row address is generated automatically internally at this time. The DQ pin and the address pin data is ignored.
6. During a self-refresh operation, all pin data (states) other than CKE is ignored.
7. The selected bank must be placed in the inactive (idle) state in advance.
8. The selected bank must be placed in the active state in advance.
9. This command is valid only when the burst length set to full page.
10. This is possible depending on the state of the bank selected by the A11 pin.
11. Time to switch internal busses is required.
12. The DRAM can be switched to power-down mode by dropping the CKE pin LOW when both banks in the idle state. Input pins other than CKE are ignored at this time.
13. The DRAM can be switched to self-refresh mode by dropping the CKE pin LOW when both banks in the idle state. Input pins other than CKE are ignored at this time.
14. Possible if t_{RRD} is satisfied.
15. Illegal if t_{RAS} is not satisfied.
16. The conditions for burst interruption must be observed. Also note that the DRAM will enter the precharged state immediately after the burst operation completes if auto-precharge is selected.
17. Command input becomes possible after the period t_{RCD} has elapsed. Also note that the DRAM will enter the precharged state immediately after the burst operation completes if auto-precharge is selected.
18. A8,A9 = don't care.

CKE RELATED COMMAND TRUTH TABLE[1]

Current State	Operation	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A9-A0
Self-Refresh	Undefined	H	X	X	X	X	X	X	X	X
	Self-Refresh Recovery[2]	L	H	H	X	X	X	X	X	X
	Self-Refresh Recovery[2]	L	H	L	H	H	X	X	X	X
	Illegal[2]	L	H	L	H	L	X	X	X	X
	Illegal[2]	L	H	L	L	X	X	X	X	X
	Self-Refresh	L	L	X	X	X	X	X	X	X
Self-Refresh Recovery	Idle State After t_{RC} Has Elapsed	H	H	H	X	X	X	X	X	X
	Idle State After t_{RC} Has Elapsed	H	H	L	H	H	X	X	X	X
	Illegal	H	H	L	H	L	X	X	X	X
	Illegal	H	H	L	L	X	X	X	X	X
	Power-Down on the Next Cycle	H	L	H	X	X	X	X	X	X
	Power-Down on the Next Cycle	H	L	L	H	H	X	X	X	X
	Illegal	H	L	L	H	L	X	X	X	X
	Illegal	H	L	L	L	X	X	X	X	X
	Clock Suspend Termination on the Next Cycle [2]	L	H	X	X	X	X	X	X	X
	Clock Suspend	L	L	X	X	X	X	X	X	X
Power-Down	Undefined	H	X	X	X	X	X	X	X	X
	Power-Down Mode Termination, Idle After That Termination[2]	L	H	X	X	X	X	X	X	X
	Power-Down Mode	L	L	X	X	X	X	X	X	X
Both Banks Idle	No Operation	H	H	H	X	X	X	X	X	X
	See the Operation Command Table	H	H	L	H	X	X	X	X	X
	Bank Active Or Precharge	H	H	L	L	H	X	X	X	X
	Auto-Refresh	H	H	L	L	L	H	X	X	X
	Mode Register Set	H	H	L	L	L	L	OP CODE		
	See the Operation Command Table	H	L	H	X	X	X	X	X	X
	See the Operation Command Table	H	L	L	H	X	X	X	X	X
	See the Operation Command Table	H	L	L	L	H	X	X	X	X
	Self-Refresh[3]	H	L	L	L	L	H	X	X	X
	See the Operation Command Table	H	L	L	L	L	L	OP CODE		
	Power-Down Mode[3]	L	X	X	X	X	X	X	X	X
Other States	See the Operation Command Table	H	H	X	X	X	X	X	X	X
	Clock Suspend on the Next Cycle[4]	H	L	X	X	X	X	X	X	X
	Clock Suspend Termination on the Next Cycle	L	H	X	X	X	X	X	X	X
	Clock Suspend Termination on the Next Cycle	L	L	X	X	X	X	X	X	X

Notes:

1. H: HIGH level input, L: LOW level input, X: "Don't Care" input
2. The CLK pin and the other input are reactivated asynchronously by the transition of the CKE level from LOW to HIGH. The minimum setup time (t_{CKA}) required before all commands other than mode termination must be satisfied.
3. Both banks must be set to the inactive (idle) state in advance to switch to power-down mode or self-refresh mode.
4. The input must be command defined in the operation command table.

TWO BANKS OPERATION COMMAND TRUTH TABLE(1,2)

Operation	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A9-A0	Previous State BANK 0	Previous State BANK 1	Next State BANK 0	Next State BANK 1
DESL	H	X	X	X	X	X	X	Any	Any	Any	Any
NOP	L	H	H	H	X	X	X	Any	Any	Any	Any
BST	L	H	H	L	X	X	X	R/W/A	I/A	A	I/A
								I	I/A	I	I/A
								I/A	R/W/A	I/A	A
								I/A	I	I/A	I
READ/READA	L	H	L	H	H	H	CA(3)	I/A	R/W/A	I/A	RP
					H	H	CA(3)	R/W	A	A	RP
					H	L	CA(3)	I/A	R/W/A	I/A	R
					H	L	CA(3)	R/W	A	A	R
					L	H	CA(3)	R/W/A	I/A	RP	I/A
					L	H	CA(3)	A	R/W	RP	A
					L	L	CA(3)	R/W/A	I/A	R	I/A
					L	L	CA(3)	A	R/W	R	A
WRIT/WRITA	L	H	L	L	H	H	CA(3)	I/A	R/W/A	I/A	WP
					H	H	CA(3)	R/W	A	A	WP
					H	L	CA(3)	I/A	R/W/A	I/A	W
					H	L	CA(3)	R/W	A	A	W
					L	H	CA(3)	R/W/A	I/A	WP	I/A
					L	H	CA(3)	A	R/W	WP	A
					L	L	CA(3)	R/W/A	I/A	W	I/A
					L	L	CA(3)	A	R/W	W	A
ACT	L	L	H	H	H	RA	RA	Any	I	Any	A
					L	RA	RA	I	Any	A	Any
PRE/PALL	L	L	H	L	X	H	X	R/W/A/I	I/A	I	I
					X	H	X	I/A	R/W/A/I	I	I
					H	L	X	I/A	R/W/A/I	I/A	I
					H	L	X	R/W/A/I	I/A	R/W/A/I	I
					L	L	X	R/W/A/I	I/A	I	I/A
					L	L	X	I/A	R/W/A/I	I	R/W/A/I
REF	L	L	L	H	X	X	X	I	I	I	I
MRS	L	L	L	L	OPCODE			I	I	I	I

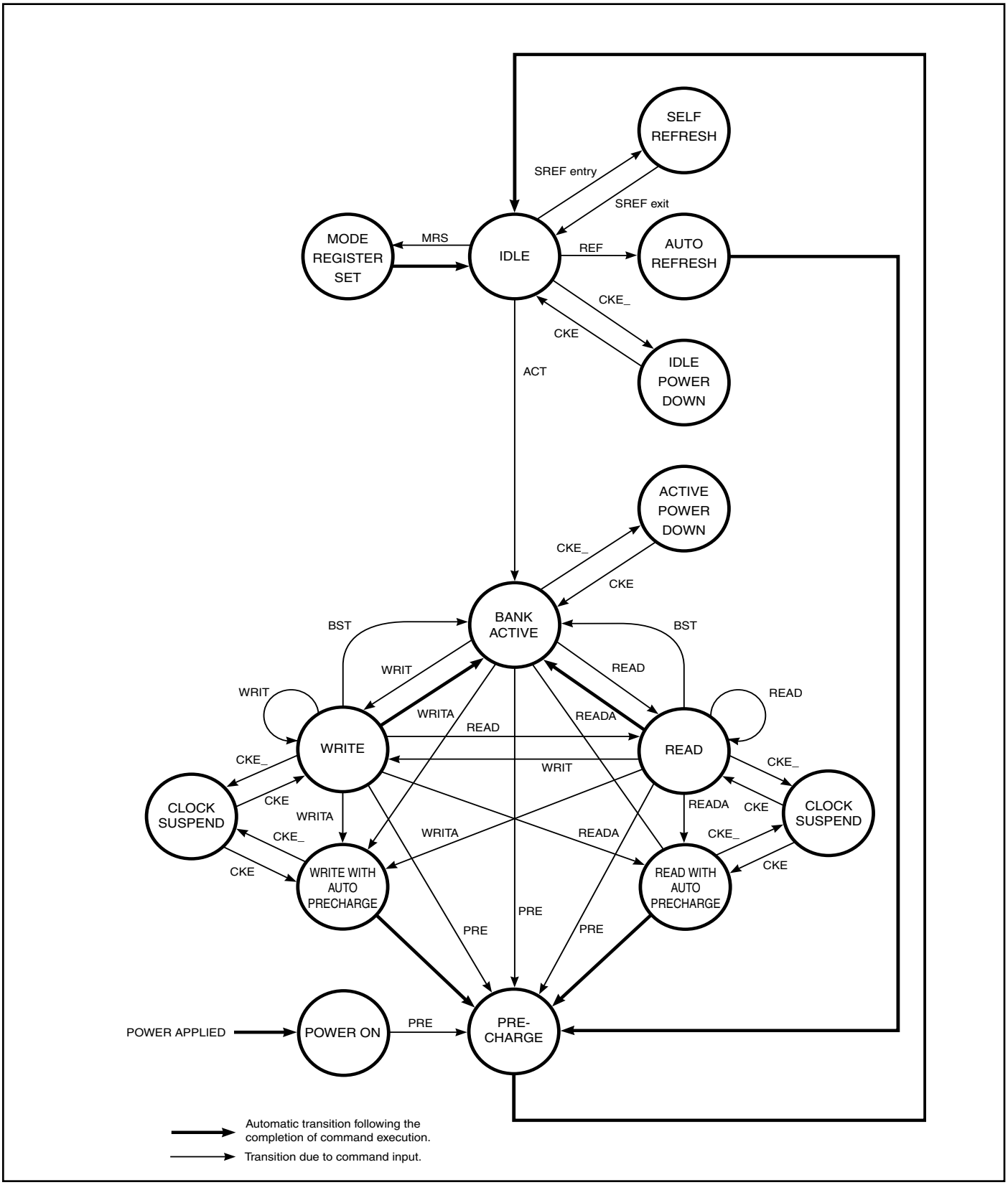
Notes:

1. H: HIGH level input, L: LOW level input, X: HIGH or LOW level input, RA: Row Address, CA: Column Address
2. The device state symbols are interpreted as follows:

I	Idle (inactive state)
A	Row Active State
R	Read
W	Write
RP	Read With Auto-Precharge
WP	Write With Auto-Precharge
Any	Any State

3. CA: A8,A9 = don't care.

SIMPLIFIED STATE TRANSITION DIAGRAM (One Bank Operation)



Device Initialization At Power-On

(Power-On Sequence)

As is the case with conventional DRAMs, the DRAM product must be initialized by executing a stipulated power-on sequence after power is applied.

After power is applied and VDD and VDDQ reach their stipulated voltages, set and hold the CKE and DQM pins HIGH for 100 µs. Then, execute the precharge command to precharge both bank. Next, execute the auto-refresh command twice or more and define the device operation mode by executing a mode register set command.

The mode register set command can be also set before auto-refresh command.

Mode Register Settings

The mode register set command sets the mode register. When this command is executed, pins A0 to A9, A10, and A11 function as data input pins for setting the register, and this data becomes the device internal OP code. This OP code has four fields as listed in the table below.

Input Pin	Field
A11, A10, A9, A8, A7	Mode Options
A6, A5, A4	$\overline{\text{CAS}}$ Latency
A3	Burst Type
A2, A1, A0	Burst Length

Note that the mode register set command can be executed only when both banks are in the idle (inactive) state. If the Mode Register Set command is executed, the next command (except NOP or Deselect) cannot be executed until at least two clock cycles later, in order to avoid violating tMCD.

$\overline{\text{CAS}}$ Latency

During a read operation, the between the execution of the read command and data output is stipulated as the $\overline{\text{CAS}}$ latency. This period can be set using the mode register set command. The optimal $\overline{\text{CAS}}$ latency is determined by the clock frequency and device speed grade. See the "Operating Frequency / Latency Relationships" item for details on the relationship between the clock frequency and the $\overline{\text{CAS}}$ latency. See the table on the next page for details on setting the mode register.

Burst Length

When writing or reading, data can be input or output data continuously. In these operations, an address is input only once and that address is taken as the starting address internally by the device. The device then automatically generates the following address. The burst length field in the mode register stipulates the number of data items input or output in sequence. In the DRAM product, a burst length of 1, 2, 4, 8, or full page can be specified. See the table on the next page for details on setting the mode register.

Burst Type

The burst data order during a read or write operation is stipulated by the burst type, which can be set by the mode register set command. The DRAM product supports sequential mode and interleaved mode burst type settings. See the table on the next page for details on setting the mode register. See the "Burst Length and Column Address Sequence" item for details on DQ data orders in these modes.

Write Mode

Burst write or single write mode is selected by the OP code (A11, A10, A9) of the mode register.

A burst write operation is enabled by setting the OP code (A11, A10, A9) to (0,0,0). A burst write starts on the same cycle as a write command set. The write start address is specified by the column address and bank select address at the write command set cycle.

A single write operation is enabled by setting OP code (A11, A10, A9) to (0, 0,1). In a single write operation, data is only written to the column address and bank select address specified by the write command set cycle without regard to the bust length setting.

MODE REGISTER

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
WRITE MODE				LT MODE			BT		BL		

Address Bus (Ax)
Mode Register (Mx)

	M2	M1	M0	Sequential	Interleaved
Burst Length	0	0	0	1	1
	0	0	1	2	2
	0	1	0	4	4
	0	1	1	8	8
	1	0	0	Reserved	Reserved
	1	0	1	Reserved	Reserved
	1	1	0	Reserved	Reserved
	1	1	1	Full Page	Reserved

	M3	Type
Burst Type	0	Sequential
	1	Interleaved

	M6	M5	M4	CAS **Latency**
Latency Mode	0	0	0	Reserved
	0	0	1	Reserved
	0	1	0	2
	0	1	1	3
	1	0	0	Reserved
	1	0	1	Reserved
	1	1	0	Reserved
	1	1	1	Reserved

M11	M10	M9	M8	M7	Write Mode
0	0	1	0	0	Burst Read & Single Write
0	0	0	0	0	Burst Read & Burst Write

Note: Other values for these bits are reserved.

BURST LENGTH AND COLUMN ADDRESS SEQUENCE

	Column Address			Address Sequence	
Burst Length	**A2**	**A1**	**A0**	**Sequential**	**Interleaved**
2	X	X	0	0-1	0-1
	X	X	1	1-0	1-0
4	X	0	0	0-1-2-3	0-1-2-3
	X	0	1	1-2-3-0	1-0-3-2
	X	1	0	2-3-0-1	2-3-0-1
	X	1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (256)	n	n	n	Cn, Cn+1, Cn+2 Cn+3, Cn+4..... ...Cn-1(Cn+255), Cn(Cn+256).....	None

Notes:
1. The burst length in full page mode is 256.

BANK SELECT AND PRECHARGE ADDRESS ALLOCATION

Row	X0	—	Row Address
	X1	—	Row Address
	X2	—	Row Address
	X3	—	Row Address
	X4	—	Row Address
	X5	—	Row Address
	X6	—	Row Address
	X7	—	Row Address
	X8	—	Row Address
	X9	—	Row Address
	X10	—	Row Address (Active Command)
		0	Precharge of the Selected Bank (Precharge Command)
		1	Precharge of Both Banks (Precharge Command)
	X11	0	Bank 0 Selected (Precharge and Active Commands)
		1	Bank 1 Selected (Precharge and Active Commands)
Column	Y0	—	Column Address
	Y1	—	Column Address
	Y2	—	Column Address
	Y3	—	Column Address
	Y4	—	Column Address
	Y5	—	Column Address
	Y6	—	Column Address
	Y7	—	Column Address
	Y8	—	Don't Care
	Y9	—	Don't Care
	Y10	0	Auto-Precharge - Disabled
		1	Auto-Precharge - Enables
	Y11	0	Bank 0 Selected (Read and Write Commands)
		1	Bank 1 Selected (Read and Write Commands)

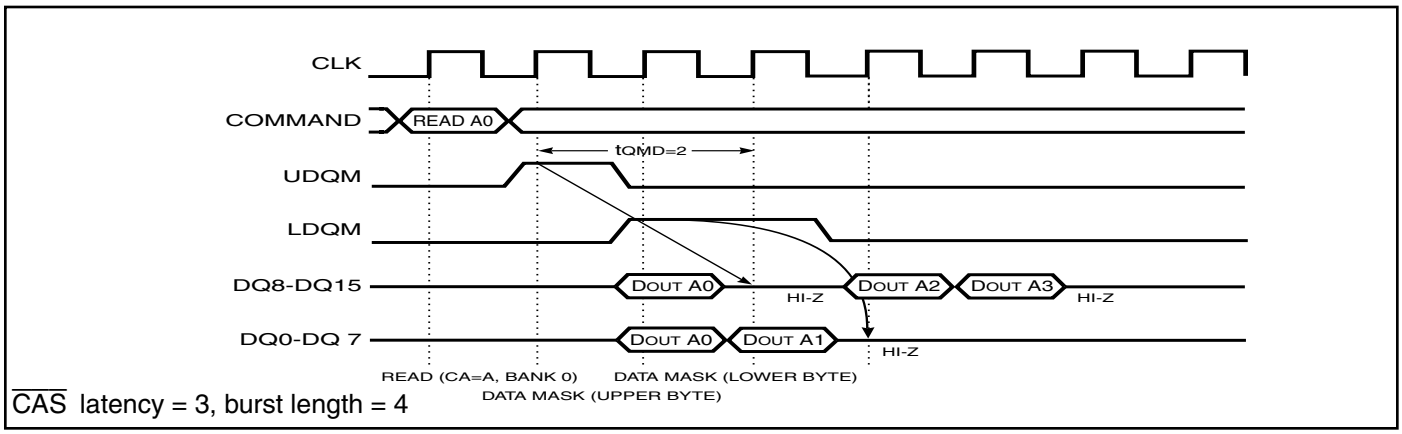
Burst Read

The read cycle is started by executing the read command. The address provided during read command execution is used as the starting address. First, the data corresponding to this address is output in synchronization with the clock signal after the $\overline{CAS}$ latency period. Next, data corresponding to an address generated automatically by the device is output in synchronization with the clock signal.

The output buffers go to the LOW impedance state $\overline{CAS}$ latency minus one cycle after the read command, and go to the HIGH impedance state automatically after the last data is output. However, the case where the burst length is a full page is an exception. In this case the output buffers must be set to the high impedance state by executing a burst stop command.

Note that upper byte and lower byte output data can be masked independently under control of the signals applied to the U/LDQM pins. The delay period (t_{QMD}) is fixed at two, regardless of the $\overline{CAS}$ latency setting, when this function is used.

The selected bank must be set to the active state before executing this command.



$\overline{CAS}$ latency = 3, burst length = 4

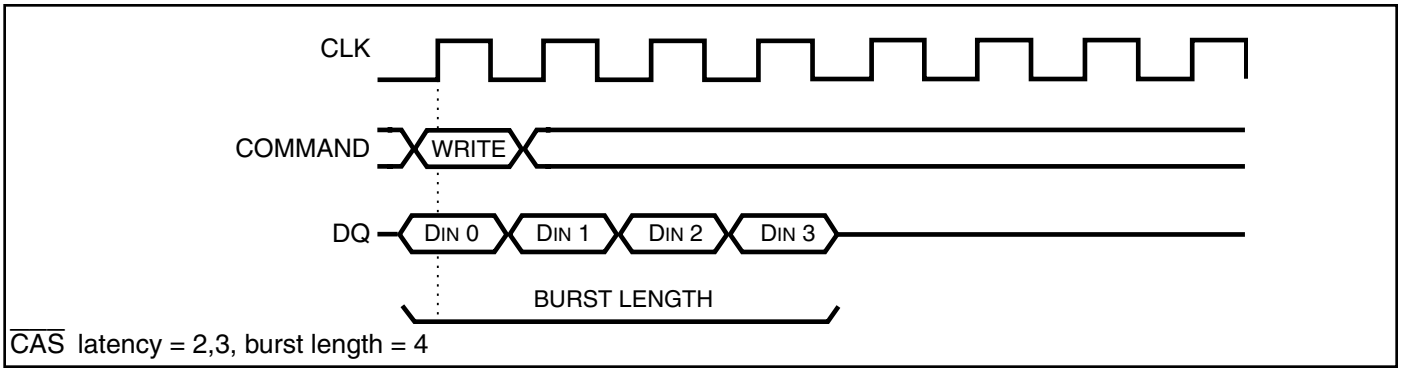
Burst Write

The write cycle is started by executing the command. The address provided during write command execution is used as the starting address, and at the same time, data for this address is input in synchronization with the clock signal.

Next, data is input in other in synchronization with the clock signal. During this operation, data is written to address generated automatically by the device. This cycle terminates automatically after a number of clock cycles determined by the stipulated burst length. However, the case where the burst length is a full page is an exception. In this case the write cycle must be terminated by executing a burst stop command. The latency for DQ pin data input is zero, regardless of the $\overline{CAS}$ latency setting. However, a wait period (write recovery: t_{DPL}) after the last data input is required for the device to complete the write operation.

Note that the upper byte and lower byte input data can be masked independently under control of the signals applied to the U/LDQM pins. The delay period (t_{DMD}) is fixed at zero, regardless of the $\overline{CAS}$ latency setting, when this function is used.

The selected bank must be set to the active state before executing this command.



$\overline{CAS}$ latency = 2,3, burst length = 4

Read With Auto-Precharge

The read with auto-precharge command first executes a burst read operation and then puts the selected bank in the precharged state automatically. After the precharge completes, the bank goes to the idle state. Thus this command performs a read command and a precharge command in a single operation.

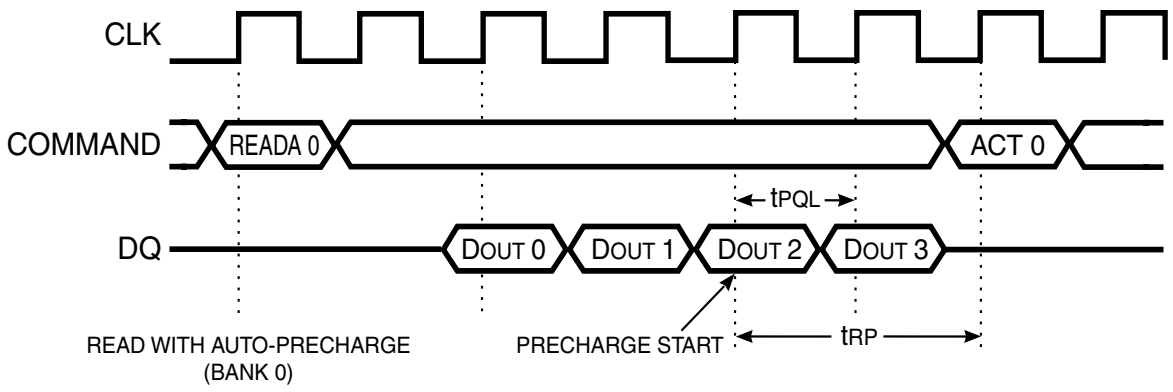
During this operation, the delay period (t_{PQL}) between the last burst data output and the start of the precharge operation differs depending on the $\overline{CAS}$ latency setting.

When the $\overline{CAS}$ latency setting is two, the precharge operation starts on one clock cycle before the last burst data is output (t_{PQL} = –1). When the $\overline{CAS}$ latency setting is three, the precharge operation starts on two clock cycles before the last burst data is output (t_{PQL} = –2). Therefore, the selected bank can be made active after a delay of t_{RP} from the start position of this precharge operation.

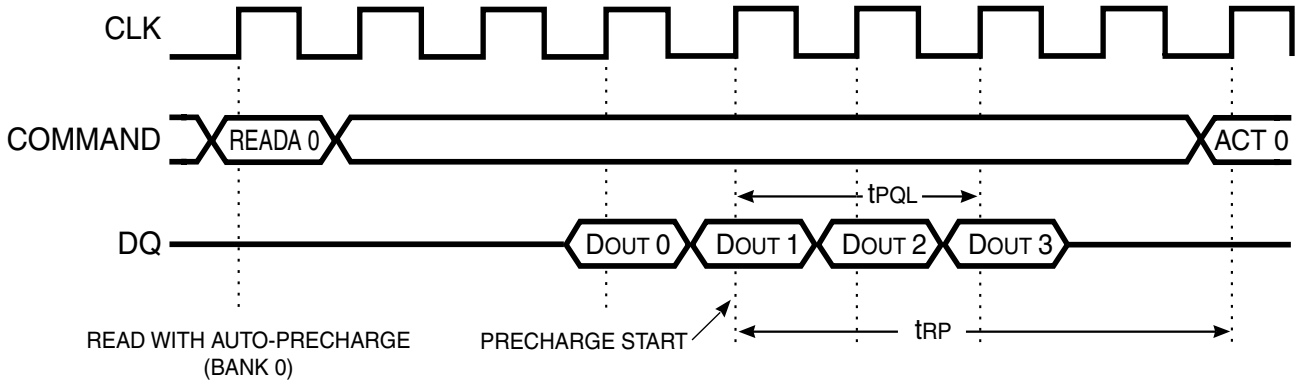
The selected bank must be set to the active state before executing this command.

The auto-precharge function is invalid if the burst length is set to full page.

$\overline{CAS}$ **Latency**	**3**	**2**
t_{PQL}	–2	–1



$\overline{CAS}$ latency = 2, burstlength = 4



$\overline{CAS}$ latency = 3, burstlength = 4

Write With Auto-Precharge

The write with auto-precharge command first executes a burst write operation and then puts the selected bank in the precharged state automatically. After the precharge completes the bank goes to the idle state. Thus this command performs a write command and a precharge command in a single operation.

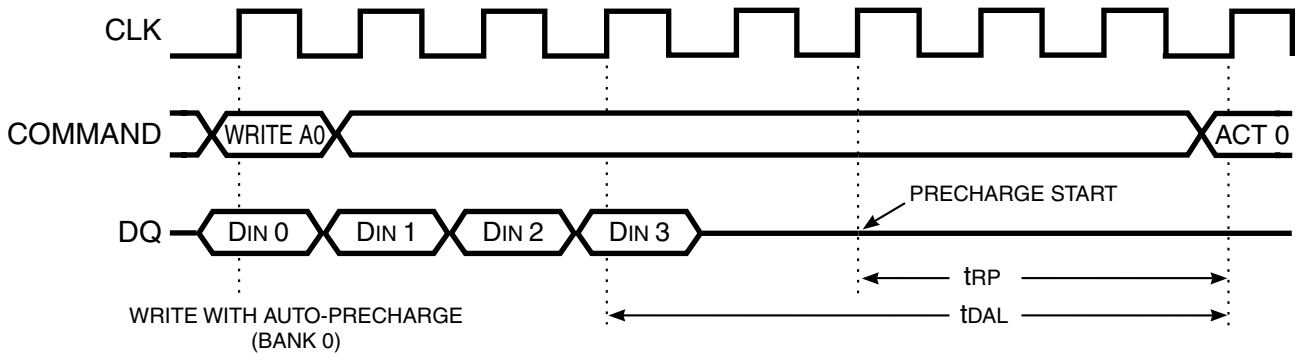
During this operation, the delay period (t_{DAL}) between the last burst data input and the completion of the precharge operation differs depending on the $\overline{CAS}$ latency setting. The delay (t_{DAL}) is t_{RP} plus two CLK periods. That is, the precharge operation starts two clock periods after the last burst data input.

Therefore, the selected bank can be made active after a delay of t_{DAL}.

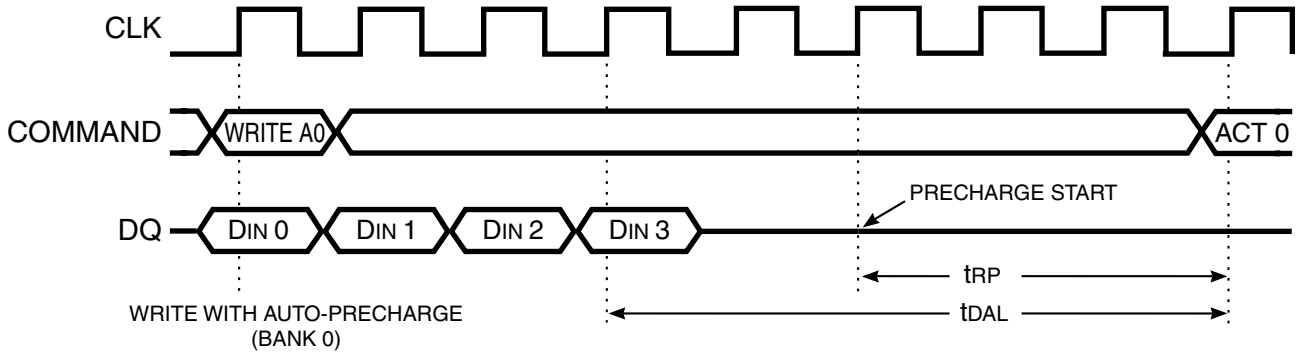
The selected bank must be set to the active state before executing this command.

The auto-precharge function is invalid if the burst length is set to full page.

$\overline{CAS}$ **Latency**	**3**	**2**
t_{DAL}	2CLK +t_{RP}	2CLK +t_{RP}



$\overline{CAS}$ latency = 2, burstlength = 4



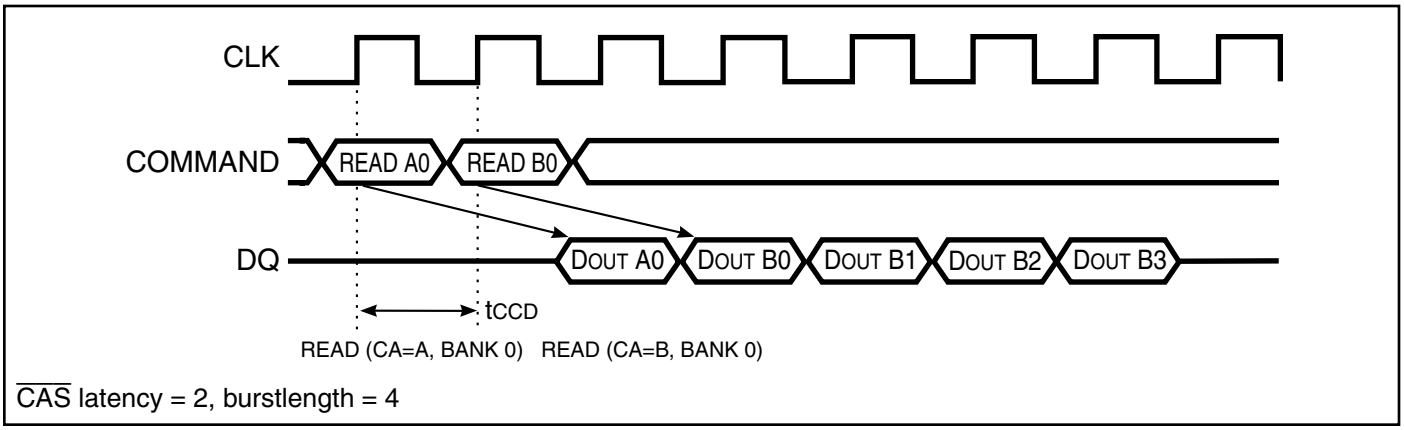
$\overline{CAS}$ latency = 3, burstlength = 4

Interval Between Read Command

A new command can be executed while a read cycle is in progress, i.e., before that cycle completes. When the second read command is executed, after the $\overline{CAS}$ latency has elapsed, data corresponding to the new read command is output in place of the data due to the previous read command.

The interval between two read command (tCCD) must be at least one clock cycle.

The selected bank must be set to the active state before executing this command.



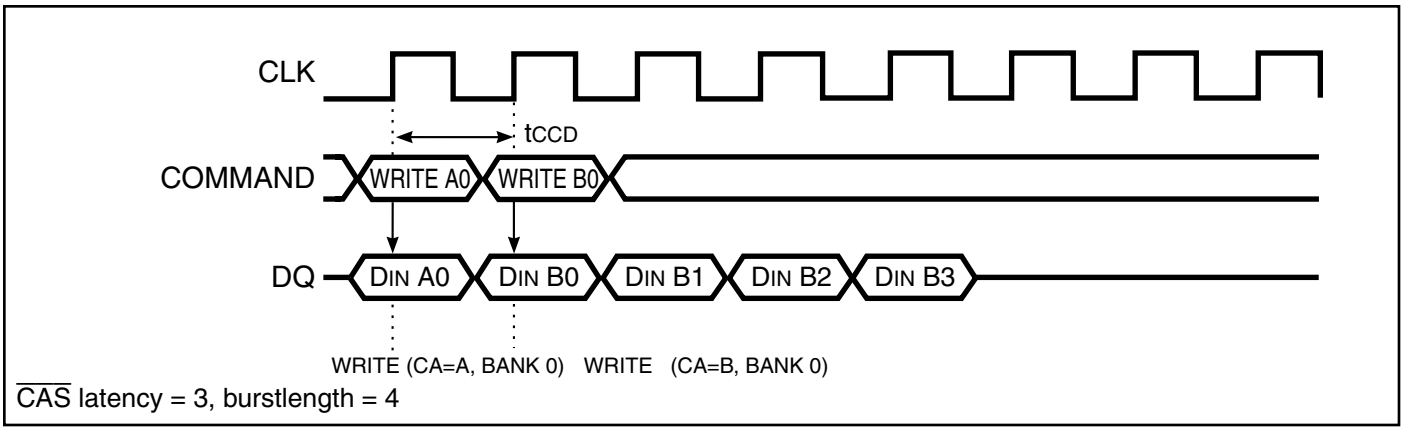
$\overline{CAS}$ latency = 2, burstlength = 4

Interval Between Write Command

A new command can be executed while a write cycle is in progress, i.e., before that cycle completes. At the point the second write command is executed, data corresponding to the new write command can be input in place of the data for the previous write command.

The interval between two write commands (tCCD) must be at least one clock cycle.

The selected bank must be set to the active state before executing this command.



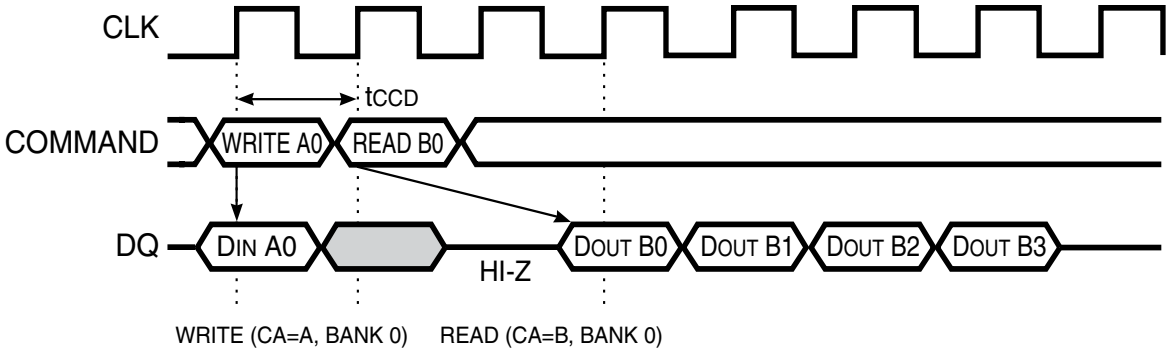
$\overline{CAS}$ latency = 3, burstlength = 4

Interval Between Write and Read Commands

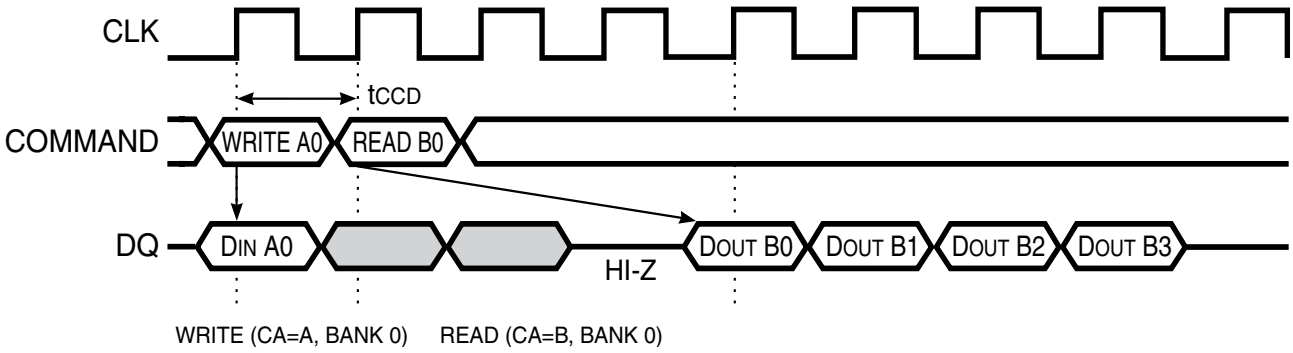
A new read command can be executed while a write cycle is in progress, i.e., before that cycle completes. Data corresponding to the new read command is output after the $\overline{CAS}$ latency has elapsed from the point the new read command was executed. The I/On pins must be placed in the HIGH impedance state at least one cycle before data is output during this operation.

The interval (t_{CCD}) between command must be at least one clock cycle.

The selected bank must be set to the active state before executing this command.



$\overline{CAS}$ latency = 2, burstlength = 4

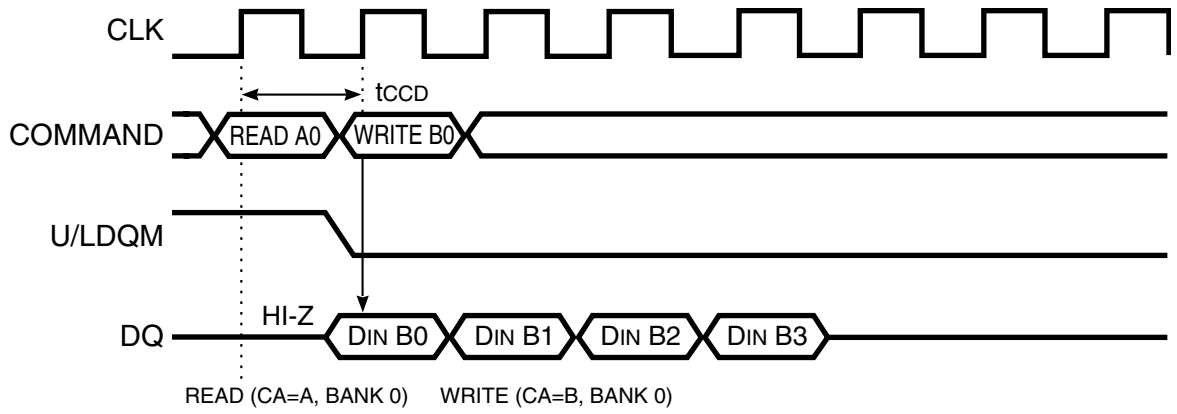


$\overline{CAS}$ latency = 3, burstlength = 4

Interval Between Read and Write Commands

A read command can be interrupted and a new write command executed while the read cycle is in progress, i.e., before that cycle completes. Data corresponding to the new write command can be input at the point new write command is executed. To prevent collision between input and output data at the DQn pins during this operation, the output data must be masked using the U/LDQM pins. The interval (t_{CCD}) between these commands must be at least one clock cycle.

The selected bank must be set to the active state before executing this command.



$\overline{CAS}$ latency = 2, 3, burstlength = 4

Precharge

The precharge command sets the bank selected by pin A11 to the precharged state. This command can be executed at a time t_{RAS} following the execution of an active command to the same bank. The selected bank goes to the idle state at a time t_{RP} following the execution of the precharge command, and an active command can be executed again for that bank.

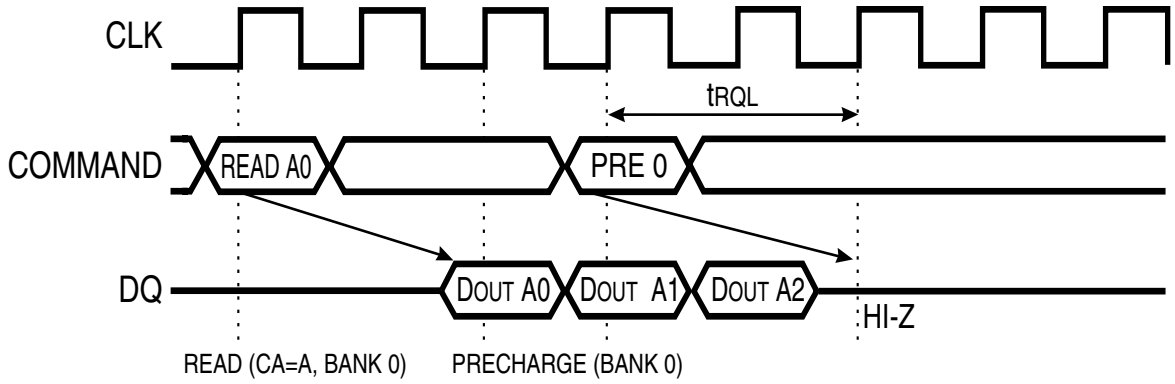
If pin A10 is low when this command is executed, the bank selected by pin A11 will be precharged, and if pin A10 is HIGH, both banks will be precharged at the same time. This input to pin A11 is ignored in the latter case.

Read Cycle Interruption

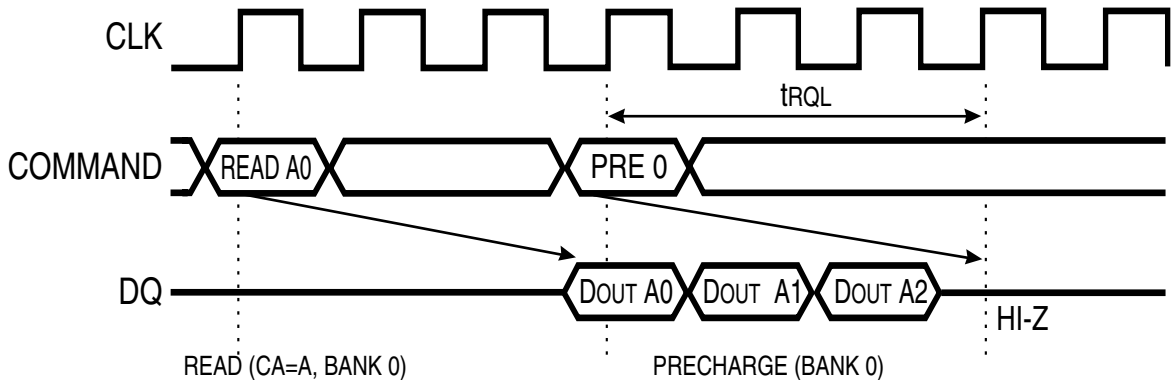
Using the Precharge Command

A read cycle can be interrupted by the execution of the precharge command before that cycle completes. The delay time (t_{RQL}) from the execution of the precharge command to the completion of the burst output is the clock cycle of $\overline{CAS}$ latency.

$\overline{CAS}$ **Latency**	**3**	**2**
t_{RQL}	3	2



$\overline{CAS}$ latency = 2, burstlength = 4



$\overline{CAS}$ latency = 3, burstlength = 4

Write Cycle Interruption Using the Precharge Command

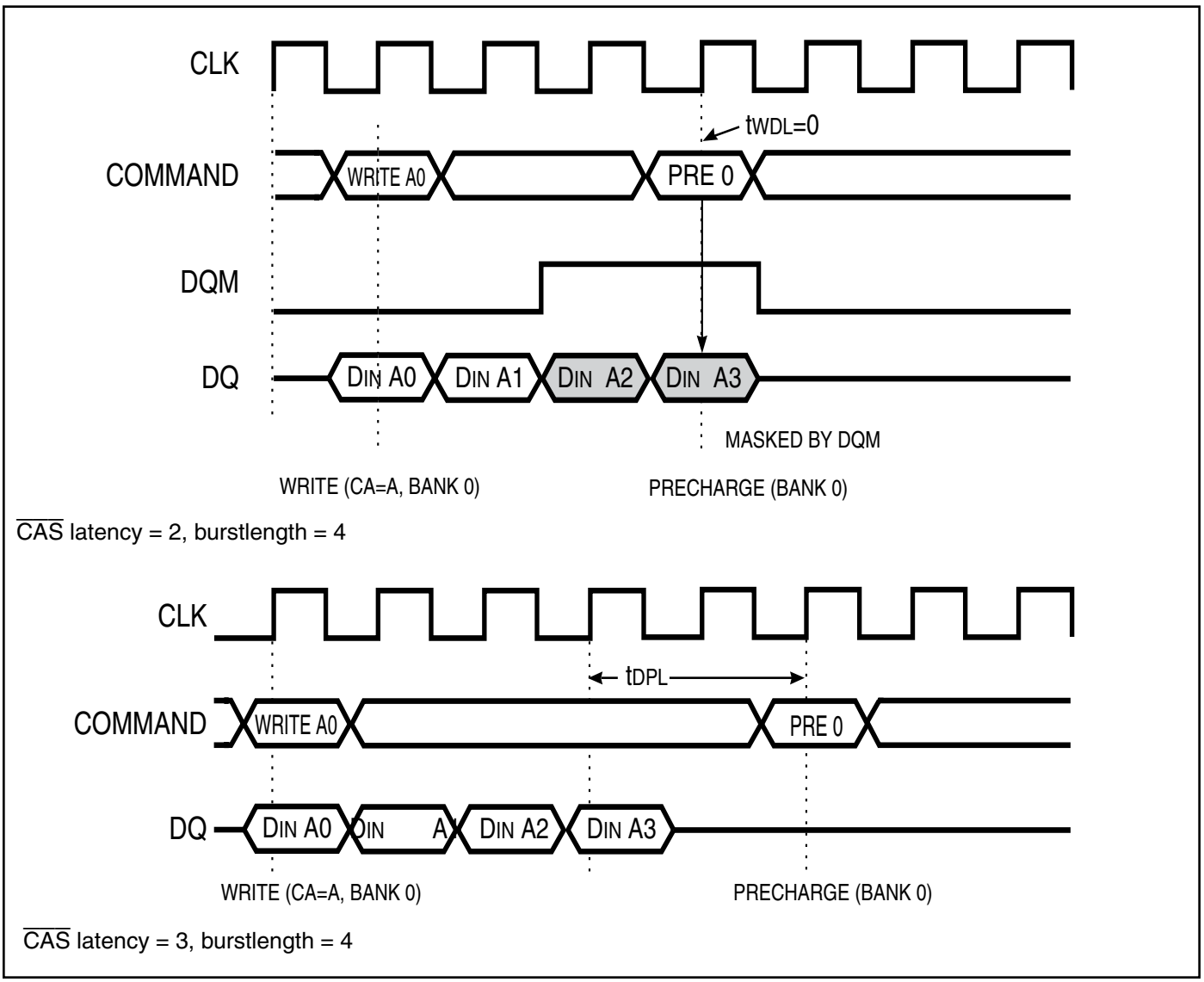
A write cycle can be interrupted by the execution of the precharge command before that cycle completes. The delay time (t_{WDL}) from the precharge command to the point where burst input is invalid, i.e., the point where input data is no longer written to device internal memory is zero clock cycles regardless of the $\overline{CAS}$.

To inhibit invalid write, the DQM signal must be asserted HIGH with the precharge command.

This precharge command and burst write command must be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of dual bank operation.

Inversely, to write all the burst data to the device, the precharge command must be executed after the write data recovery period (t_{DPL}) has elapsed. Therefore, the precharge command must be executed two clock cycles after the input of the last burst data item.

$\overline{CAS}$ Latency	3	2
t_{WDL}	0	0
t_{DPL}	2	2

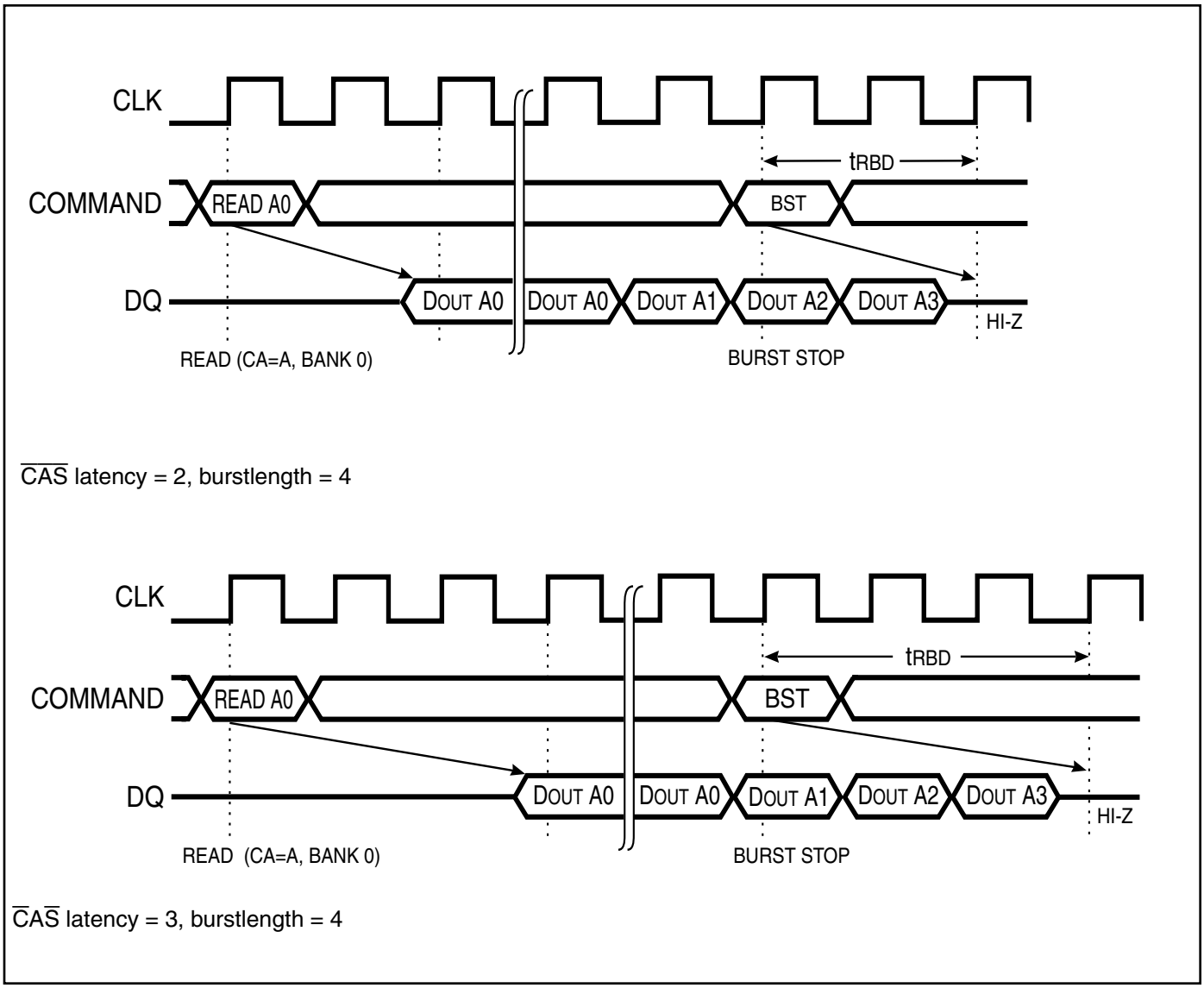


Read Cycle (Full Page) Interruption Using the Burst Stop Command

The IS42/4516100H can output data continuously from the burst start address (a) to location a+255 during a read cycle in which the burst length is set to full page. The IS42/4516100H repeats the operation starting at the 256th cycle with the data output returning to location (a) and continuing with a+1, a+2, a+3, etc. A burst stop command must be executed to terminate this cycle. A precharge command must be executed within the ACT to PRE command period (t_{RAS} max.) following the burst stop command.

After the period (t_{RBD}) required for burst data output to stop following the execution of the burst stop command has elapsed, the outputs go to the HIGH impedance state. This period (t_{RBD}) is two clock cycle when the $\overline{CAS}$ latency is two and three clock cycle when the $\overline{CAS}$ latency is three.

$\overline{CAS}$ **Latency**	**3**	**2**
t_{RBD}	3	2

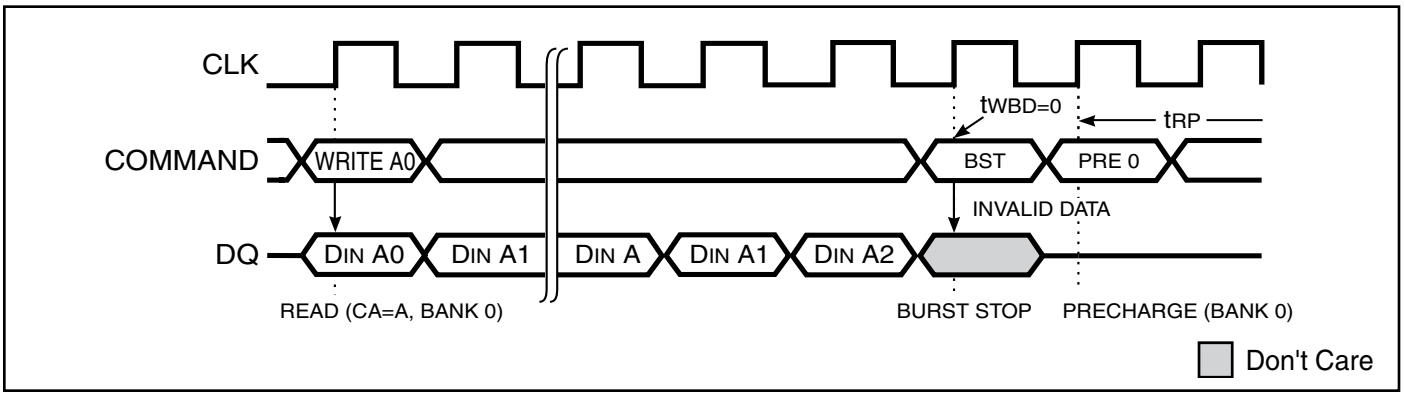


$\overline{CAS}$ latency = 2, burstlength = 4

$\overline{CAS}$ latency = 3, burstlength = 4

Write Cycle (Full Page) Interruption Using the Burst Stop Command

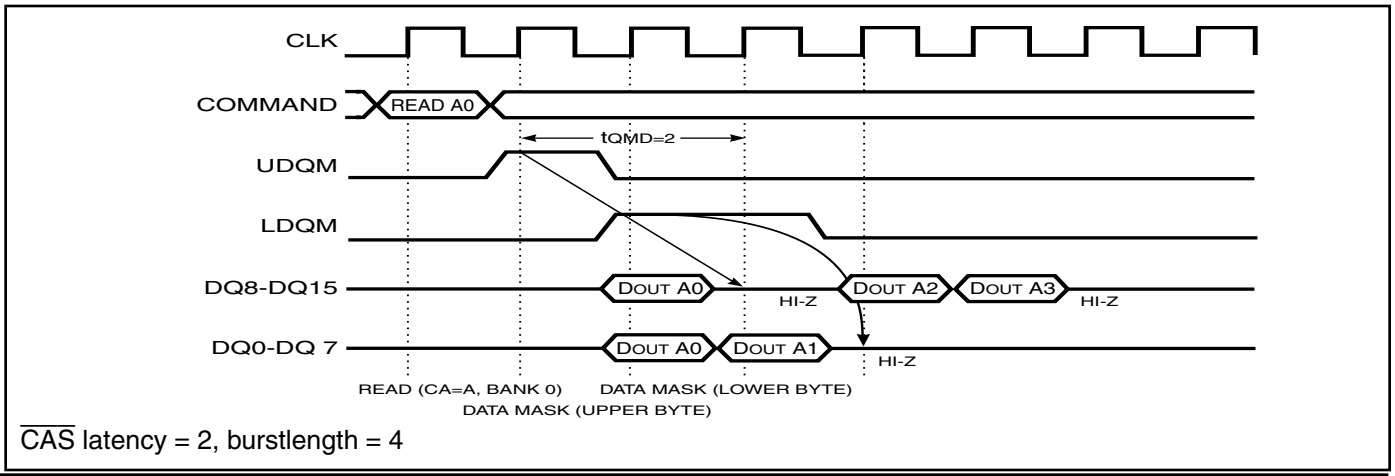
The DRAM can input data continuously from the burst start address (a) to location a+255 during a write cycle in which the burst length is set to full page. The DRAM repeats the operation starting at the 256th cycle with data input returning to location (a) and continuing with a+1, a+2, a+3, etc. A burst stop command must be executed to terminate this cycle. A precharge command must be executed within the ACT to PRE command period (tRAS max.) following the burst stop command. After the period (tWBD) required for burst data input to stop following the execution of the burst stop command has elapsed, the write cycle terminates. This period (tWBD) is zero clock cycles, regardless of the $\overline{CAS}$ latency.



Burst Data Interruption Using the U/LDQM Pins (Read Cycle)

Burst data output can be temporarily interrupted (masked) during a read cycle using the U/LDQM pins. Regardless of the $\overline{CAS}$ latency, two clock cycles (tQMD) after one of the U/LDQM pins goes HIGH, the corresponding outputs go to the HIGH impedance state. Subsequently, the outputs are maintained in the high impedance state as long as that U/LDQM pin remains HIGH. When the U/LDQM pin goes LOW, output is resumed at a time tQMD later. This output control operates independently on a byte basis with the UDQM pin controlling upper byte output (pins DQ8-DQ15) and the LDQM pin controlling lower byte output (pins DQ0 to DQ7).

Since the U/LDQM pins control the device output buffers only, the read cycle continues internally and, in particular, incrementing of the internal burst counter continues.



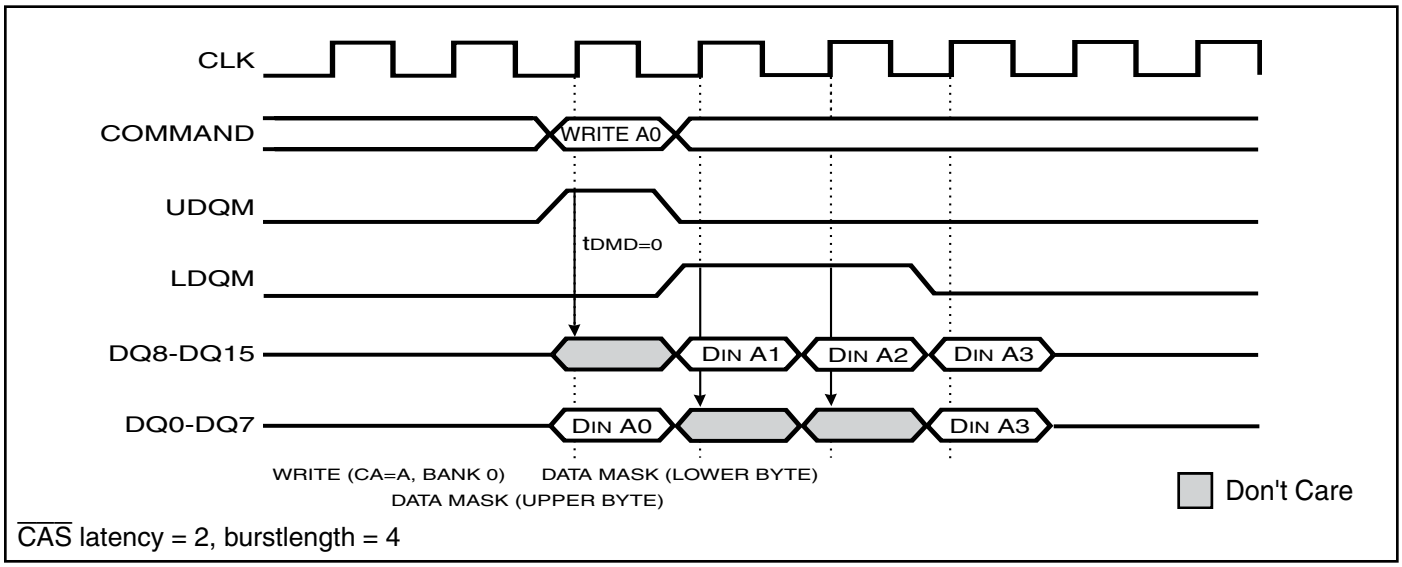
$\overline{CAS}$ latency = 2, burstlength = 4

Burst Data Interruption U/LDQM Pins (Write Cycle)

Burst data input can be temporarily interrupted (muted) during a write cycle using the U/LDQM pins. Regardless of the $\overline{CAS}$ latency, as soon as one of the U/LDQM pins goes HIGH, the corresponding externally applied input data will no longer be written to the device internal circuits. Subsequently, the corresponding input continues to be muted as long as that U/LDQM pin remains HIGH.

The DRAM will revert to accepting input as soon as that pin is dropped to LOW and data will be written to the device. This input control operates independently on a byte basis with the UDQM pin controlling upper byte input (pin DQ8 to DQ15) and the LDQM pin controlling the lower byte input (pins DQ0 to DQ7).

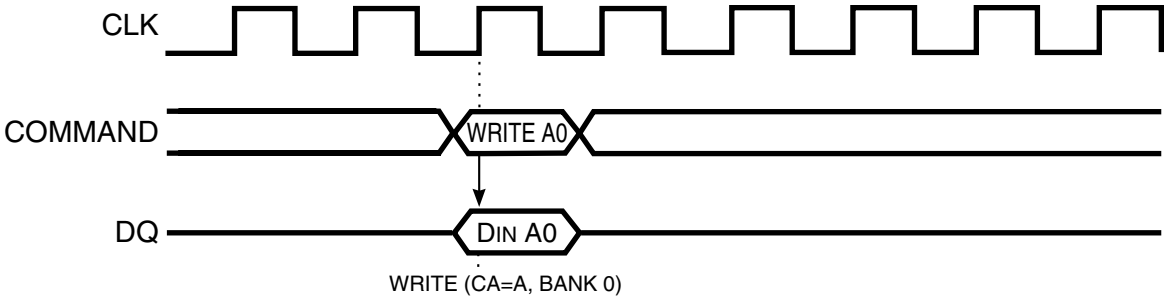
Since the U/LDQM pins control the device input buffers only, the cycle continues internally and, in particular, incrementing of the internal burst counter continues.



$\overline{CAS}$ latency = 2, burstlength = 4

Burst Read and Single Write

The burst read and single write mode is set up using the mode register set command. During this operation, the burst read cycle operates normally, but the write cycle only writes a single data item for each write cycle. The $\overline{CAS}$ latency and DQM latency are the same as in normal mode.

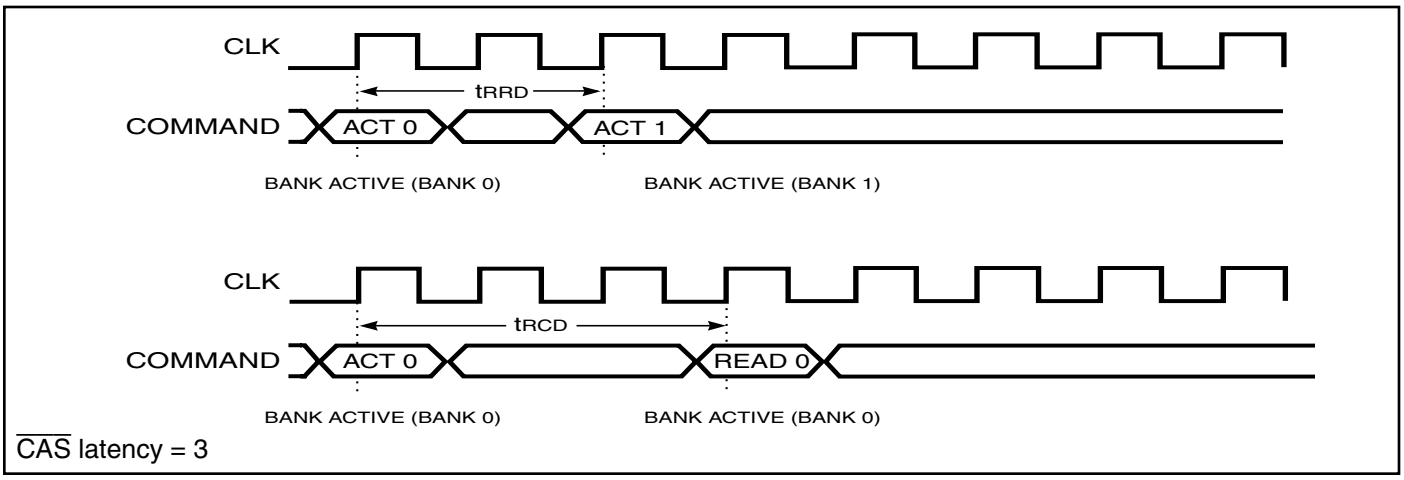


$\overline{CAS}$ latency = 2, 3

Bank Active Command Interval

When the selected bank is precharged, the period trp has elapsed and the bank has entered the idle state, the bank can be activated by executing the active command. If the other bank is in the idle state at that time, the active command can be executed for that bank after the period tRRD has elapsed. At that point both banks will be in the active state. When a bank active command has been executed, a precharge command must be executed for that bank within the ACT to PRE command period (tRAS max). Also note that a precharge command cannot be executed for an active bank before tRAS (min) has elapsed.

After a bank active command has been executed and the trcd period has elapsed, read write (including auto-precharge) commands can be executed for that bank.



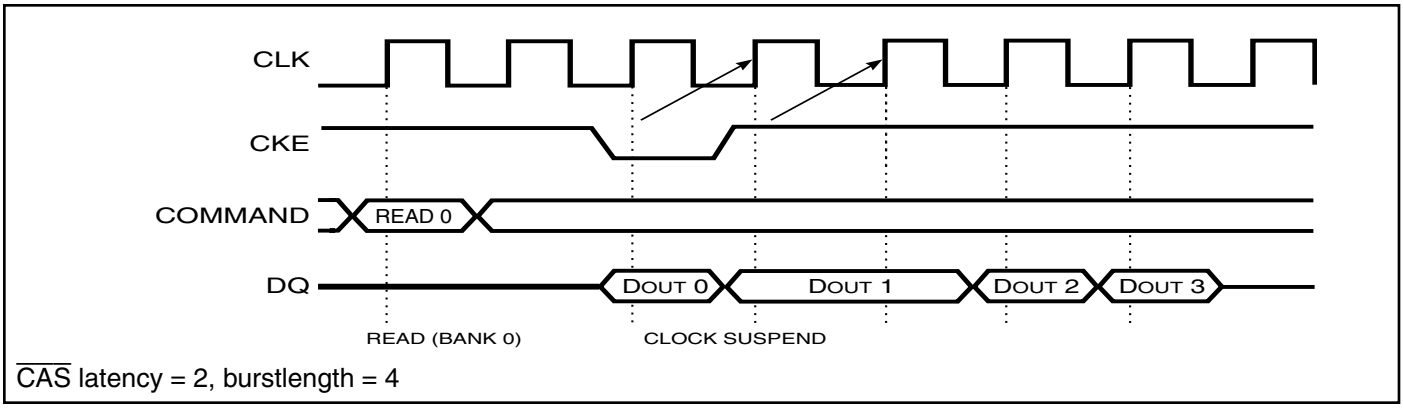
$\overline{CAS}$ latency = 3

Clock Suspend

When the CKE pin is dropped from HIGH to LOW during a read or write cycle, the DRAM enters clock suspend mode on the next CLK rising edge. This command reduces the device power dissipation by stopping the device internal clock. Clock suspend mode continues as long as the CKE pin remains low. In this state, all inputs other than CKE pin are invalid and no other commands can be executed. Also, the device internal states are maintained. When the CKE pin goes from LOW to HIGH clock suspend mode is terminated on the next CLK rising edge and device operation resumes.

The next command cannot be executed until the recovery period (tCKA) has elapsed.

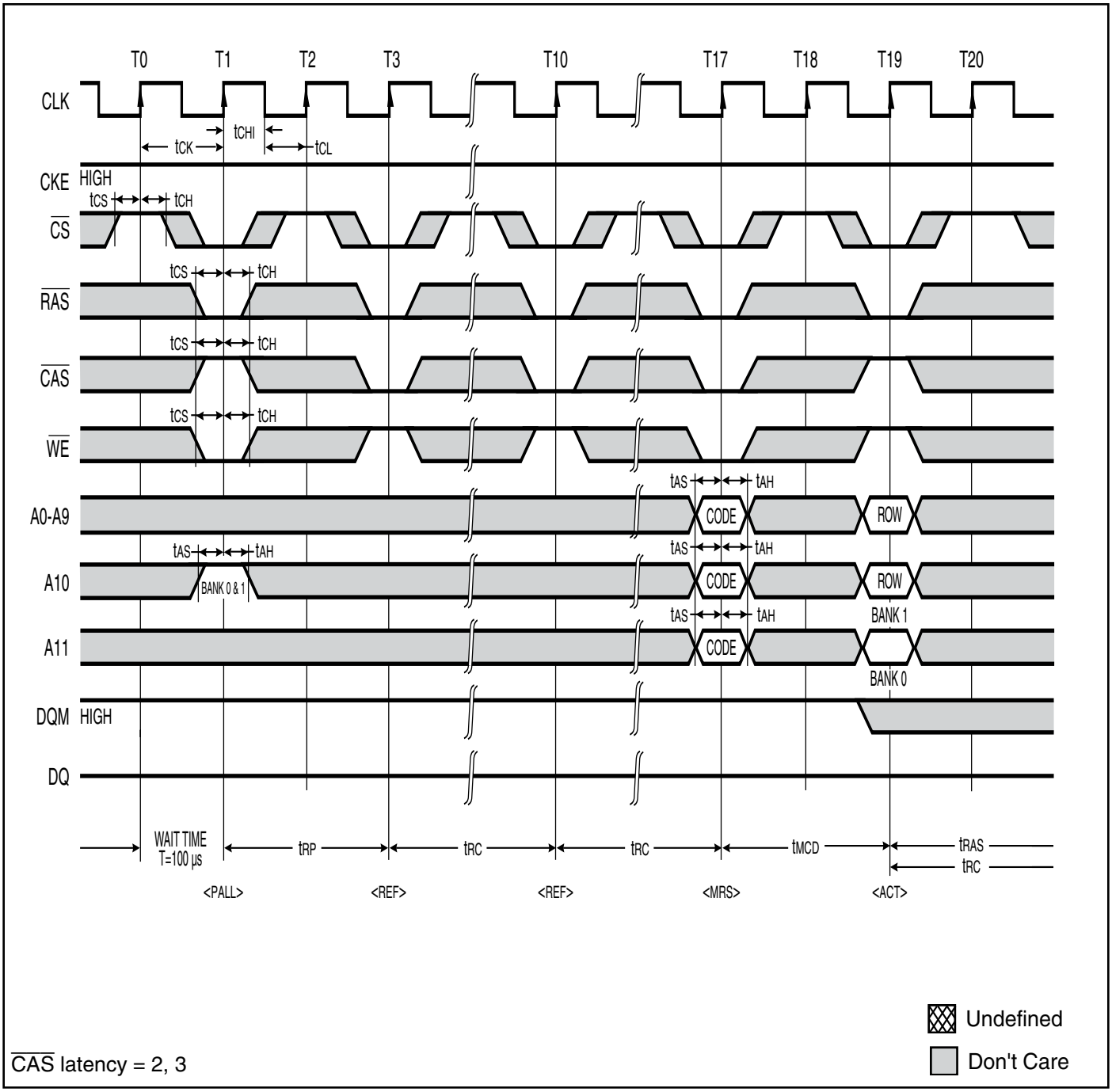
Since this command differs from the self-refresh command described previously in that the refresh operation is not performed automatically internally, the refresh operation must be performed within the refresh period (tref). Thus the maximum time that clock suspend mode can be held is just under the refresh cycle time.



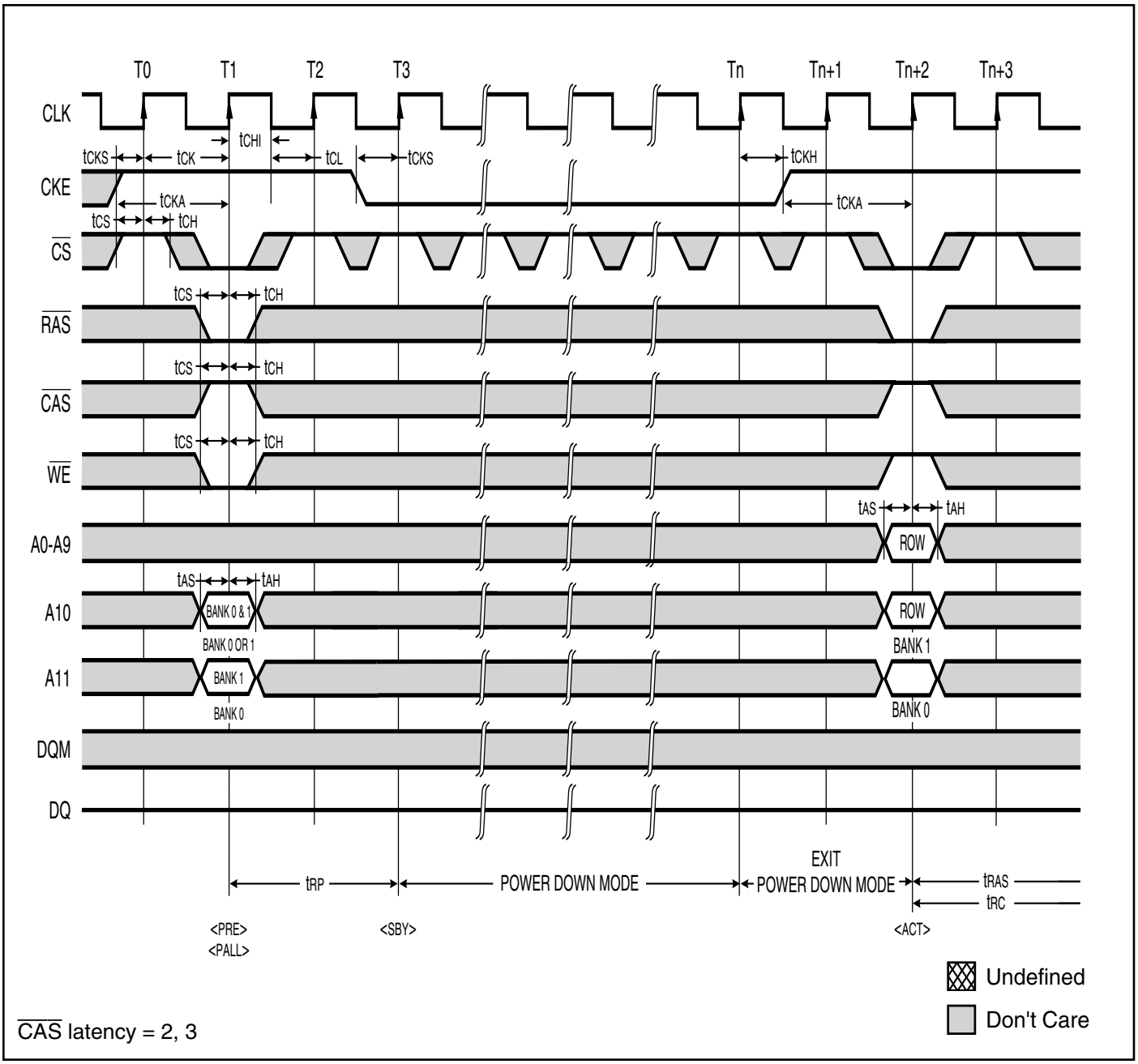
$\overline{CAS}$ latency = 2, burstlength = 4

OPERATION TIMING EXAMPLE

Power-On Sequence, Mode Register Set Cycle

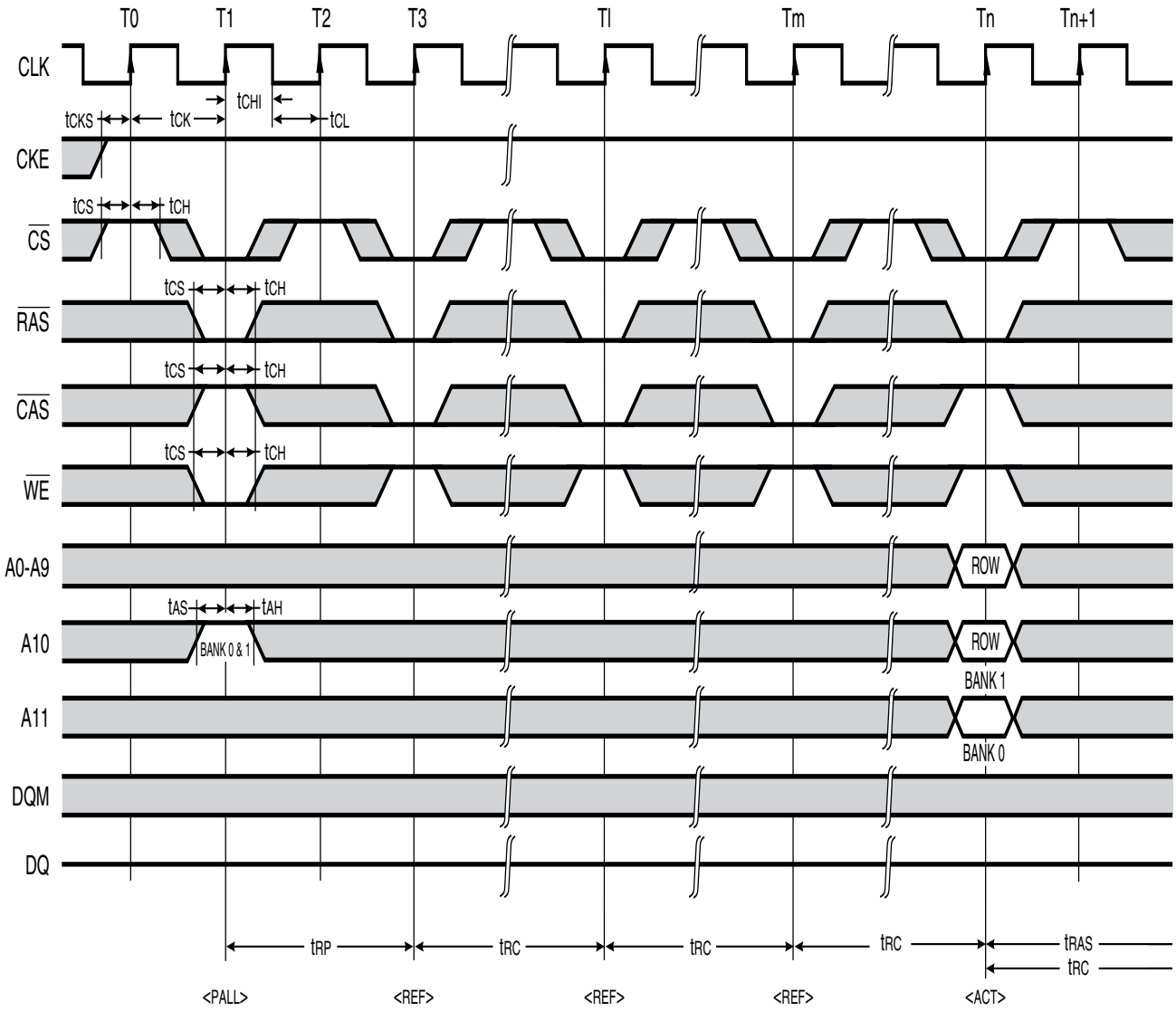


Power-Down Mode Cycle



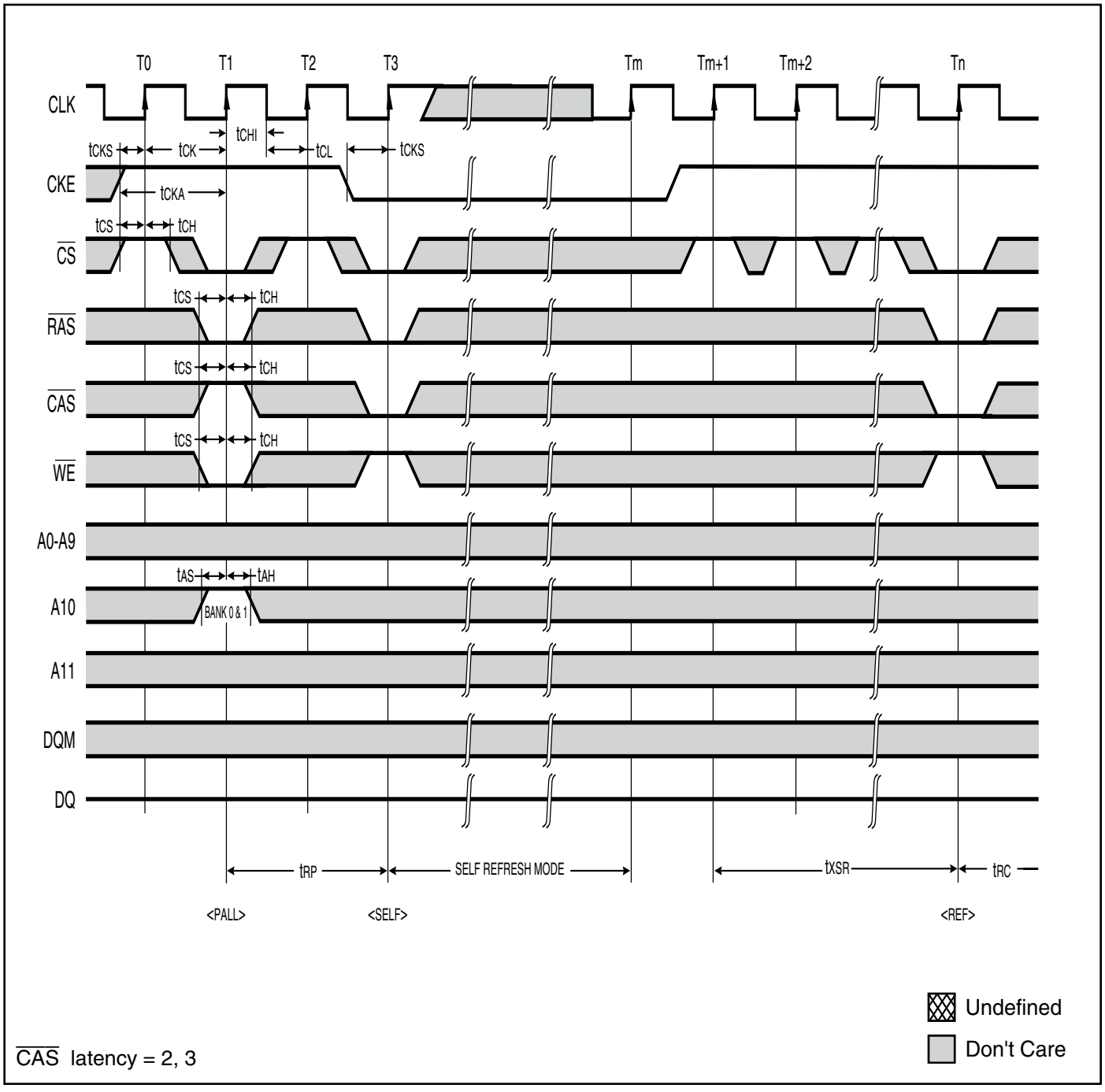
CAS latency = 2, 3

Auto-Refresh Cycle



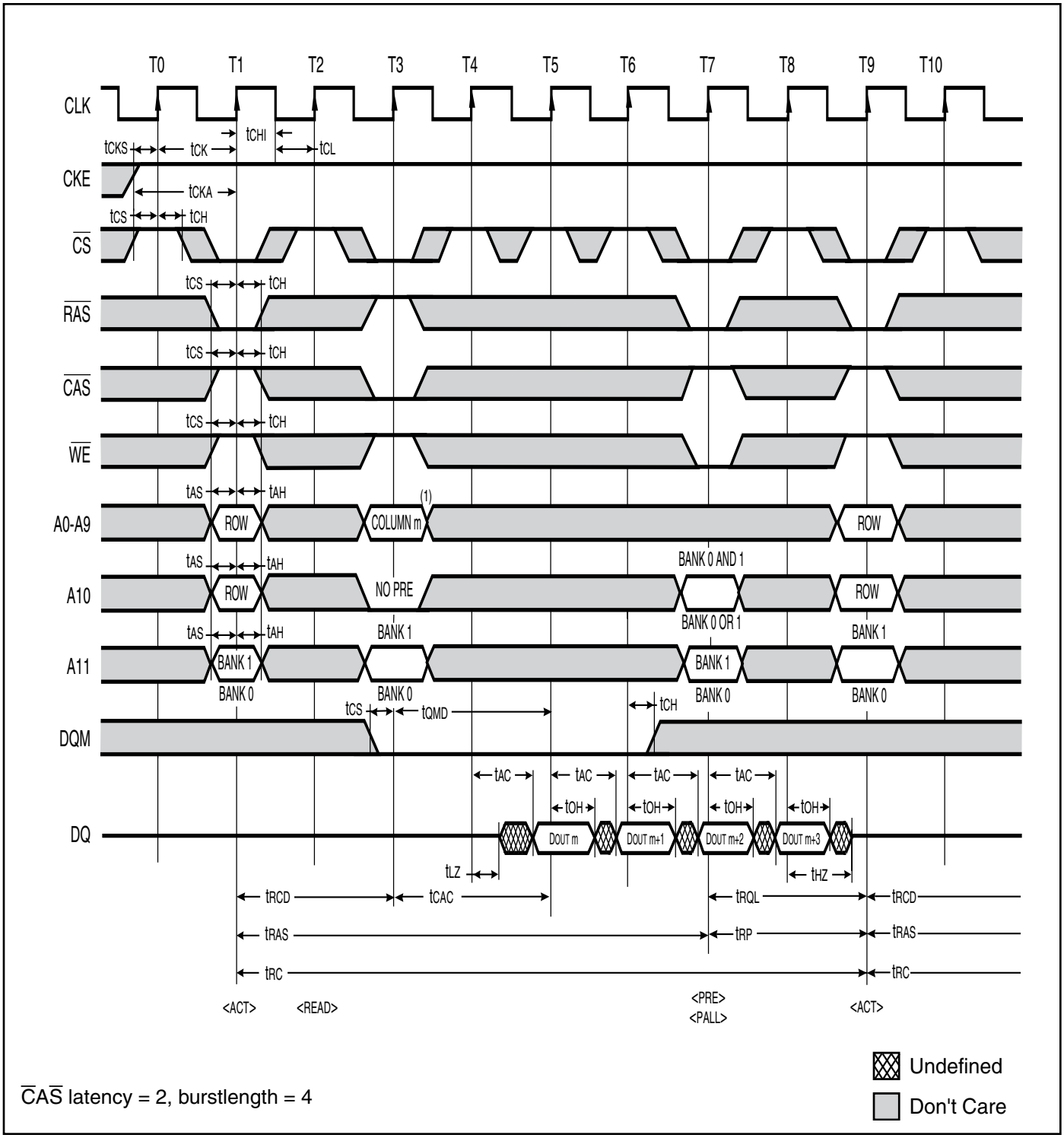
$\overline{CAS}$ latency = 2, 3

Self-Refresh Cycle



Note:
1: A8, A9 = Don't Care.
2. Self-Refresh Mode is not supported for A2 grade with T_A > 85°C.

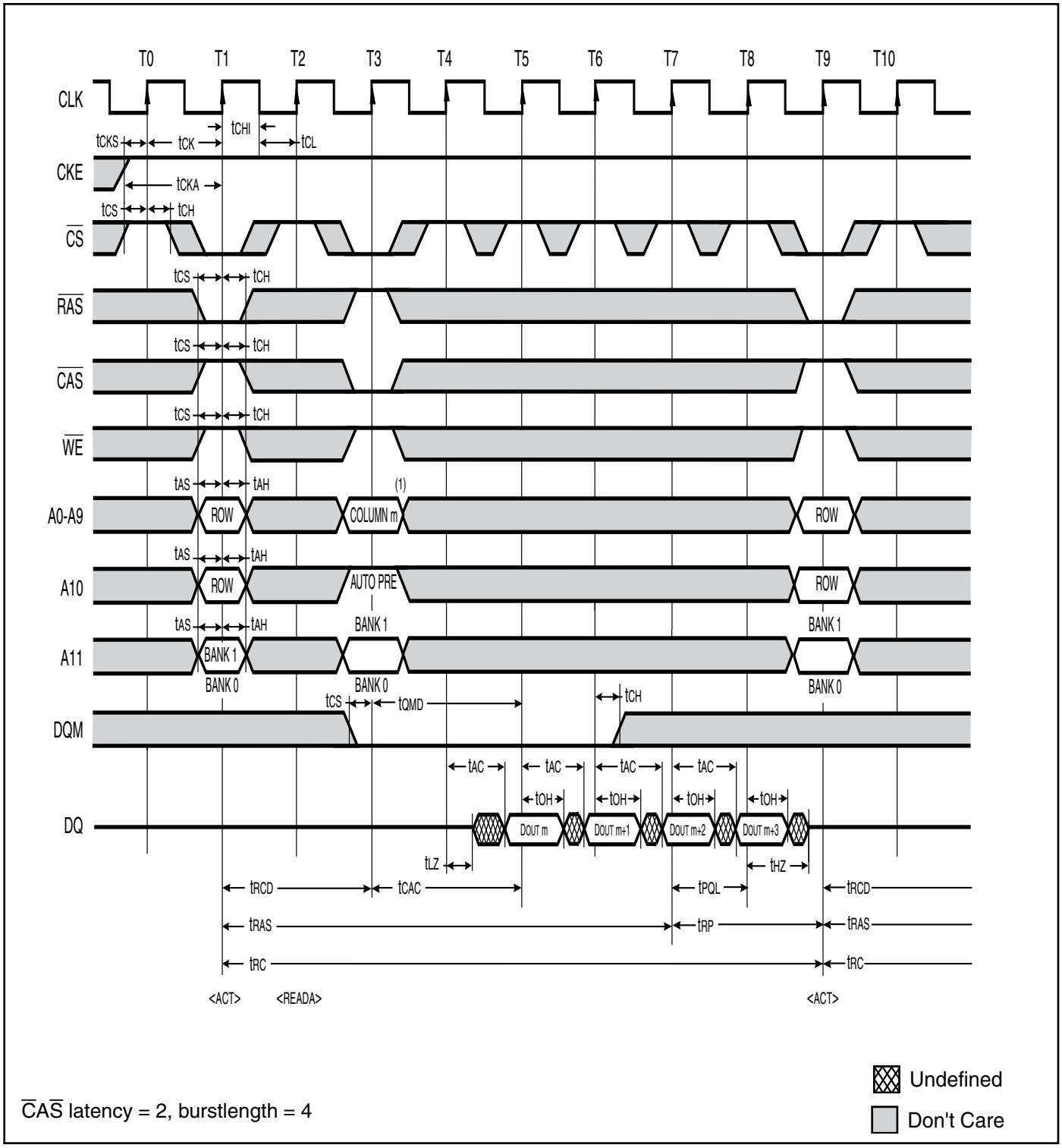
Read Cycle



$\overline{CAS}$ latency = 2, burstlength = 4

Note 1: A8,A9 = Don't Care.

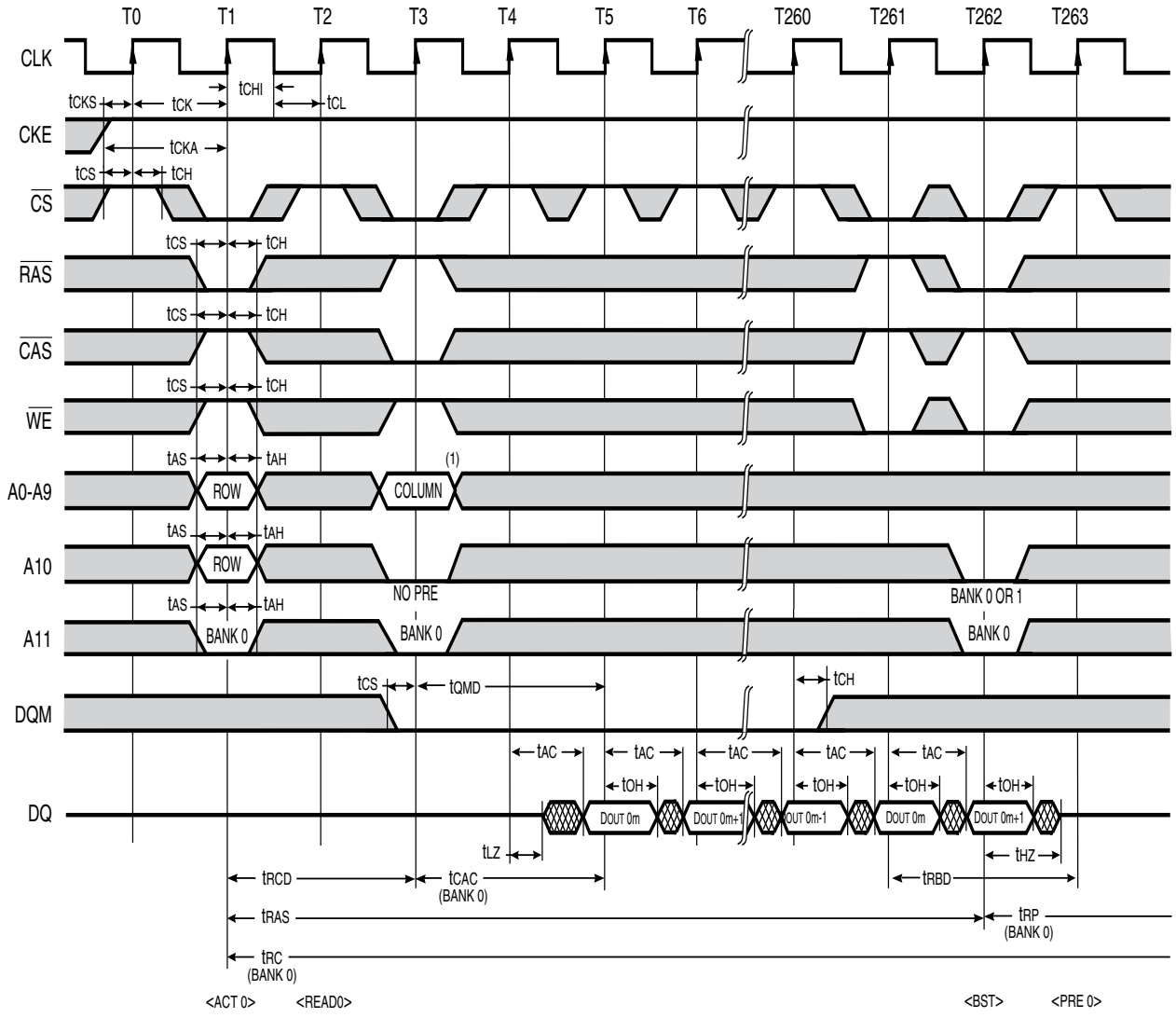
Read Cycle / Auto-Precharge



CAS latency = 2, burstlength = 4

Note 1: A8,A9 = Don't Care.

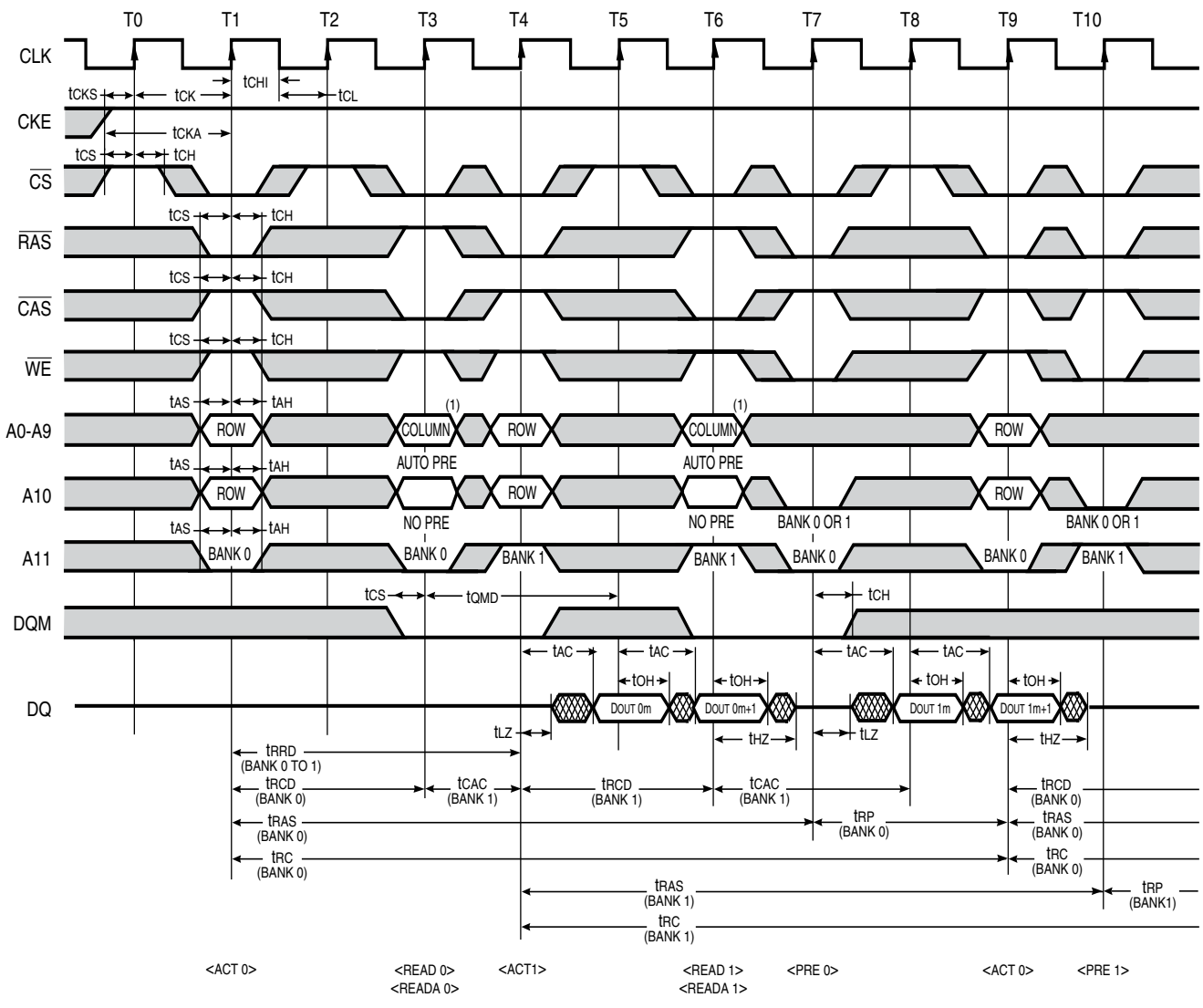
Read Cycle / Full Page



$\overline{CAS}$ latency = 2, burstlength = full page

Note 1: A8,A9 = Don't Care.

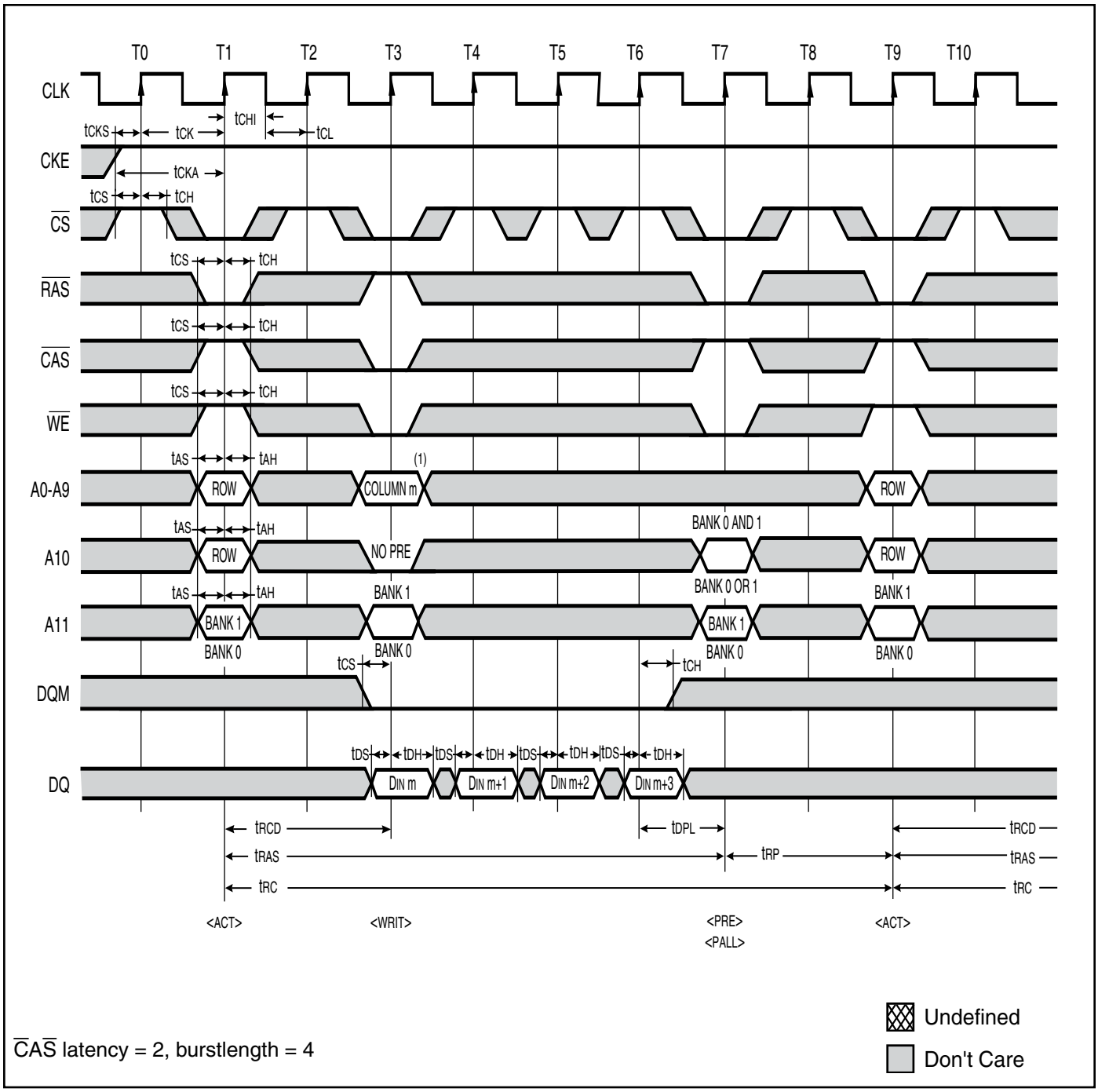
Read Cycle / Ping-Pong Operation (Bank Switching)



CAS latency = 2, burstlength = 2

Note 1: A8,A9 = Don't Care.

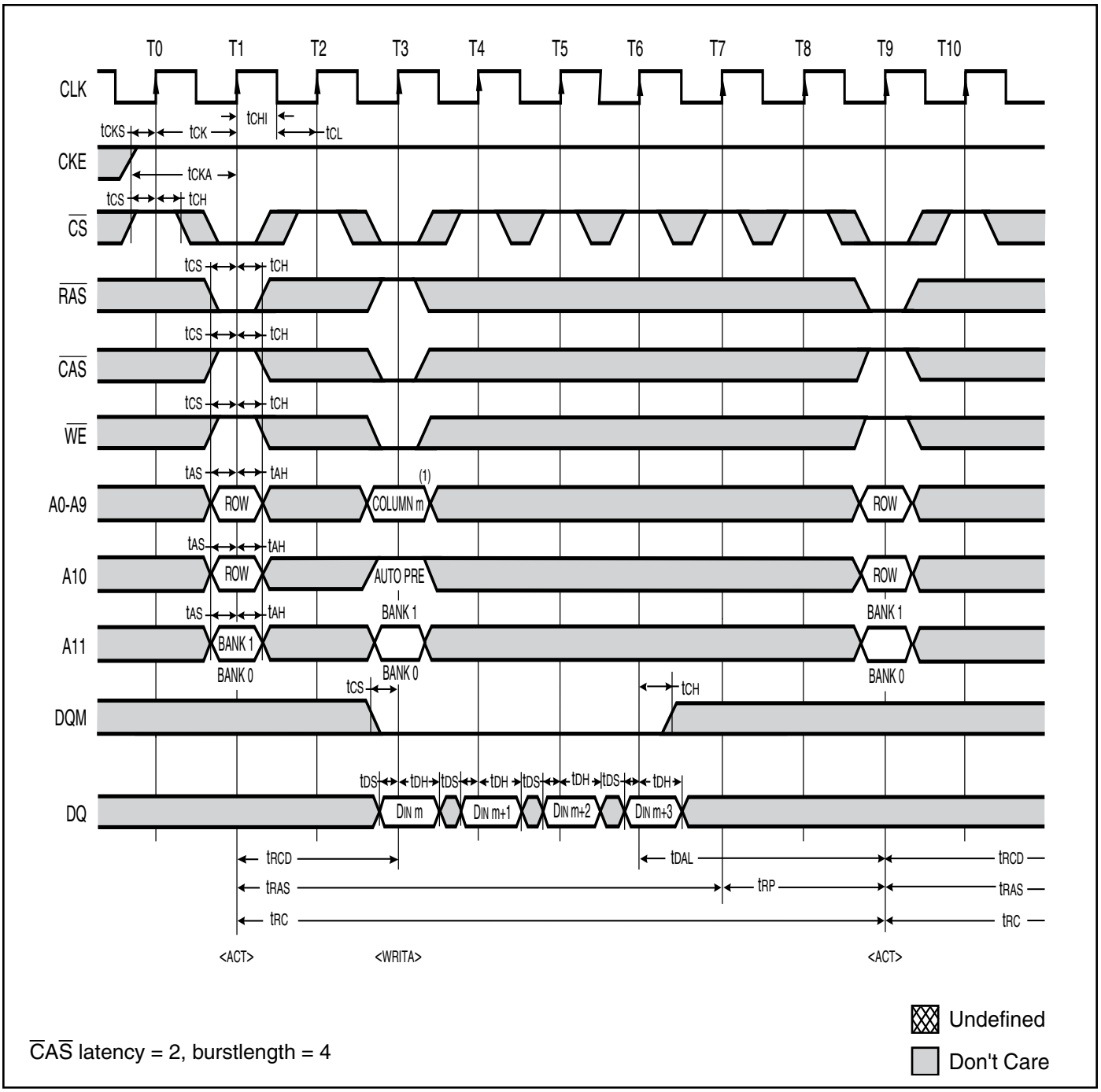
Write Cycle



CAS latency = 2, burstlength = 4

Note 1: A8,A9 = Don't Care.

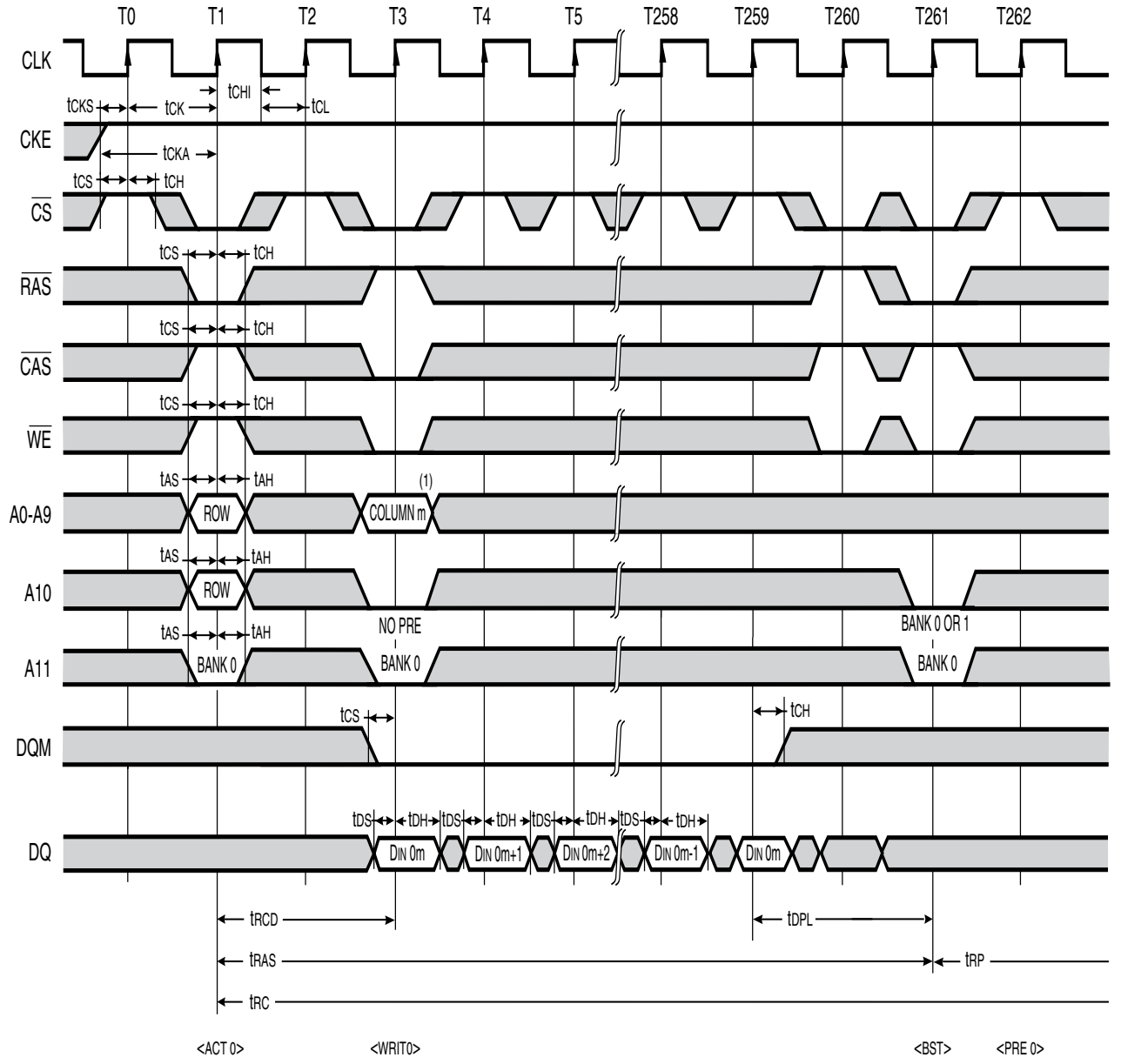
Write Cycle / Auto-Precharge



CAS latency = 2, burstlength = 4

Note 1: A8,A9 = Don't Care.

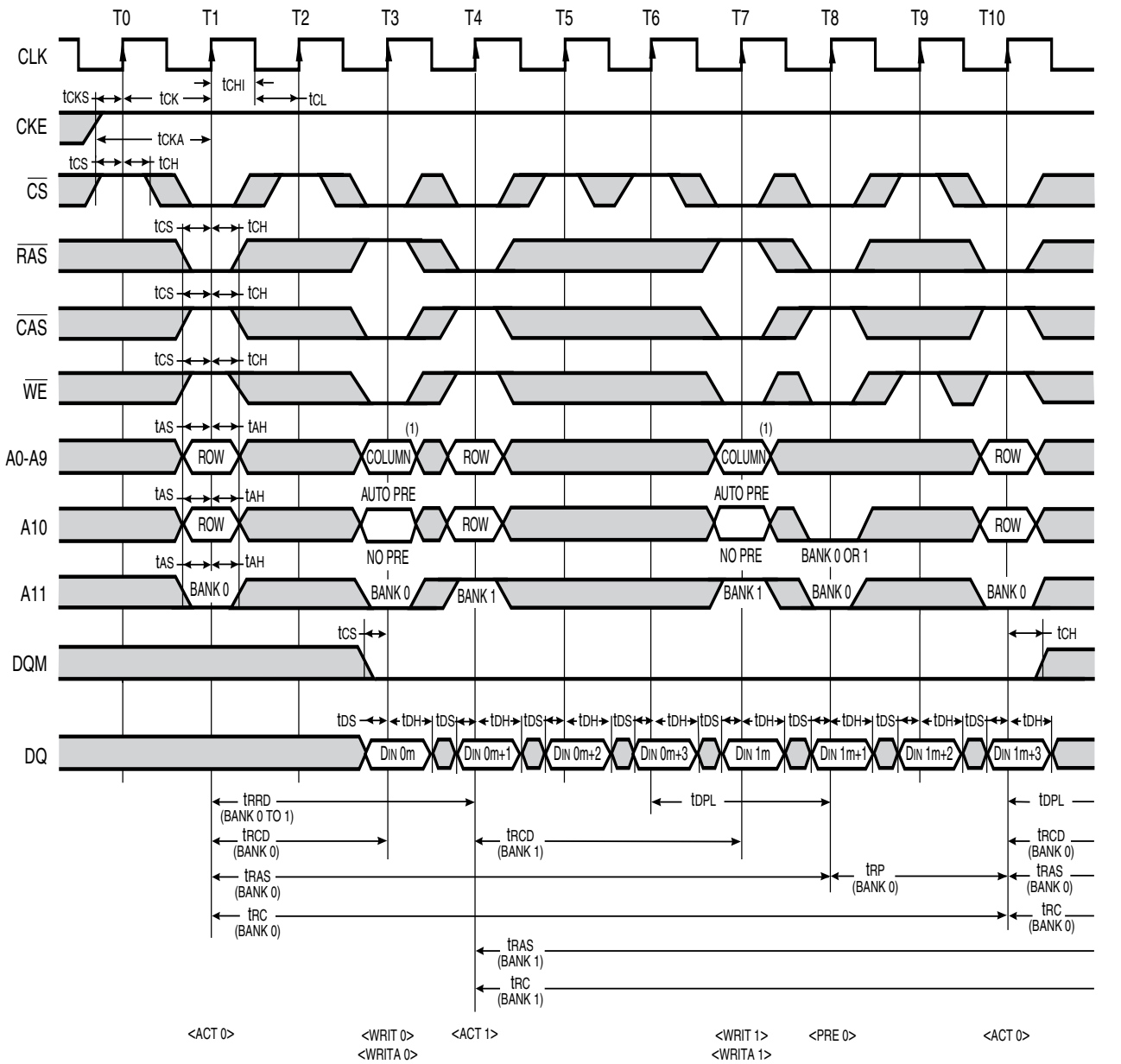
Write Cycle / Full Page



CAS latency = 2, burst length = full page

Note 1: A8,A9 = Don't Care.

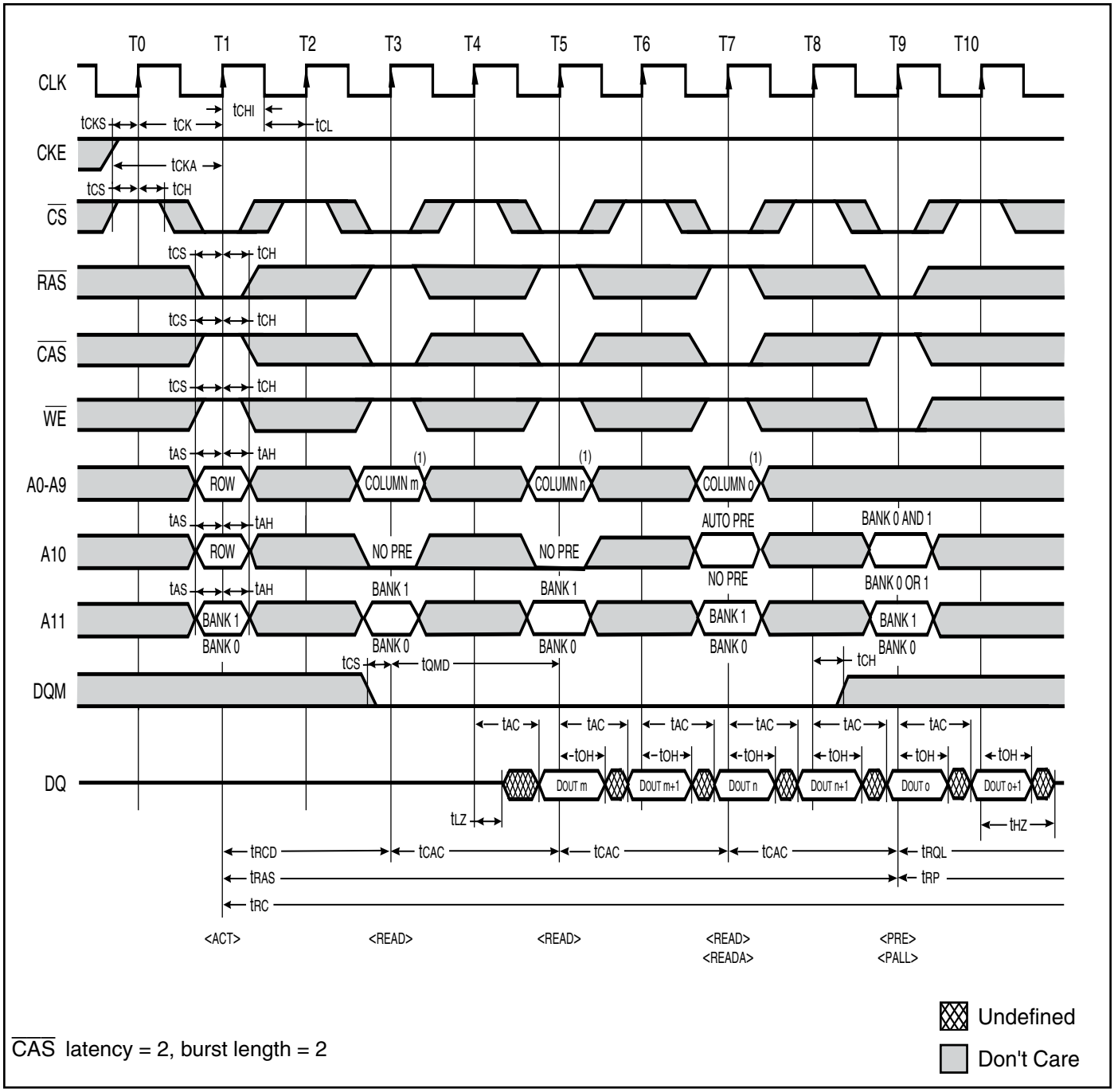
Write Cycle / Ping-Pong Operation



CAS latency = 2, burst length = 2

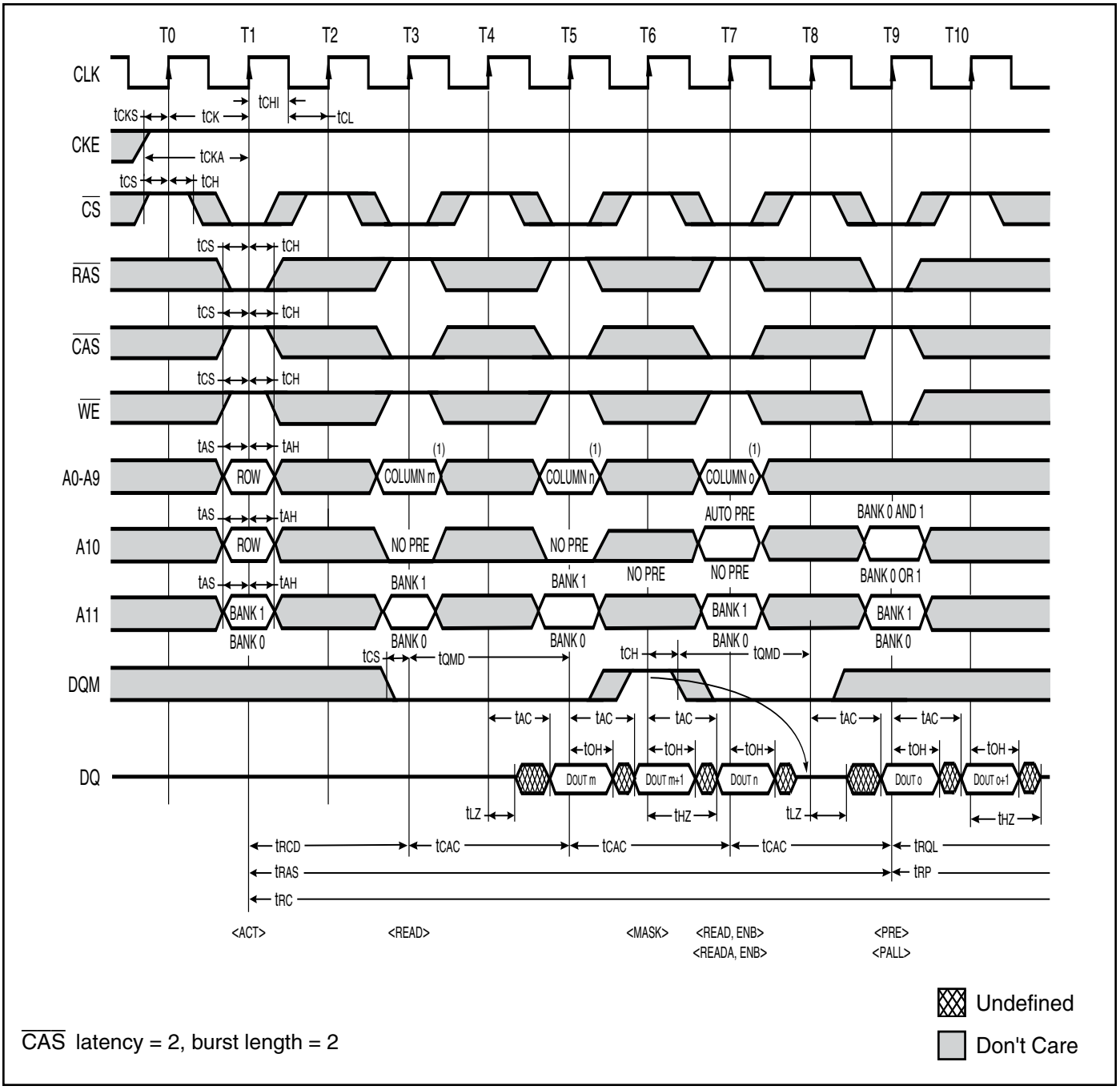
Note 1: A8,A9 = Don't Care.

Read Cycle / Page Mode



Note 1: A8,A9 = Don't Care.

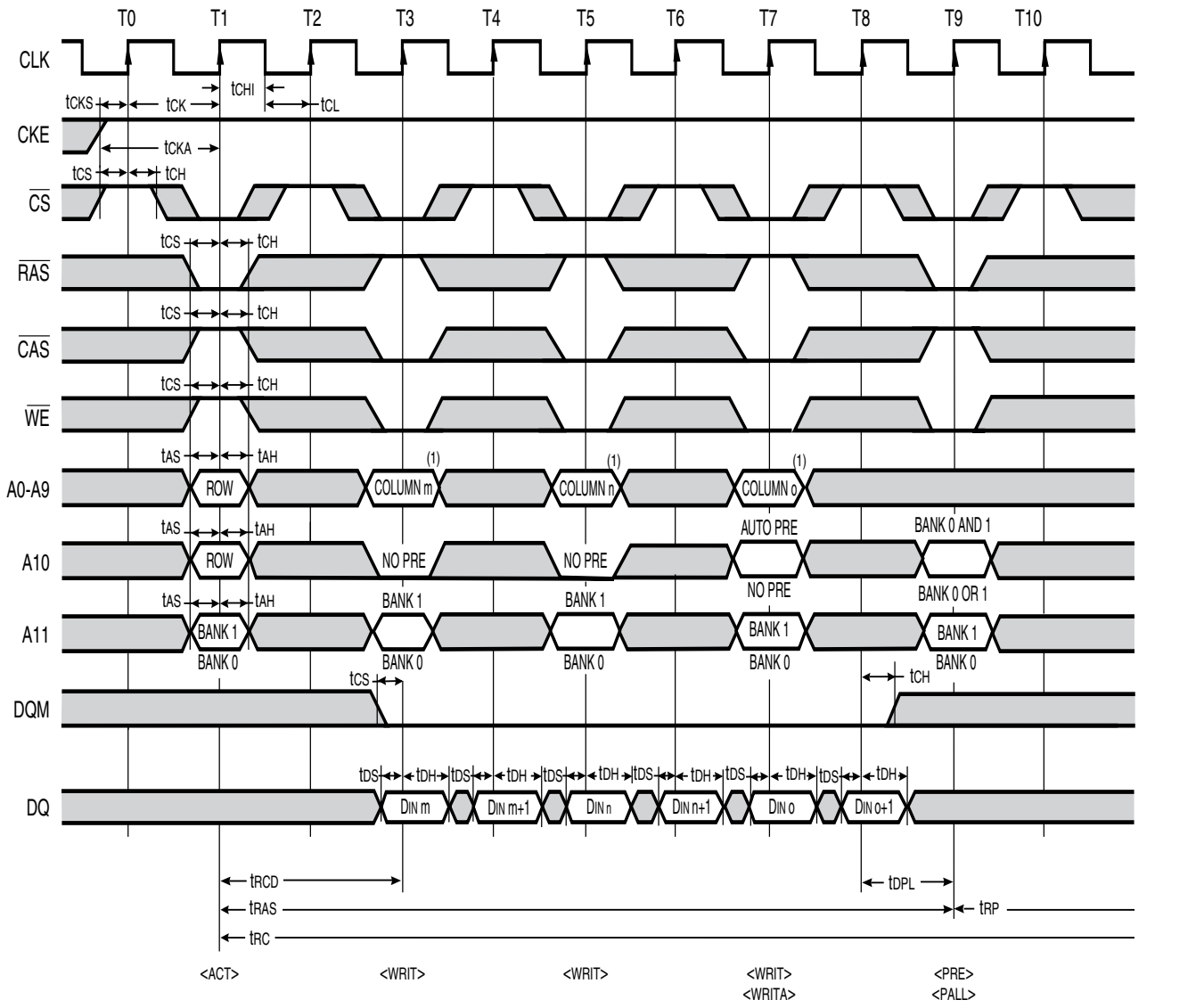
Read Cycle / Page Mode; Data Masking



CAS latency = 2, burst length = 2

Note 1: A8,A9 = Don't Care.

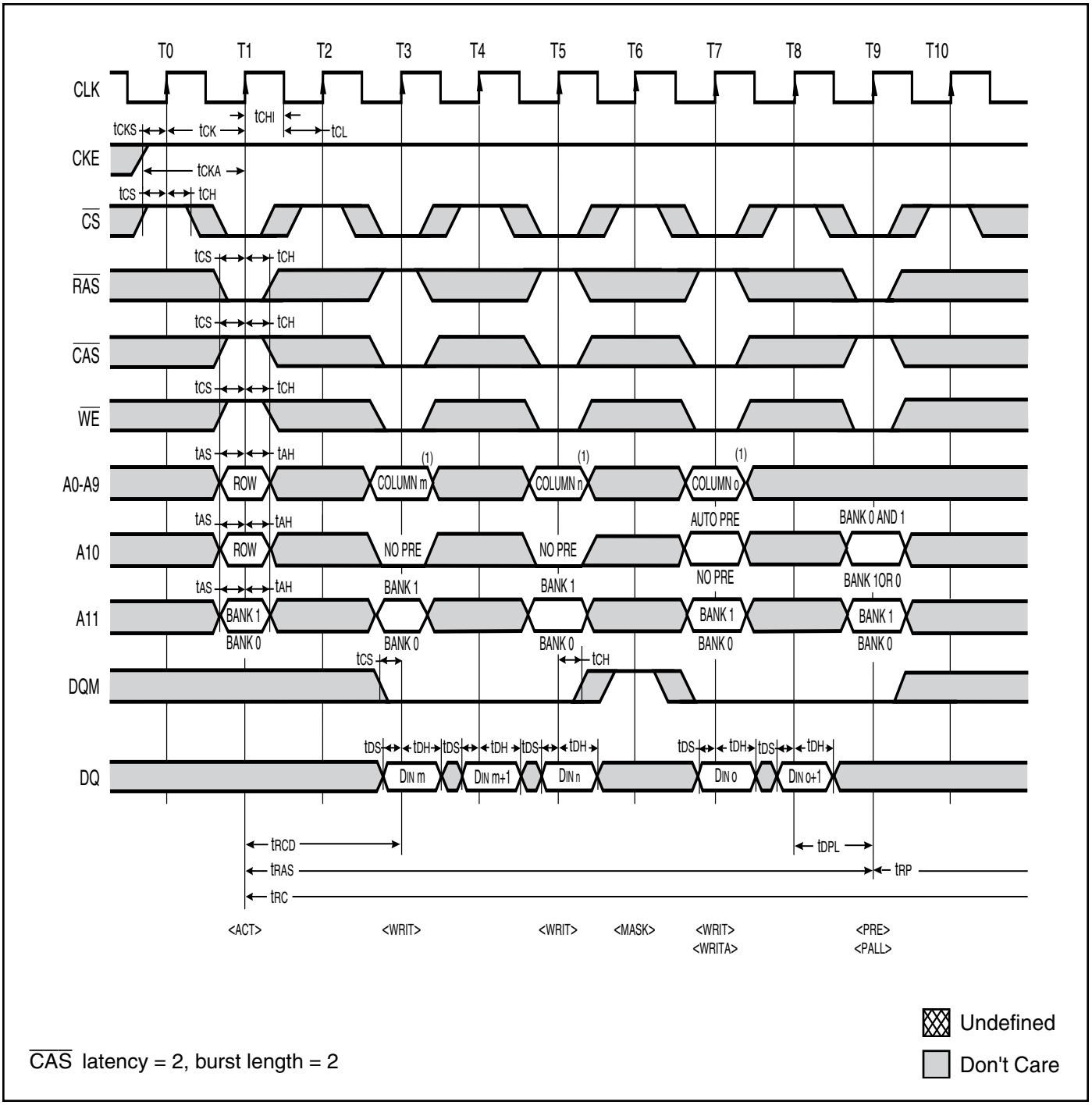
Write Cycle / Page Mode



CAS latency = 2, burst length = 2

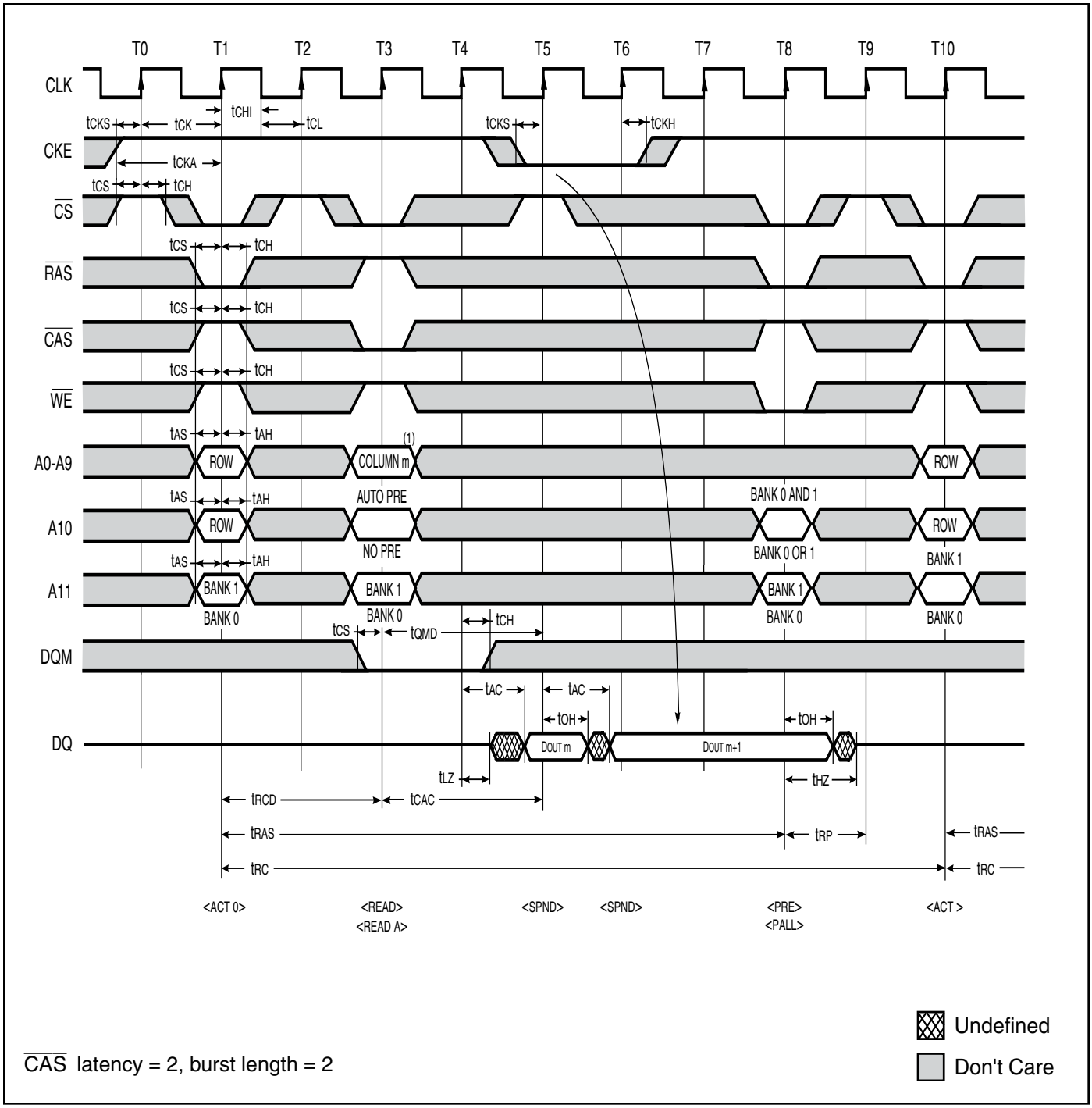
Note 1: A8,A9 = Don't Care.

Write Cycle / Page Mode; Data Masking



Note 1: A8,A9 = Don't Care.

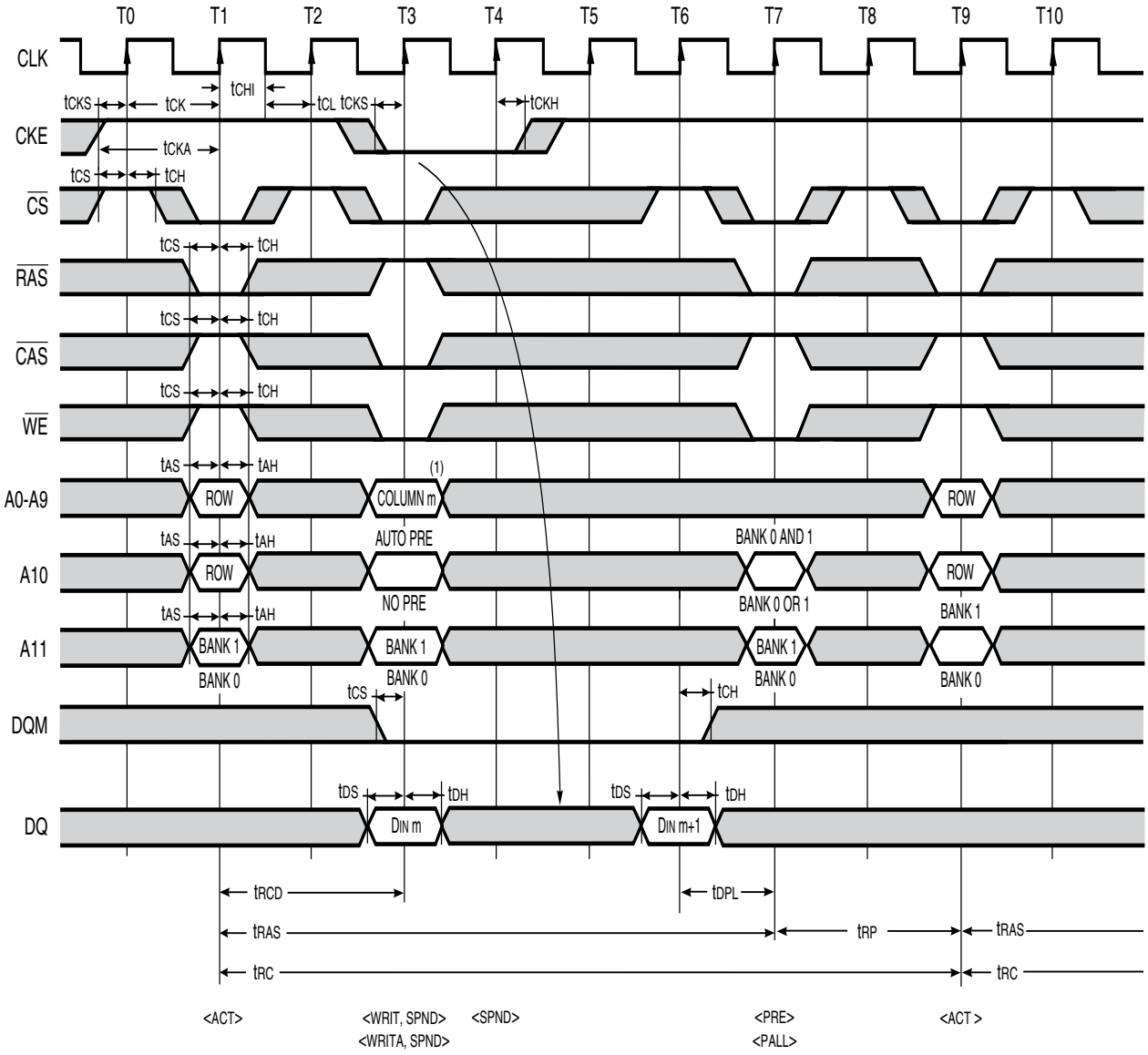
Read Cycle / Clock Suspend



CAS latency = 2, burst length = 2

Note 1: A8,A9 = Don't Care.

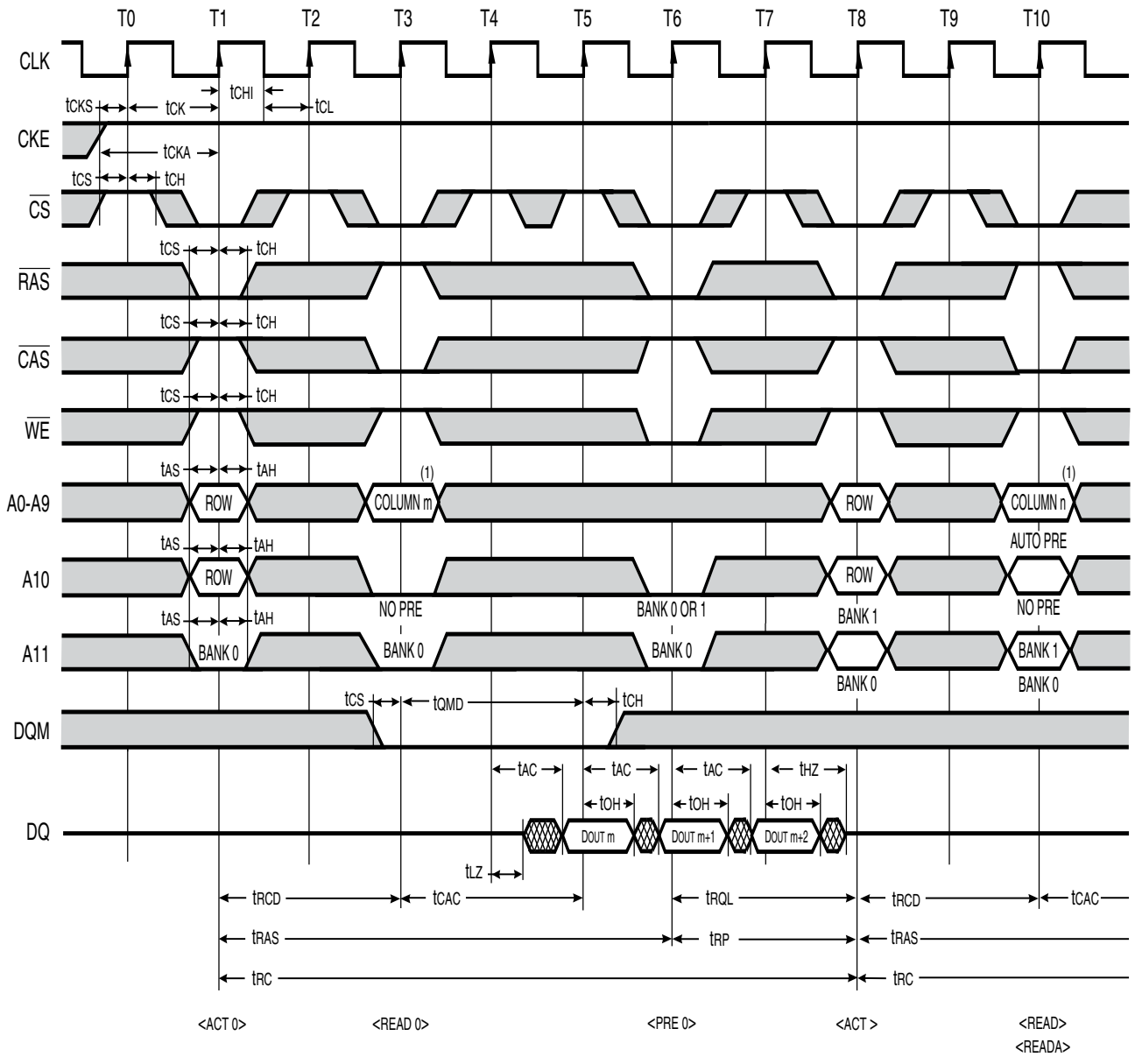
Write Cycle / Clock Suspend



CAS latency = 2, burst length = 2

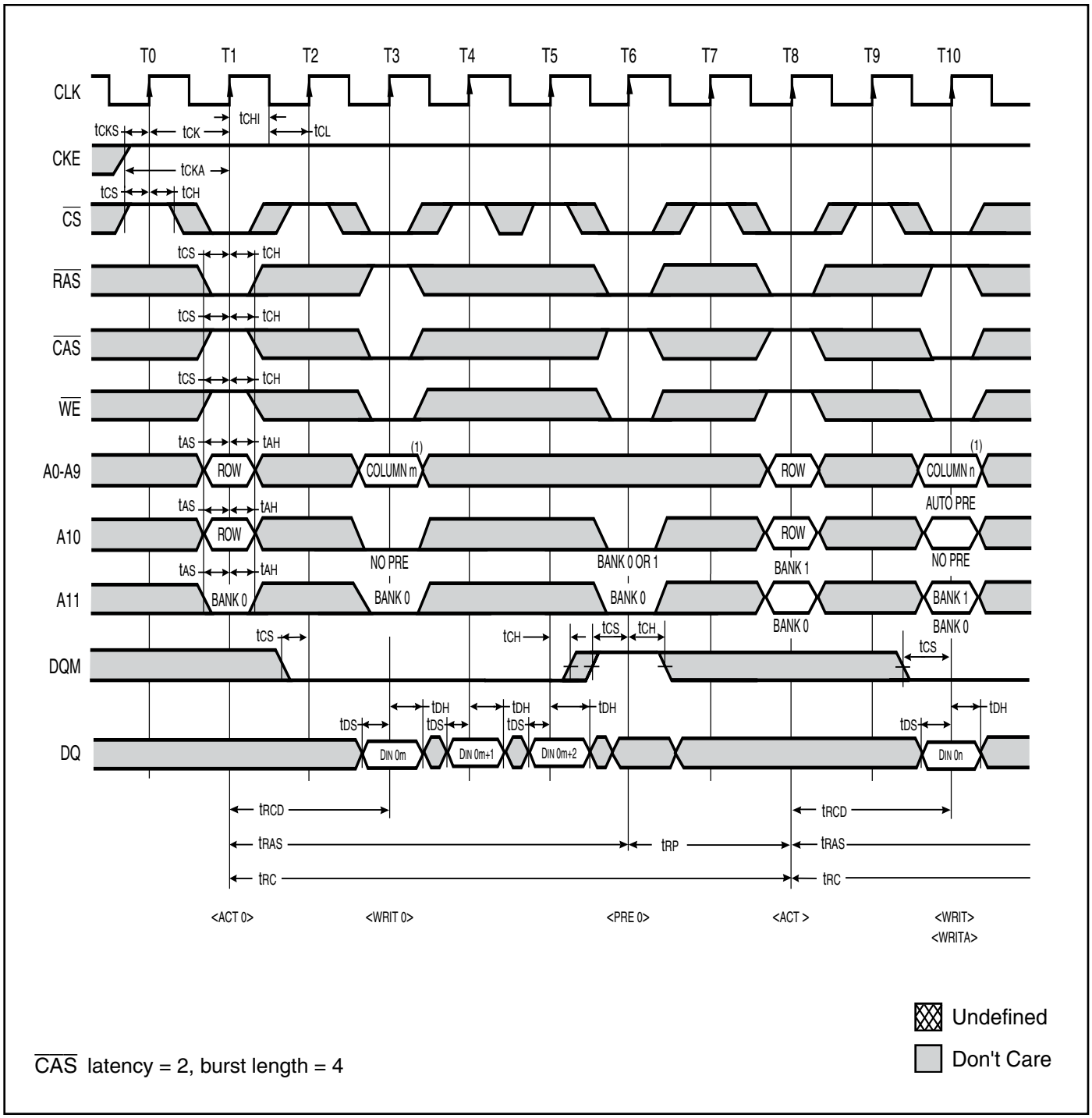
Note 1: A8,A9 = Don't Care.

Read Cycle / Precharge Termination



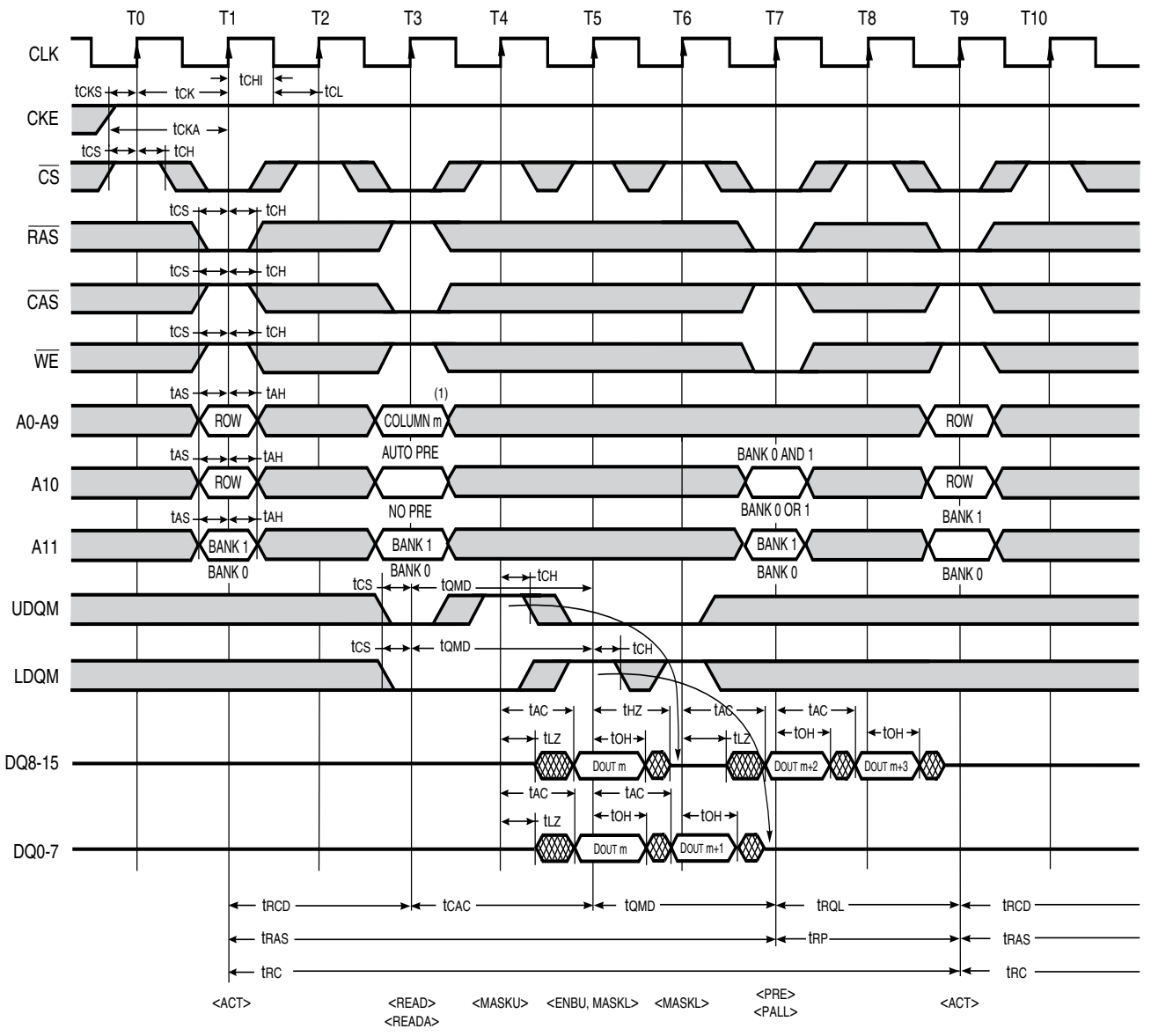
Note 1: A8,A9 = Don't Care.

Write Cycle / Precharge Termination



Note 1: A8,A9 = Don't Care.

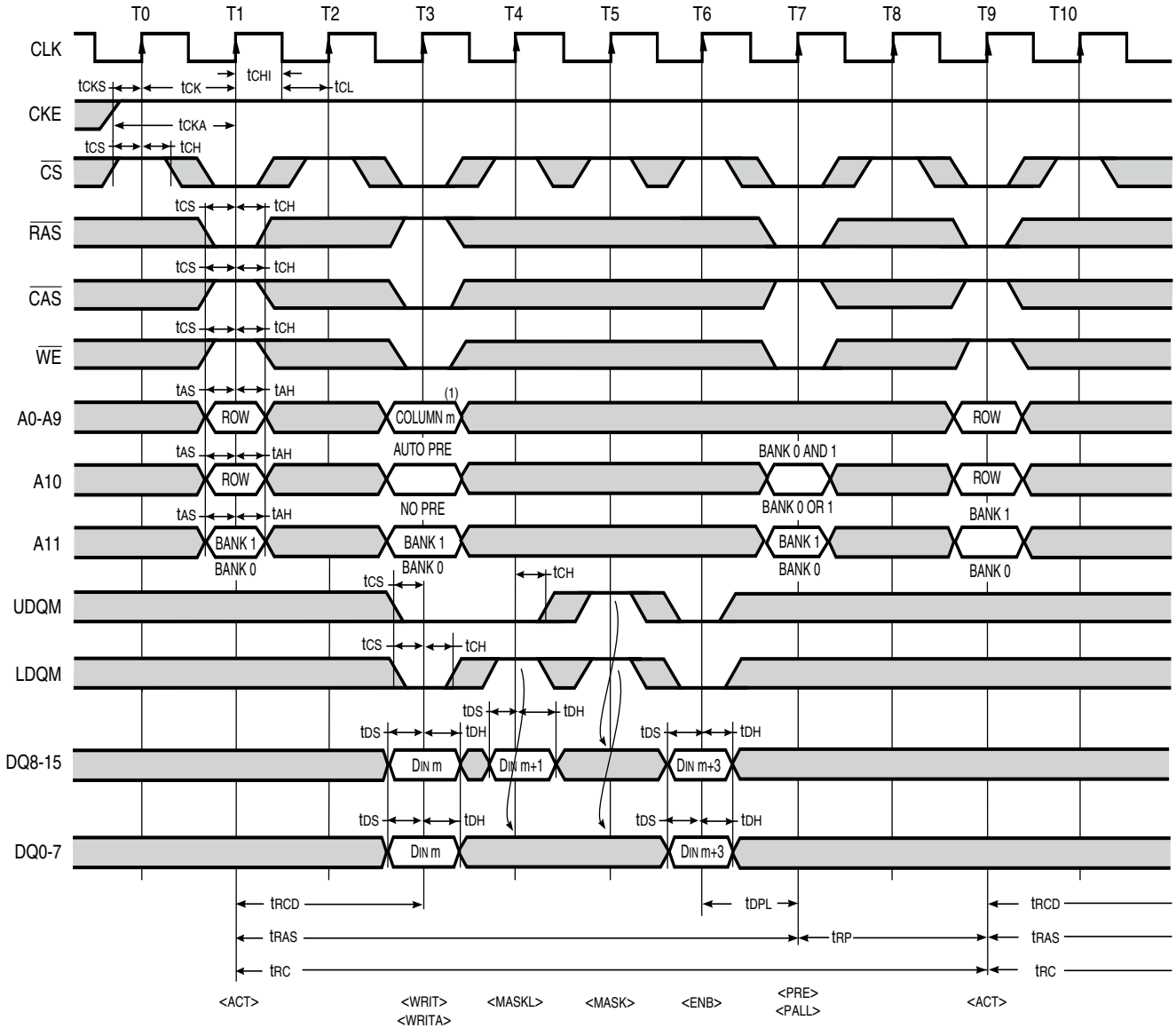
Read Cycle / Byte Operation



CAS latency = 2, burst length = 4

Note 1: A8,A9 = Don't Care.

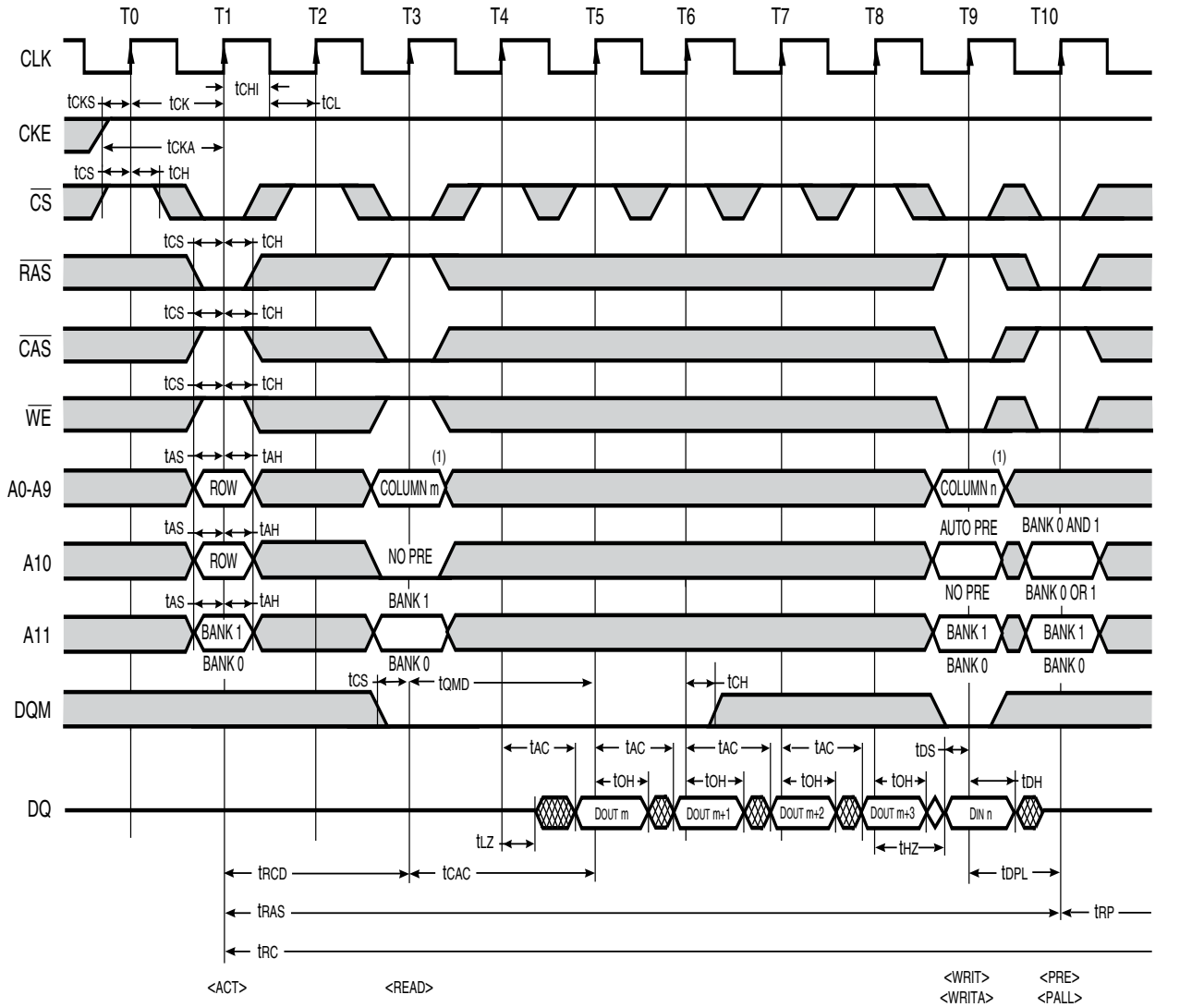
Write Cycle / Byte Operation



CAS latency = 2, burst length = 4

Note 1: A8,A9 = Don't Care.

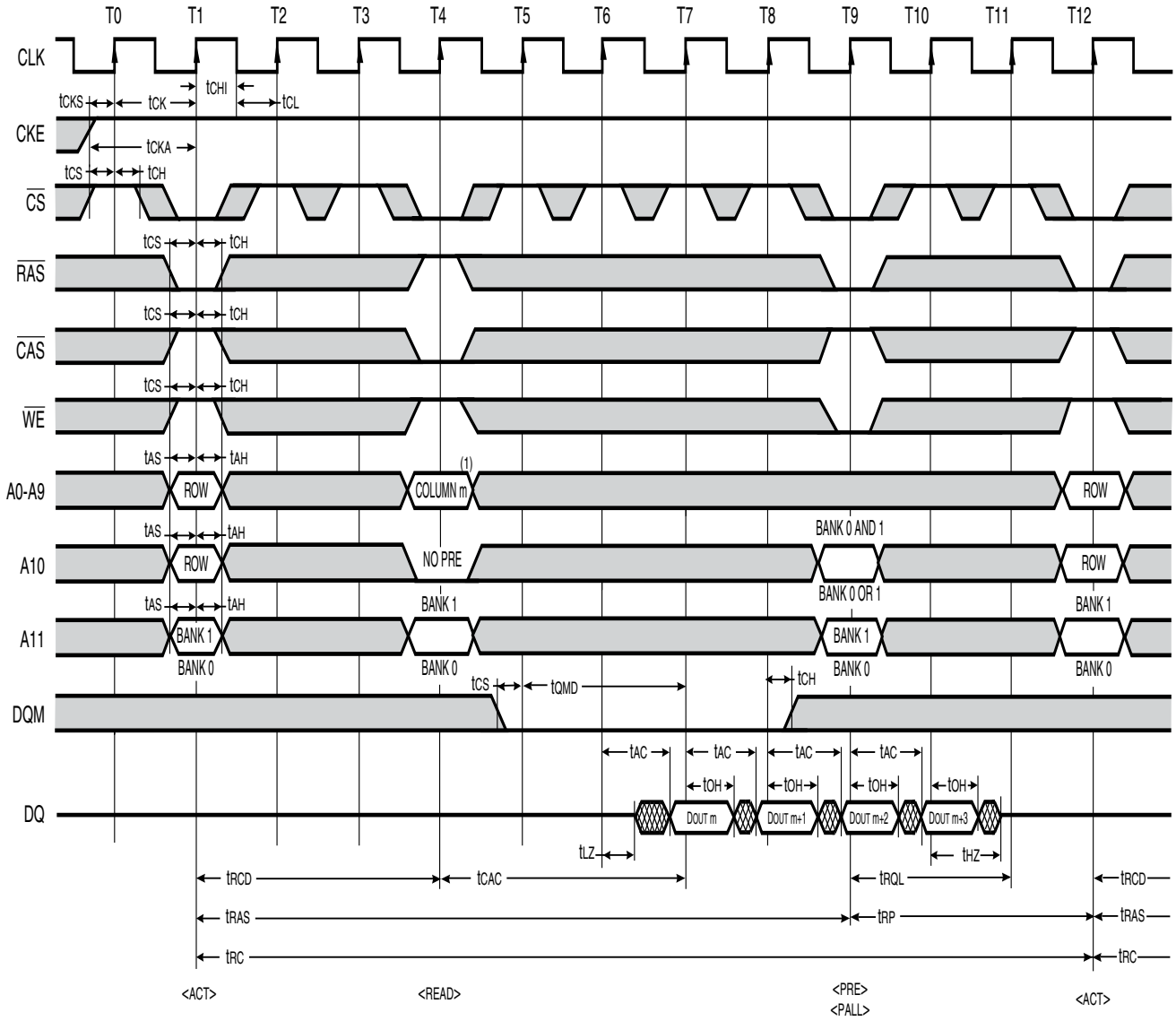
Read Cycle, Write Cycle / Burst Read, Single Write



$\overline{CAS}$ latency = 2, burst length = 4

Note 1: A8,A9 = Don't Care.

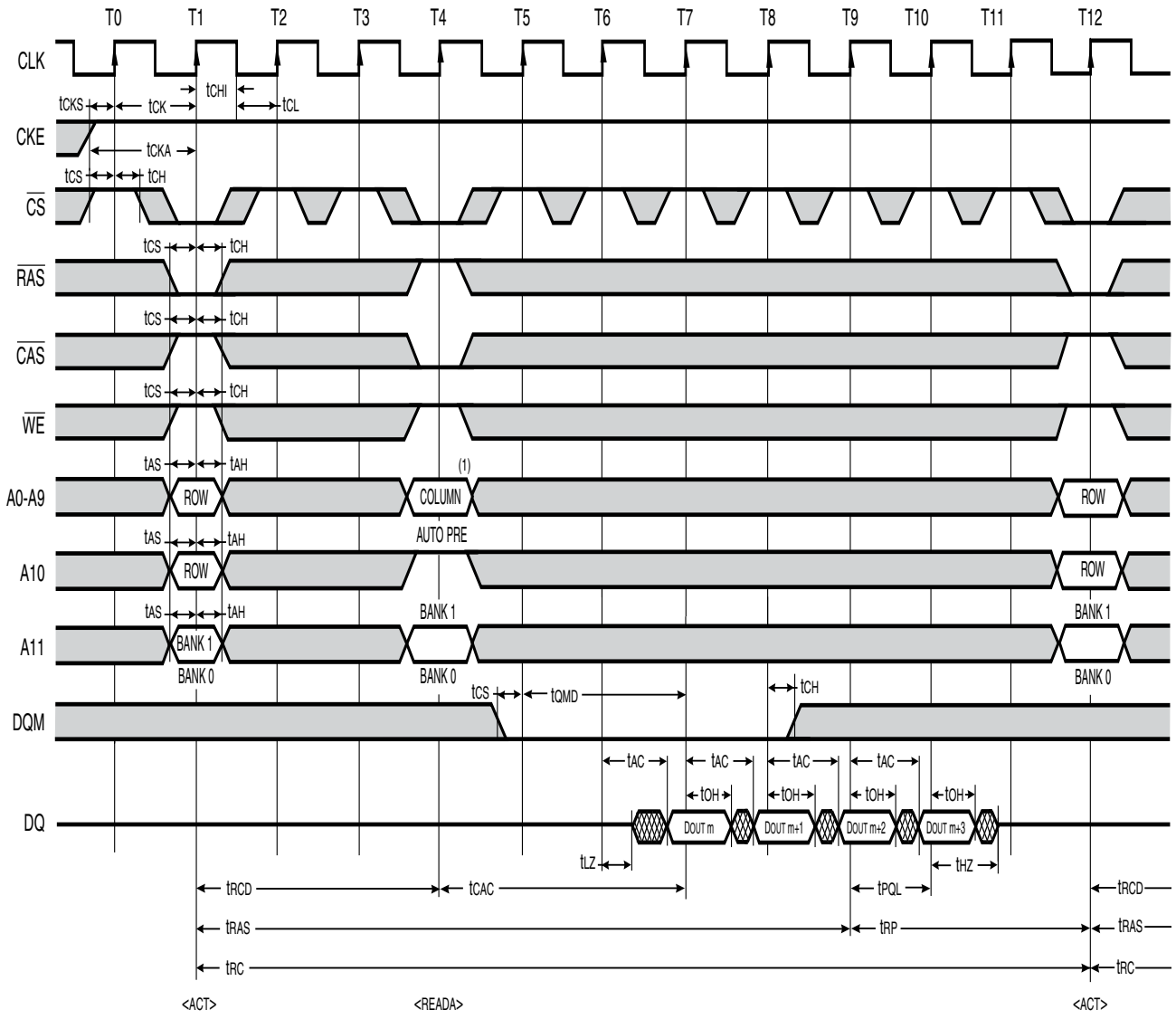
Read Cycle



CAS latency = 3, burst length = 4

Note 1: A8,A9 = Don't Care.

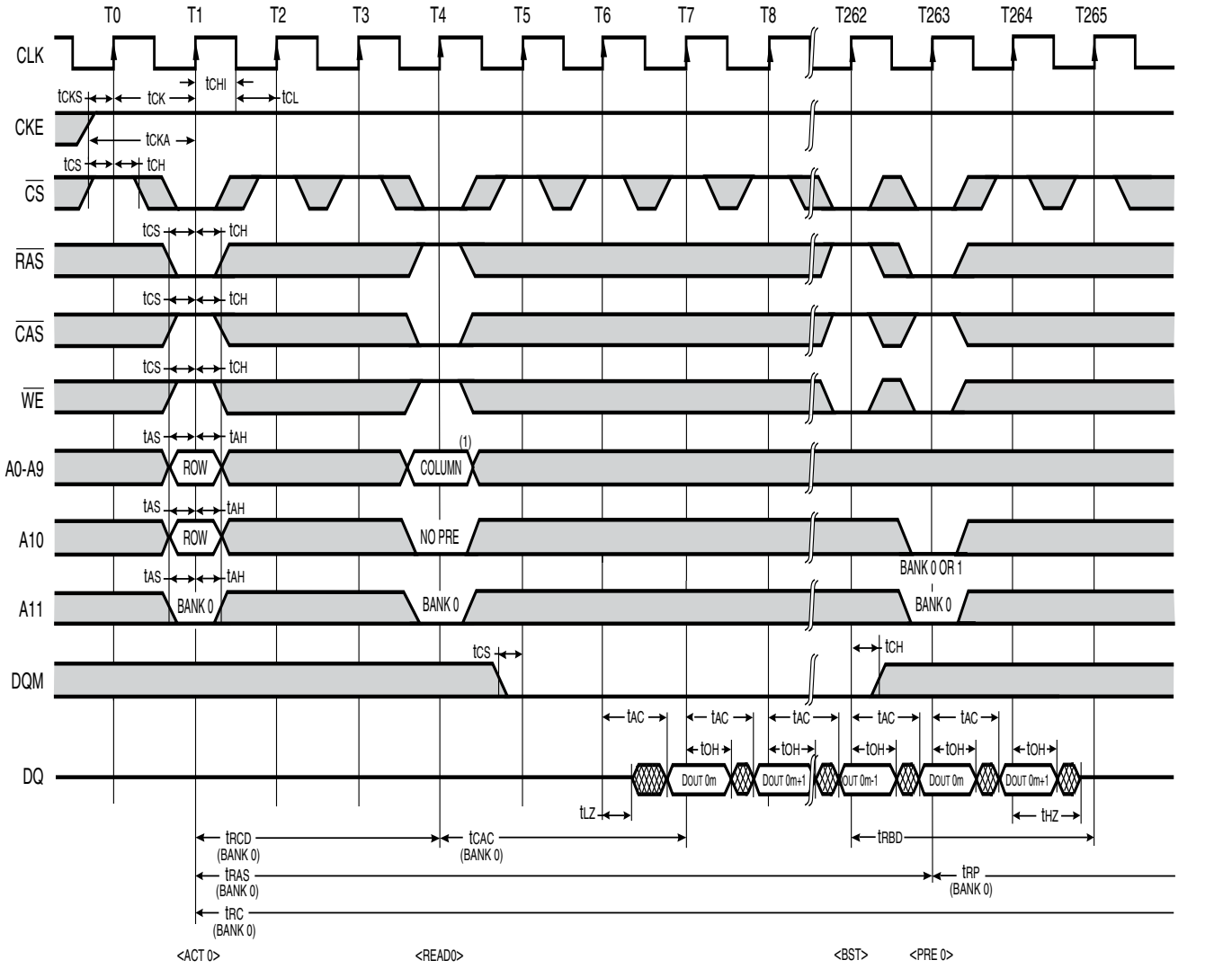
Read Cycle / Auto-Precharge



CAS latency = 3, burst length = 4

Note 1: A8,A9 = Don't Care.

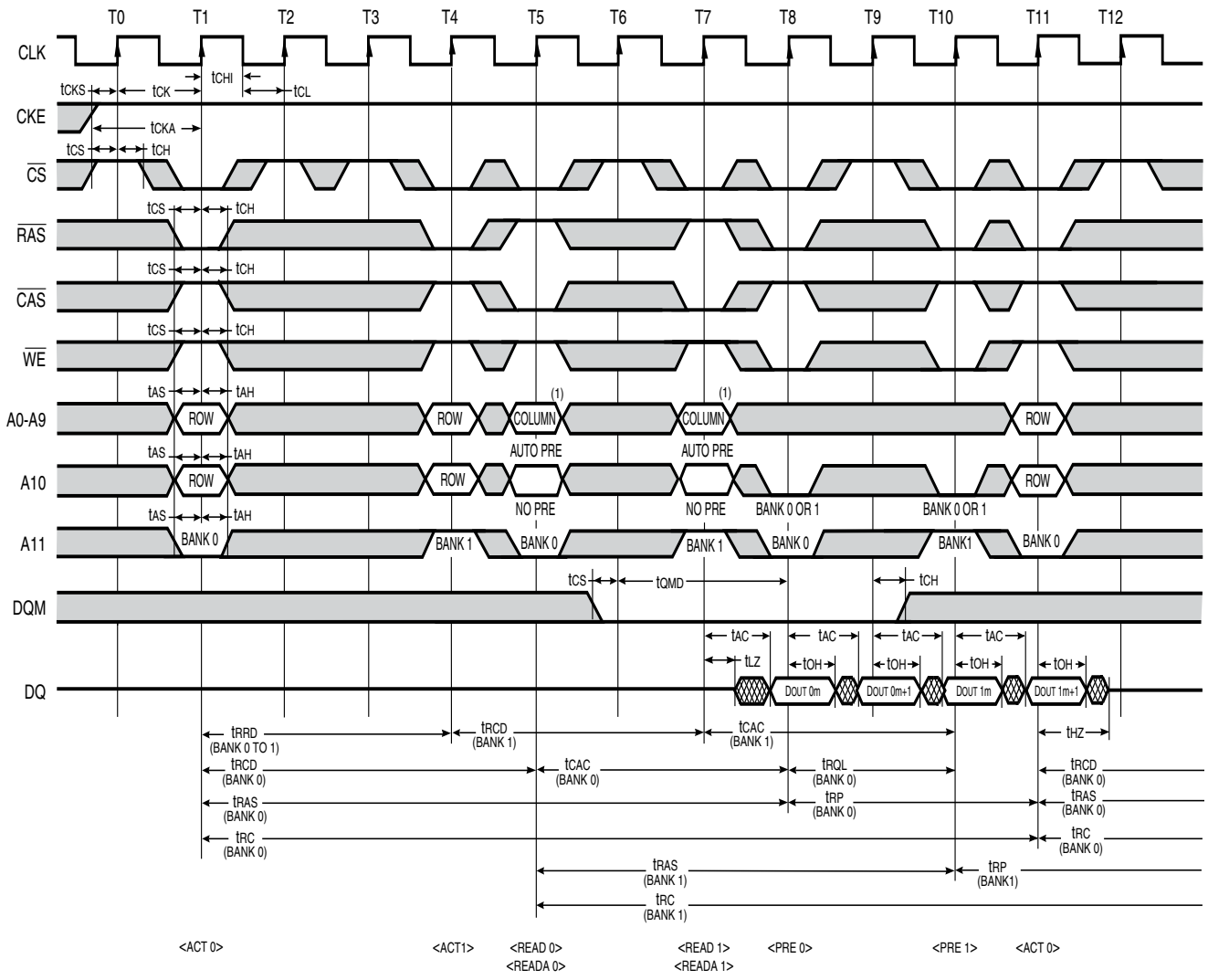
Read Cycle / Full Page



CAS latency = 3, burst length = full page

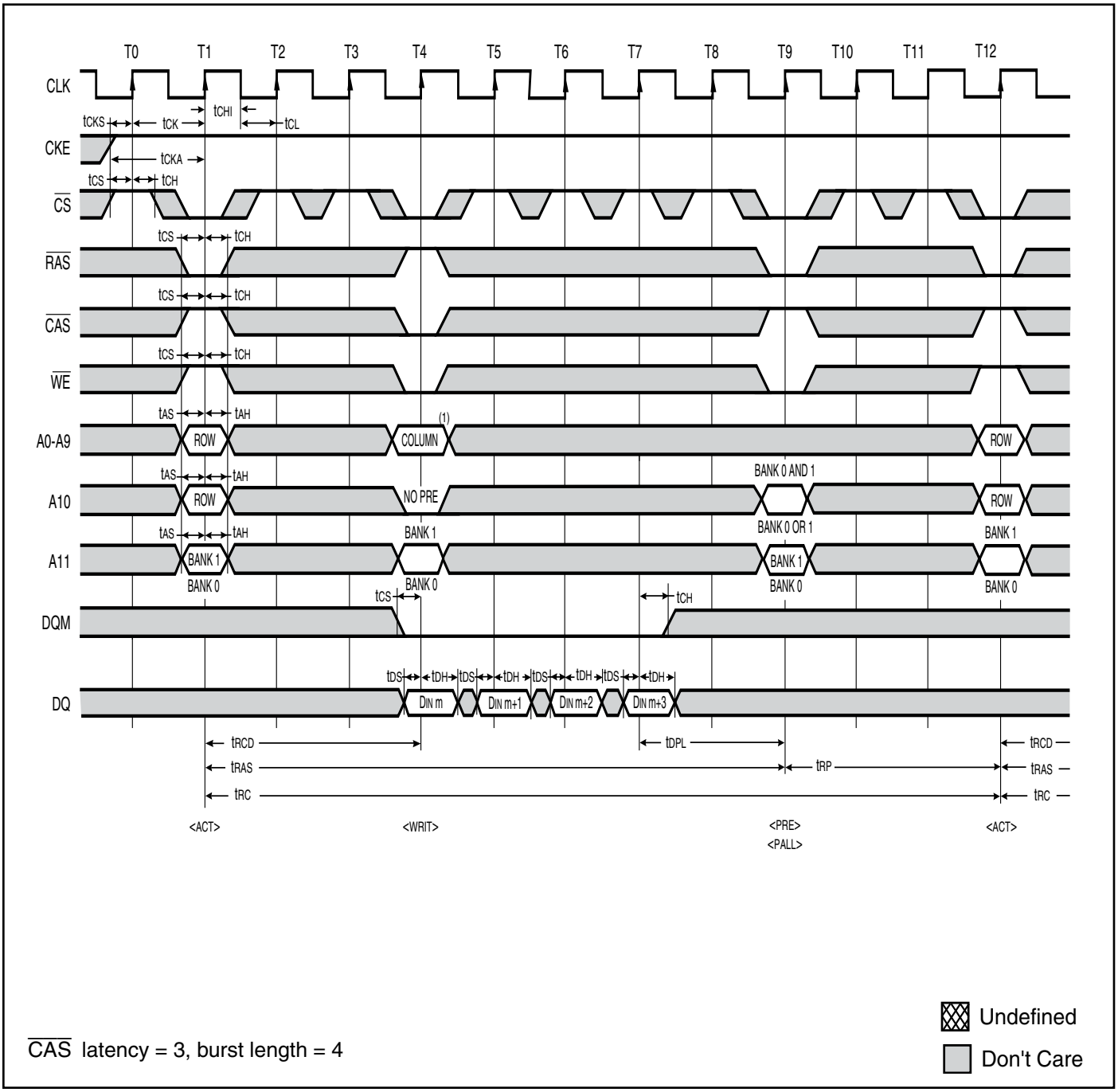
Note 1: A8,A9 = Don't Care.

Read Cycle / Ping Pong Operation (Bank Switching)



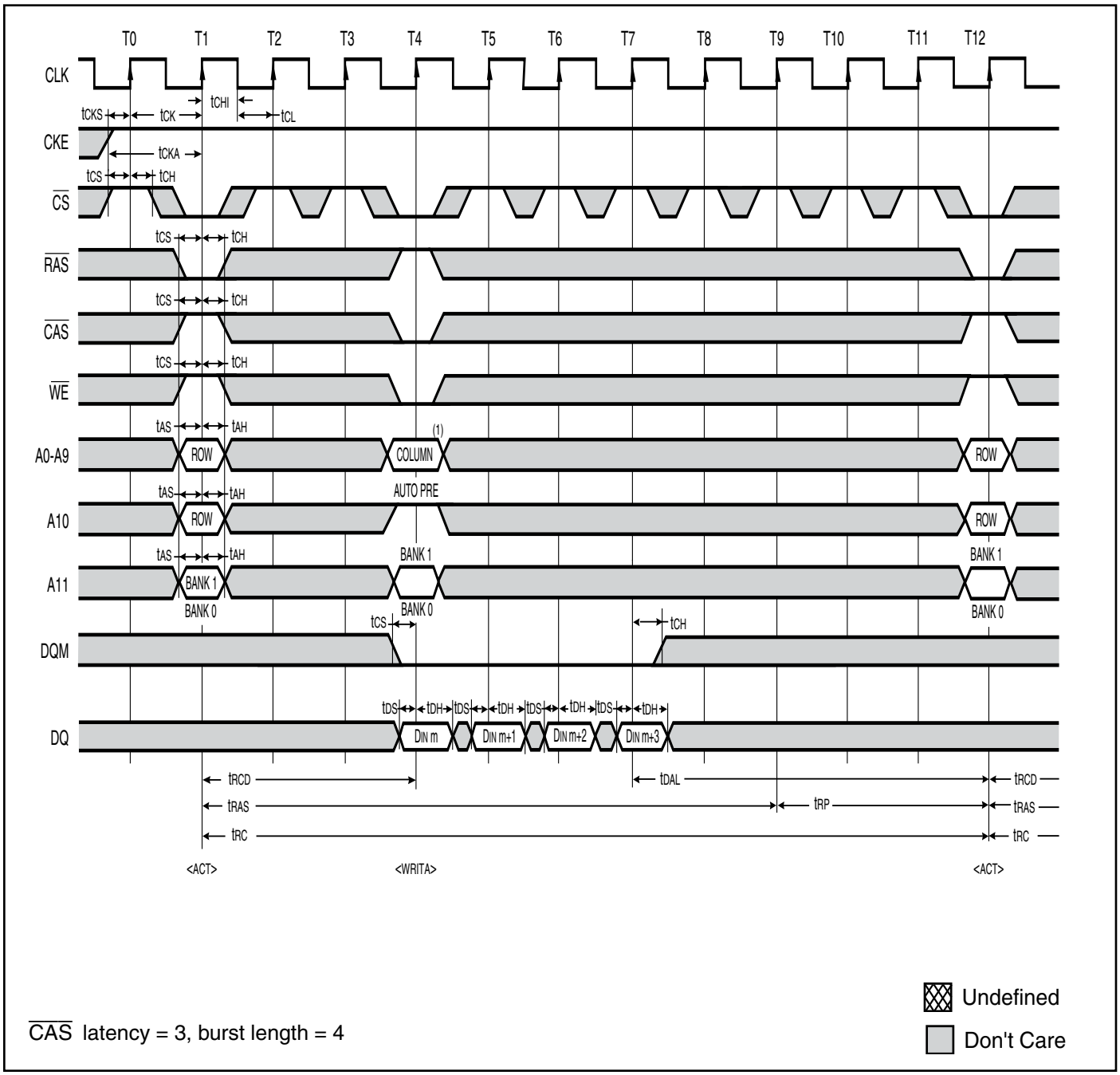
Note 1: A8,A9 = Don't Care.

Write Cycle



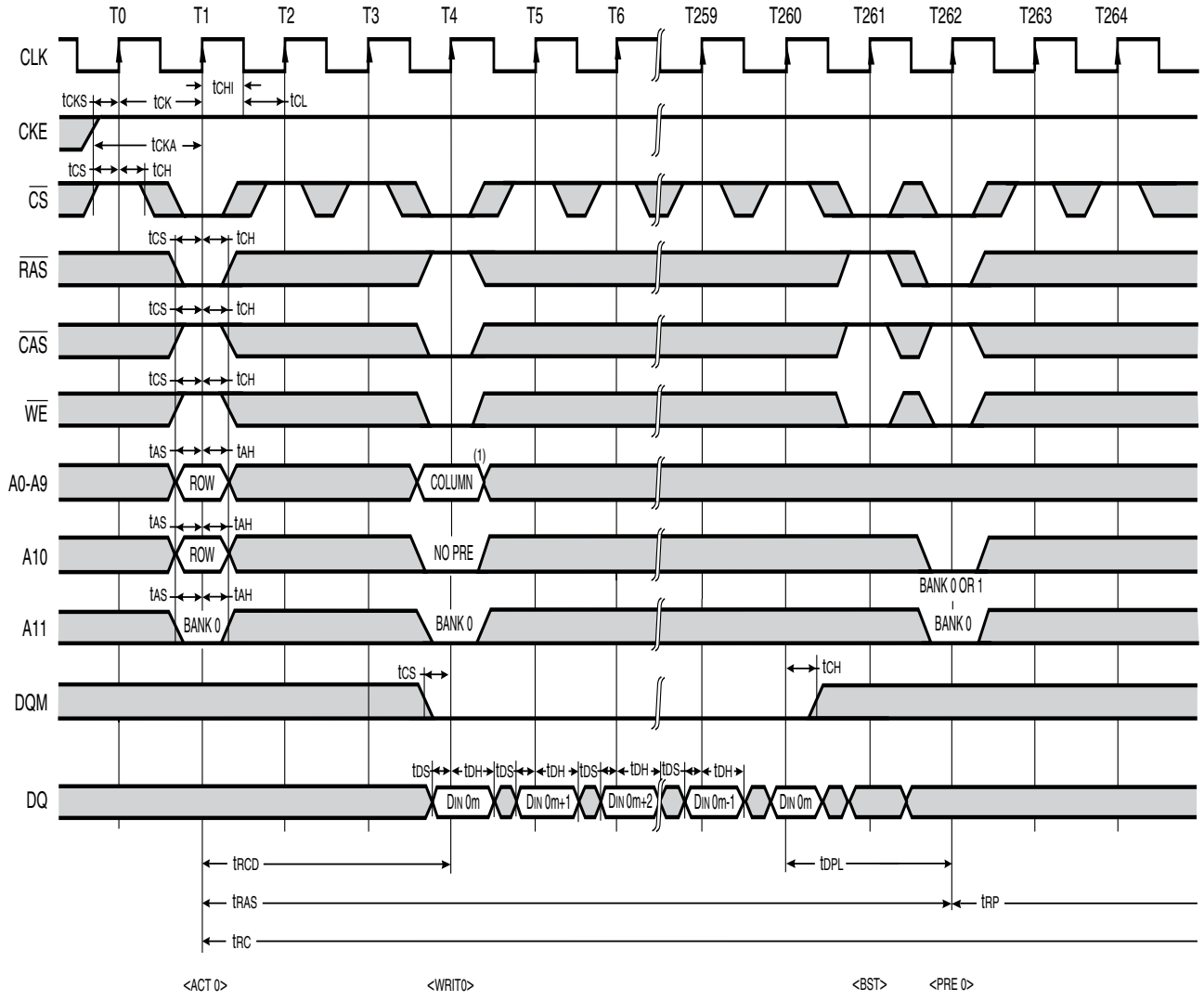
Note 1: A8,A9 = Don't Care.

Write Cycle / Auto-Precharge



Note 1: A8,A9 = Don't Care.

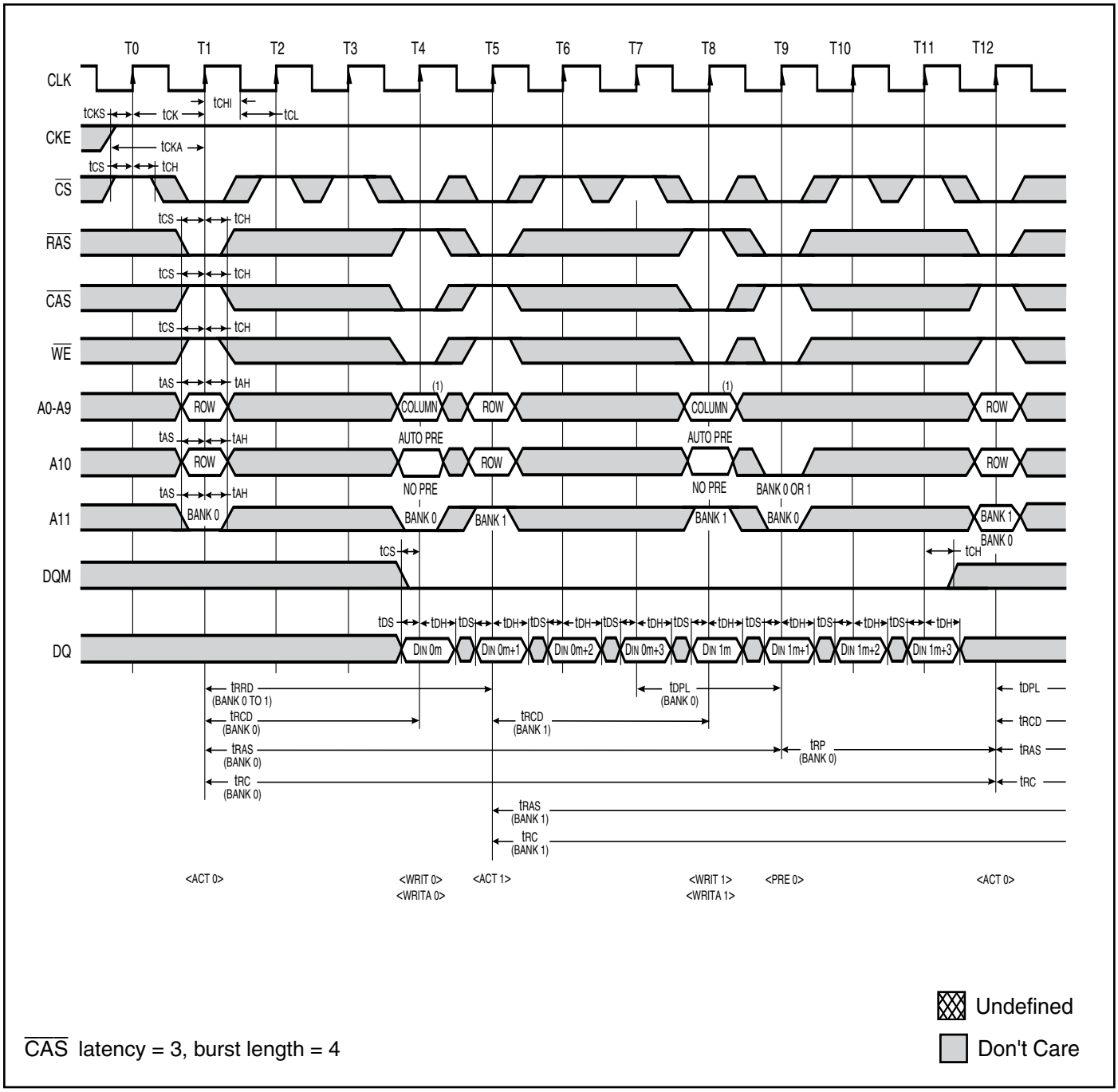
Write Cycle / Full Page



CAS latency = 3, burst length = full page

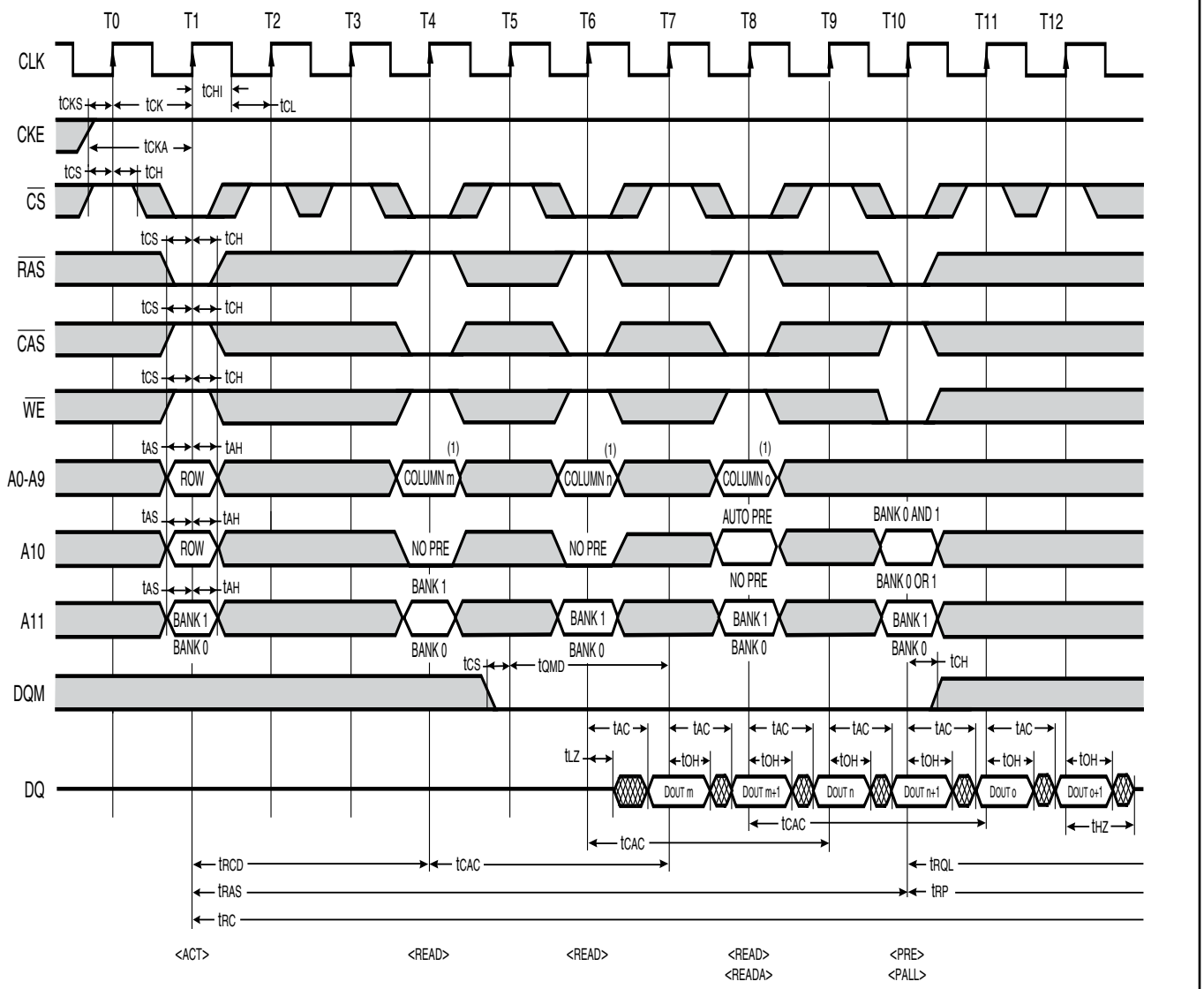
Note 1: A8,A9 = Don't Care.

Write Cycle / Ping-Pong Operation (Bank Switching)



Note 1: A8,A9 = Don't Care.

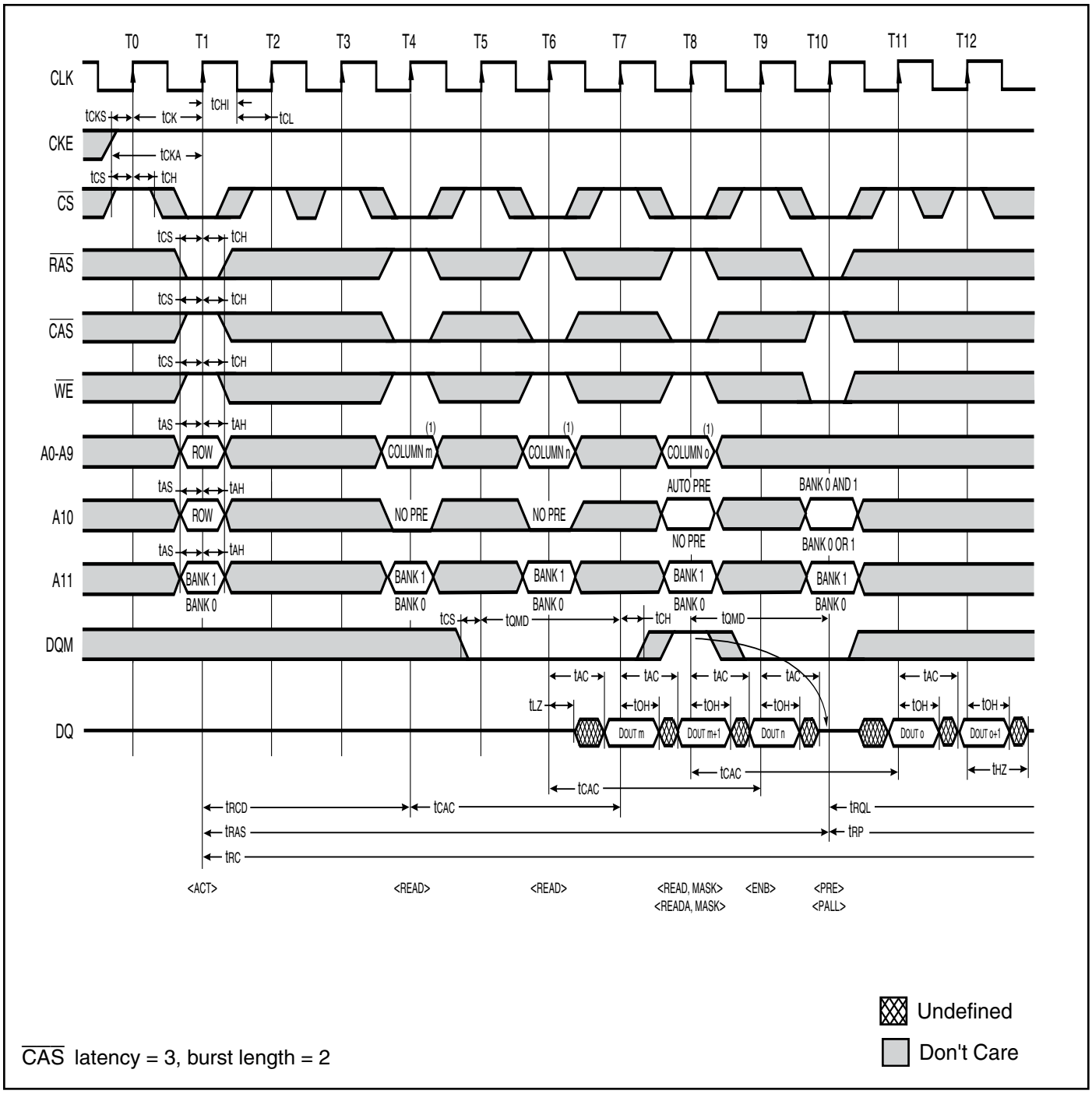
Read Cycle / Page Mode



CAS latency = 3, burst length = 2

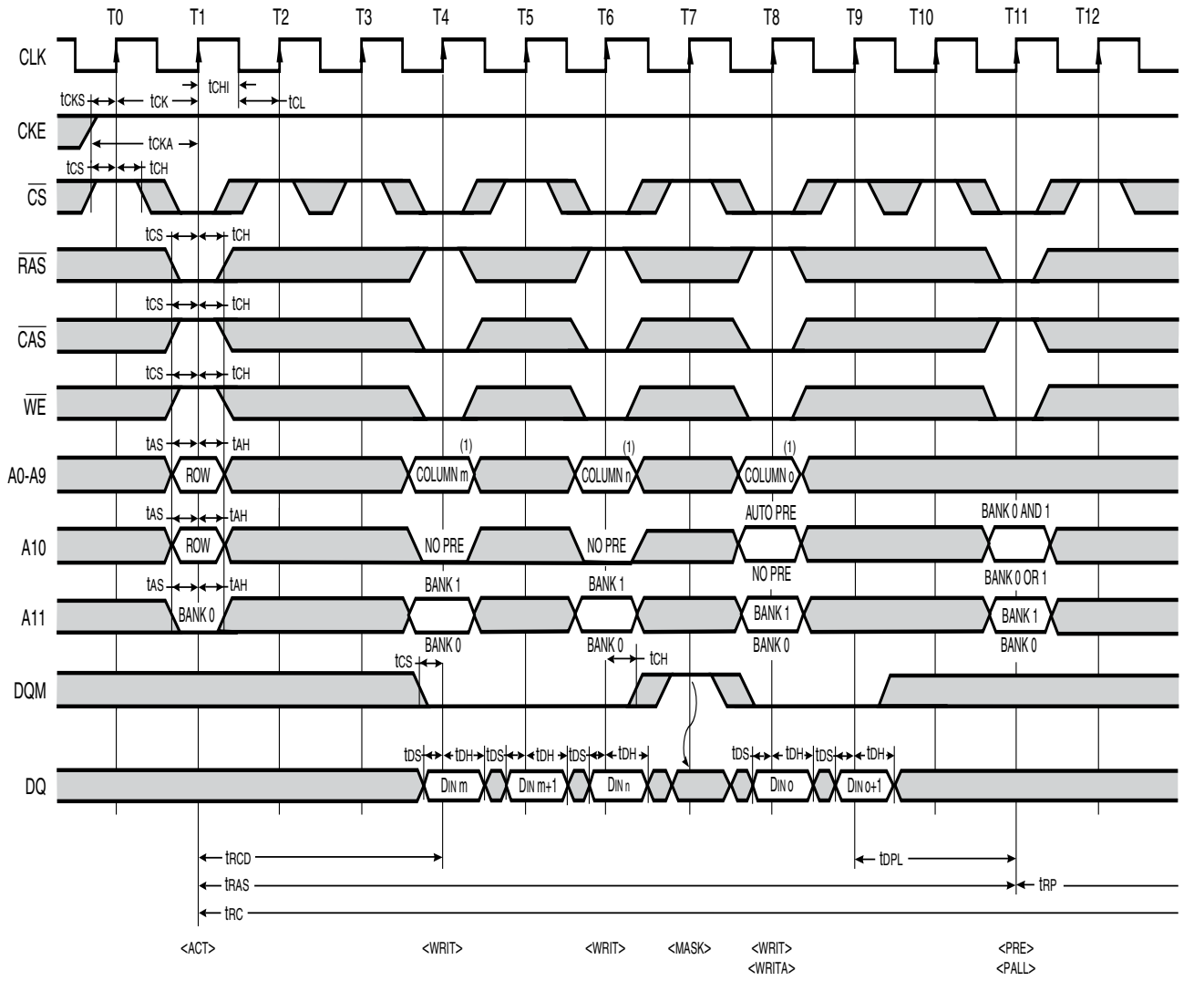
Note 1: A8,A9 = Don't Care.

Read Cycle / Page Mode; Data Masking



Note 1: A8,A9 = Don't Care.

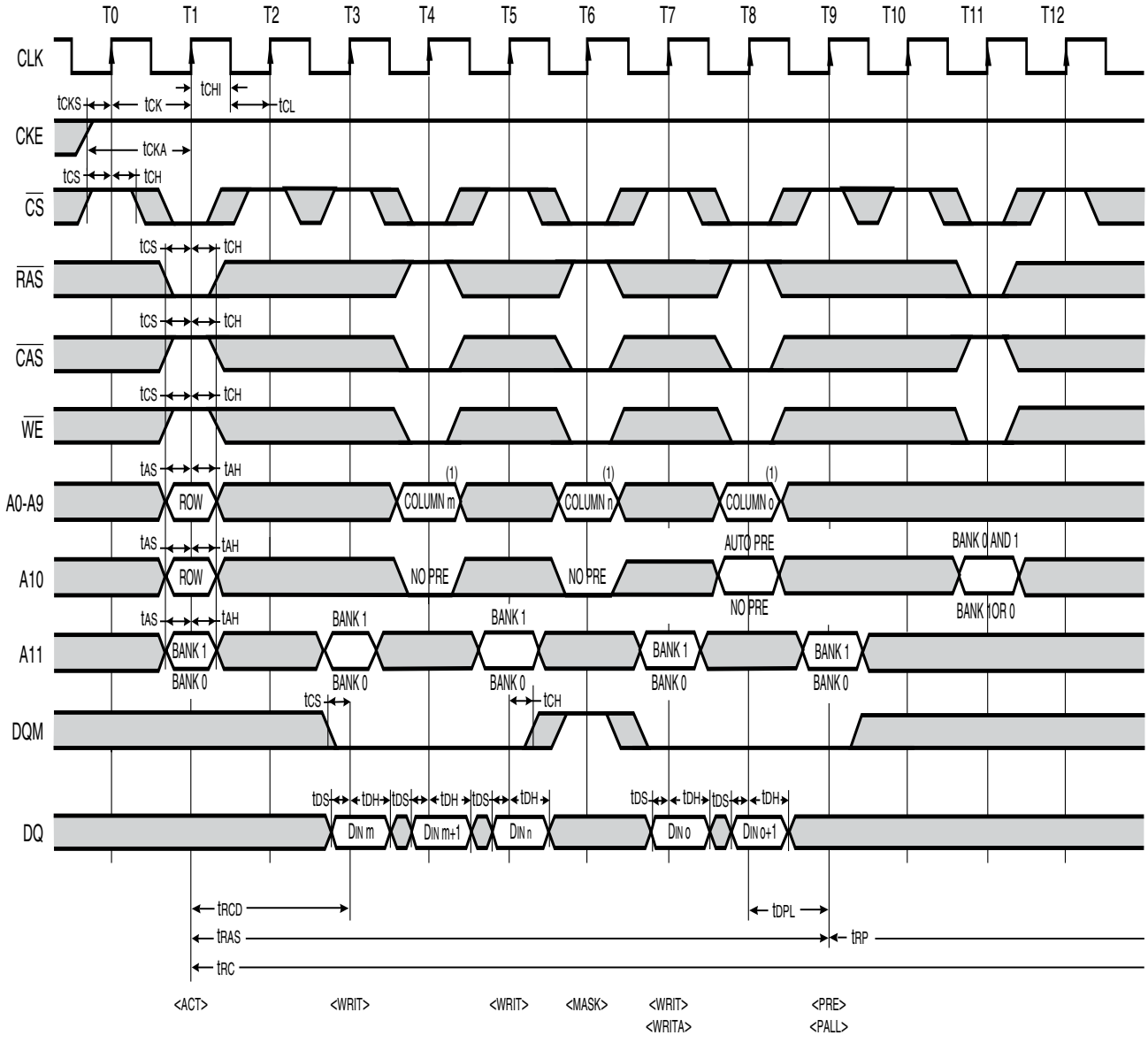
Write Cycle / Page Mode



CAS latency = 3, burst length = 2

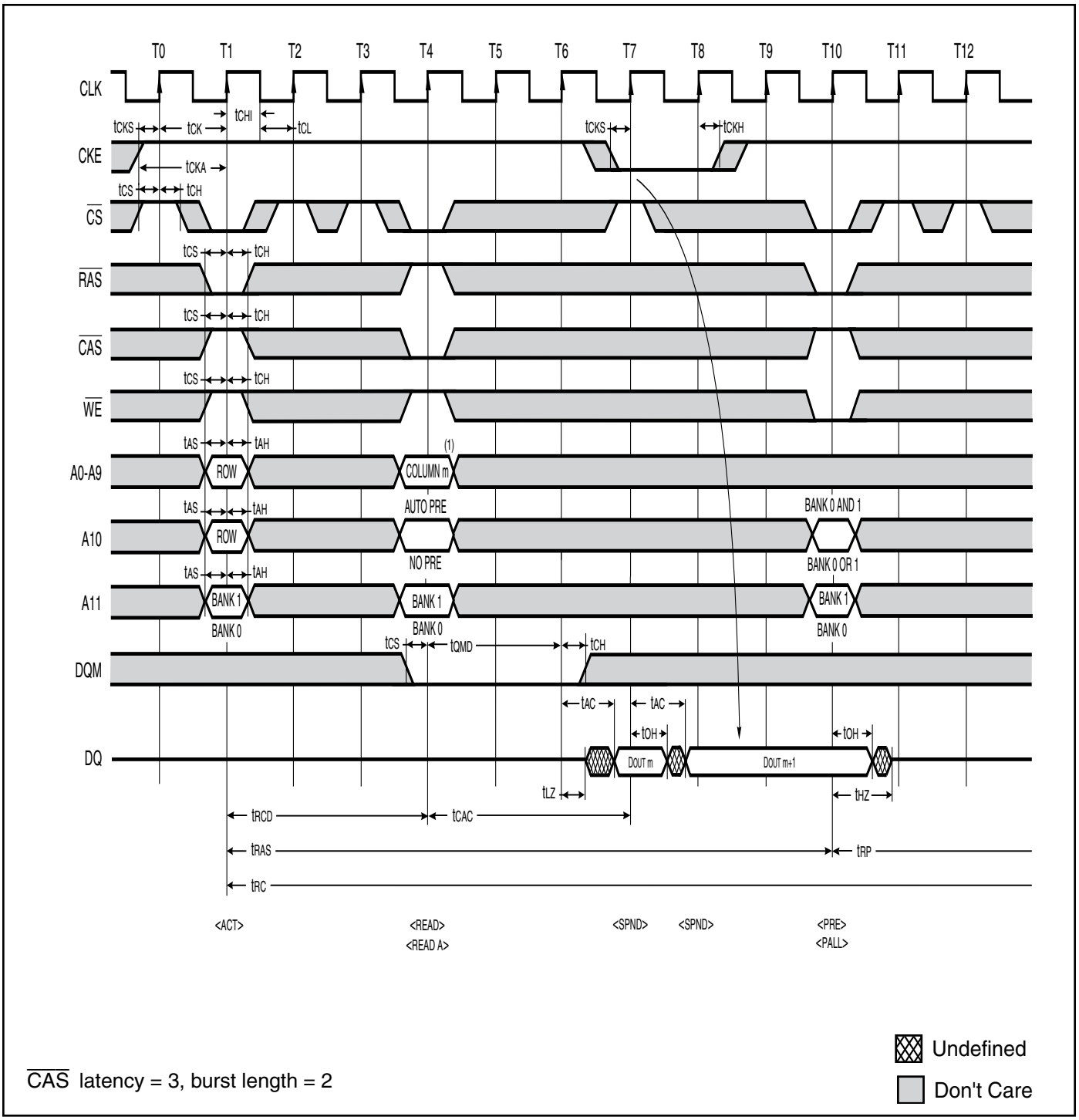
Note 1: A8,A9 = Don't Care.

Write Cycle / Page Mode; Data Masking



Note 1: A8,A9 = Don't Care.

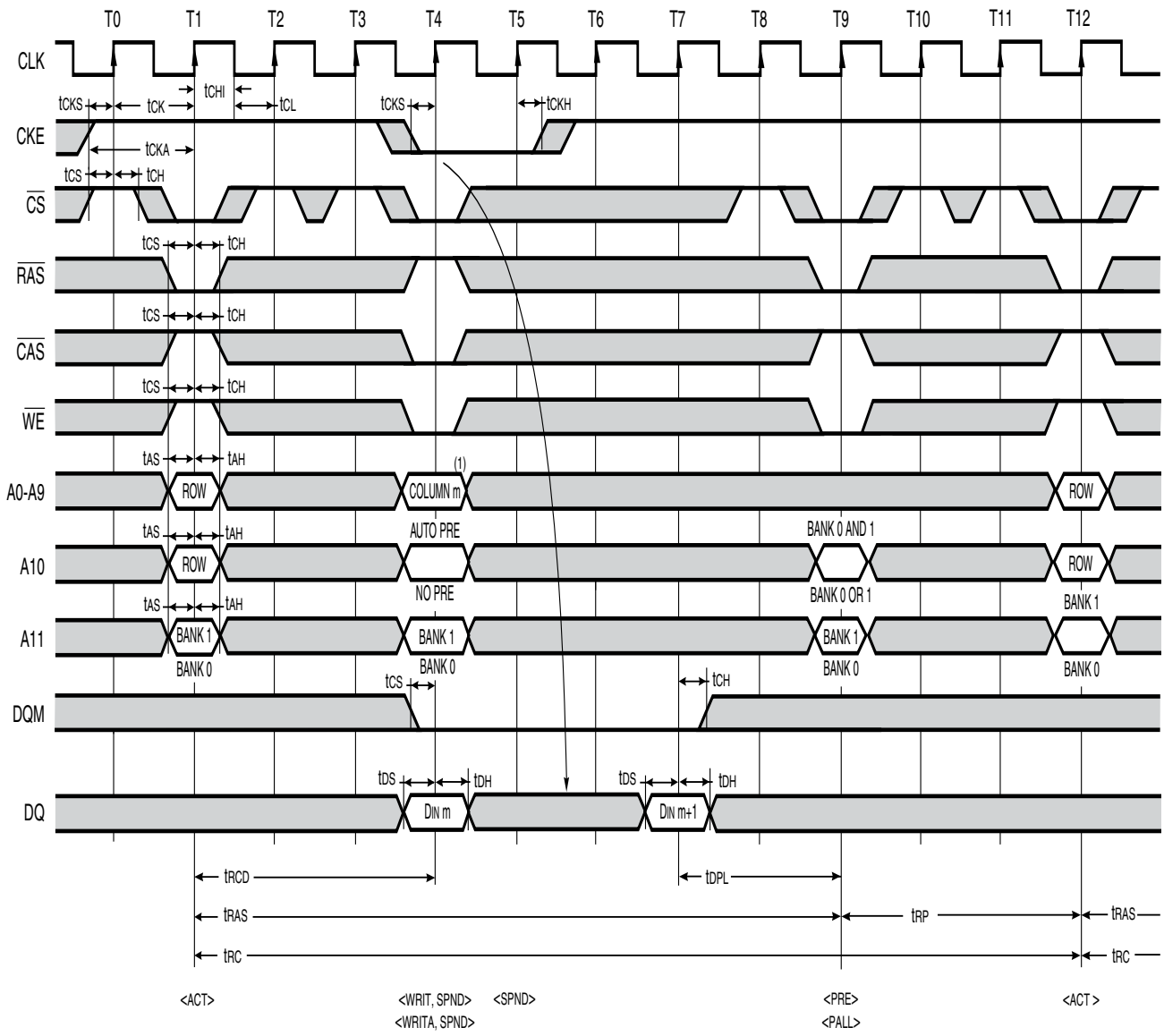
Read Cycle / Clock Suspend



$\overline{CAS}$ latency = 3, burst length = 2

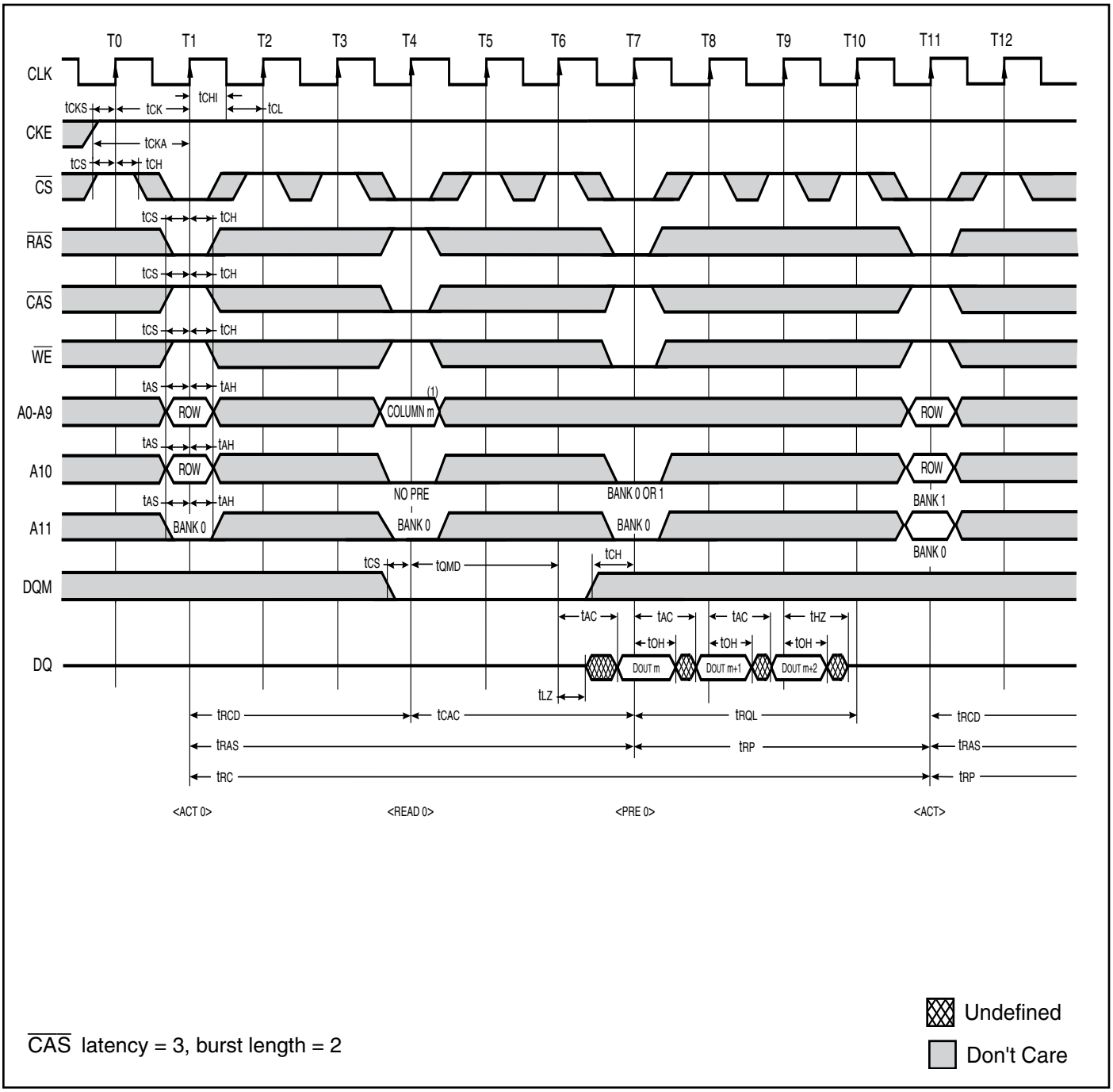
Note 1: A8,A9 = Don't Care.

Write Cycle / Clock Suspend



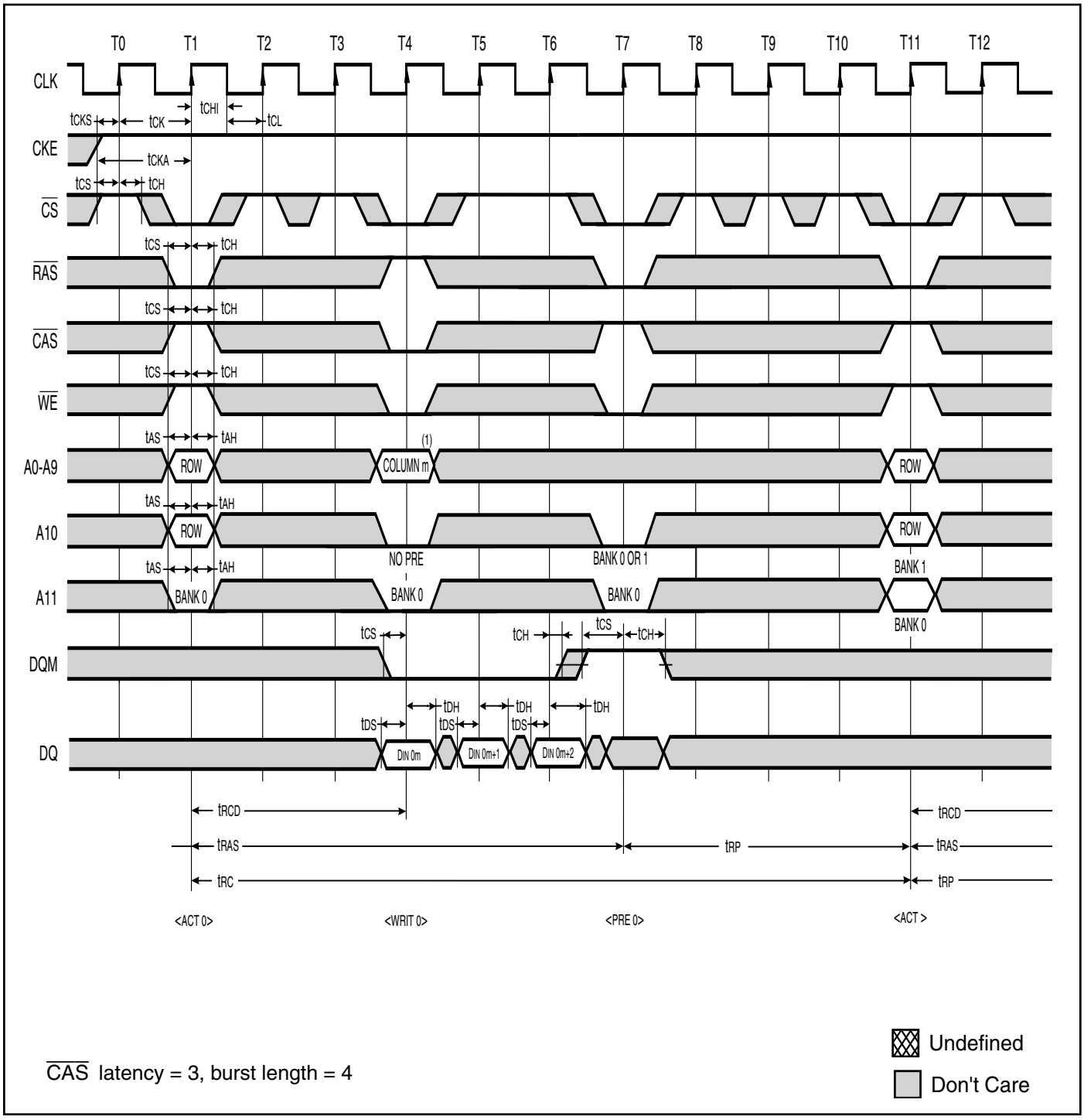
Note 1: A8,A9 = Don't Care.

Read Cycle / Precharge Termination



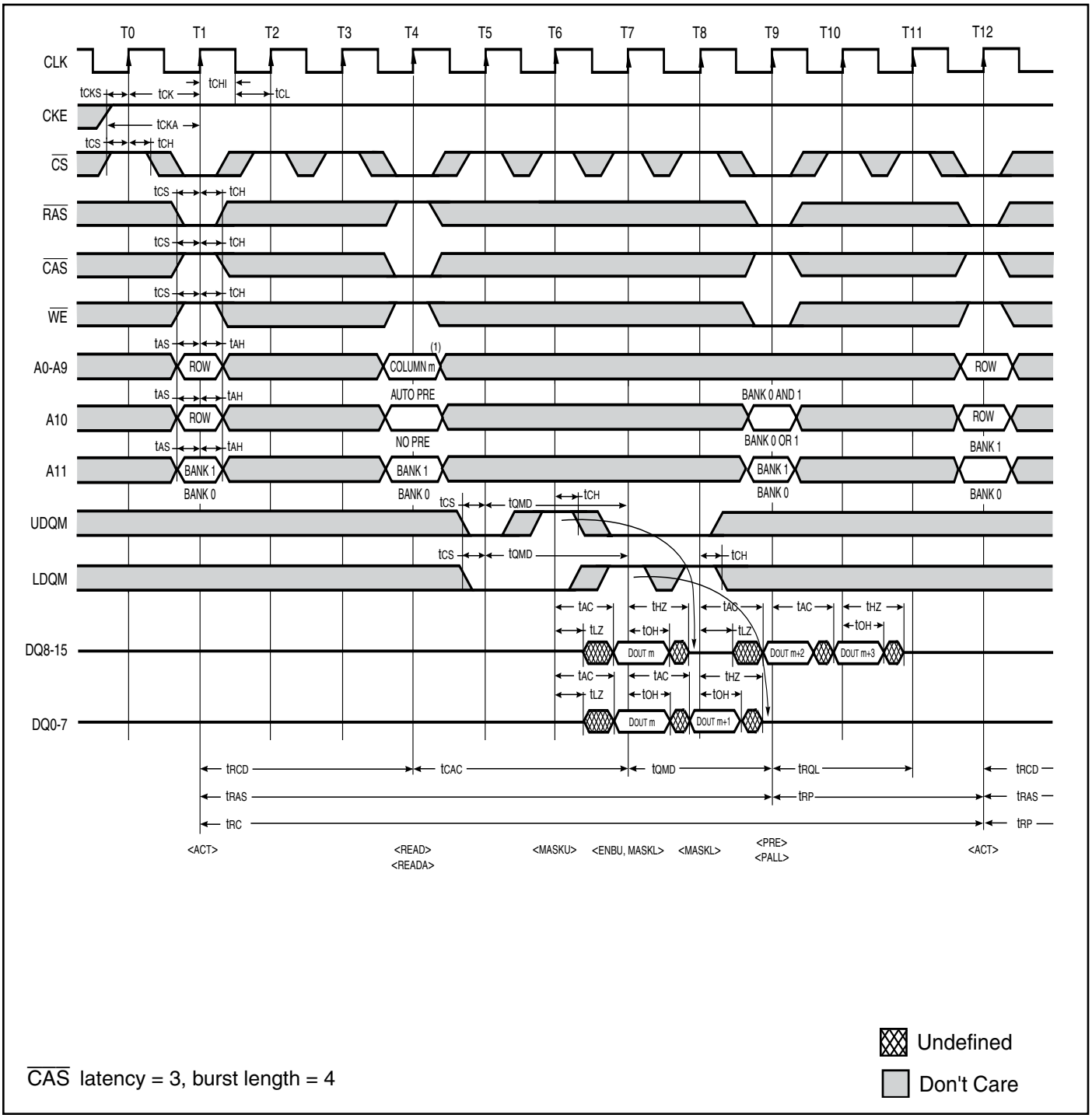
Note 1: A8,A9 = Don't Care.

Write Cycle / Precharge Termination



Note 1: A8,A9 = Don't Care.

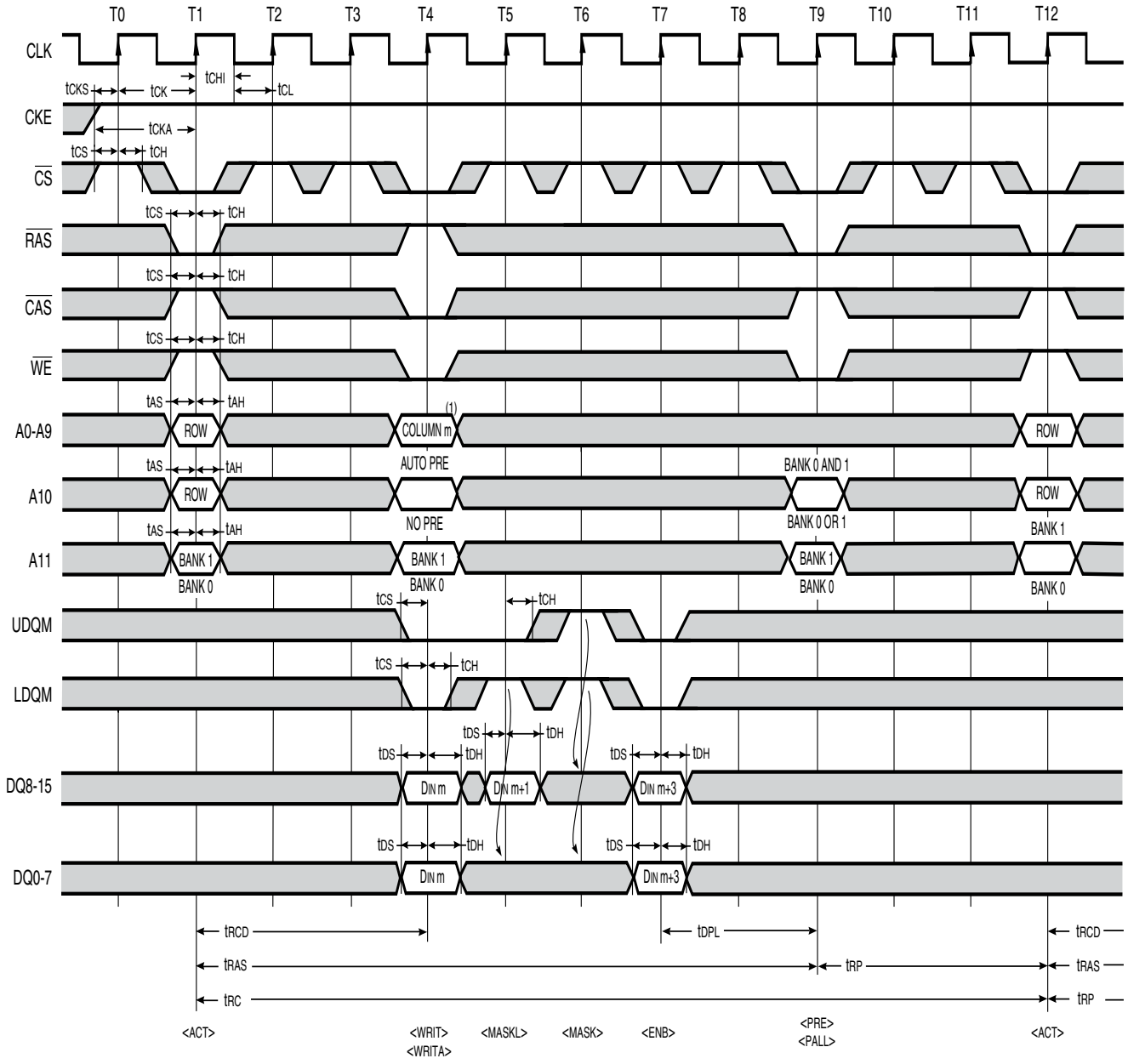
Read Cycle / Byte Operation



CAS latency = 3, burst length = 4

Note 1: A8,A9 = Don't Care.

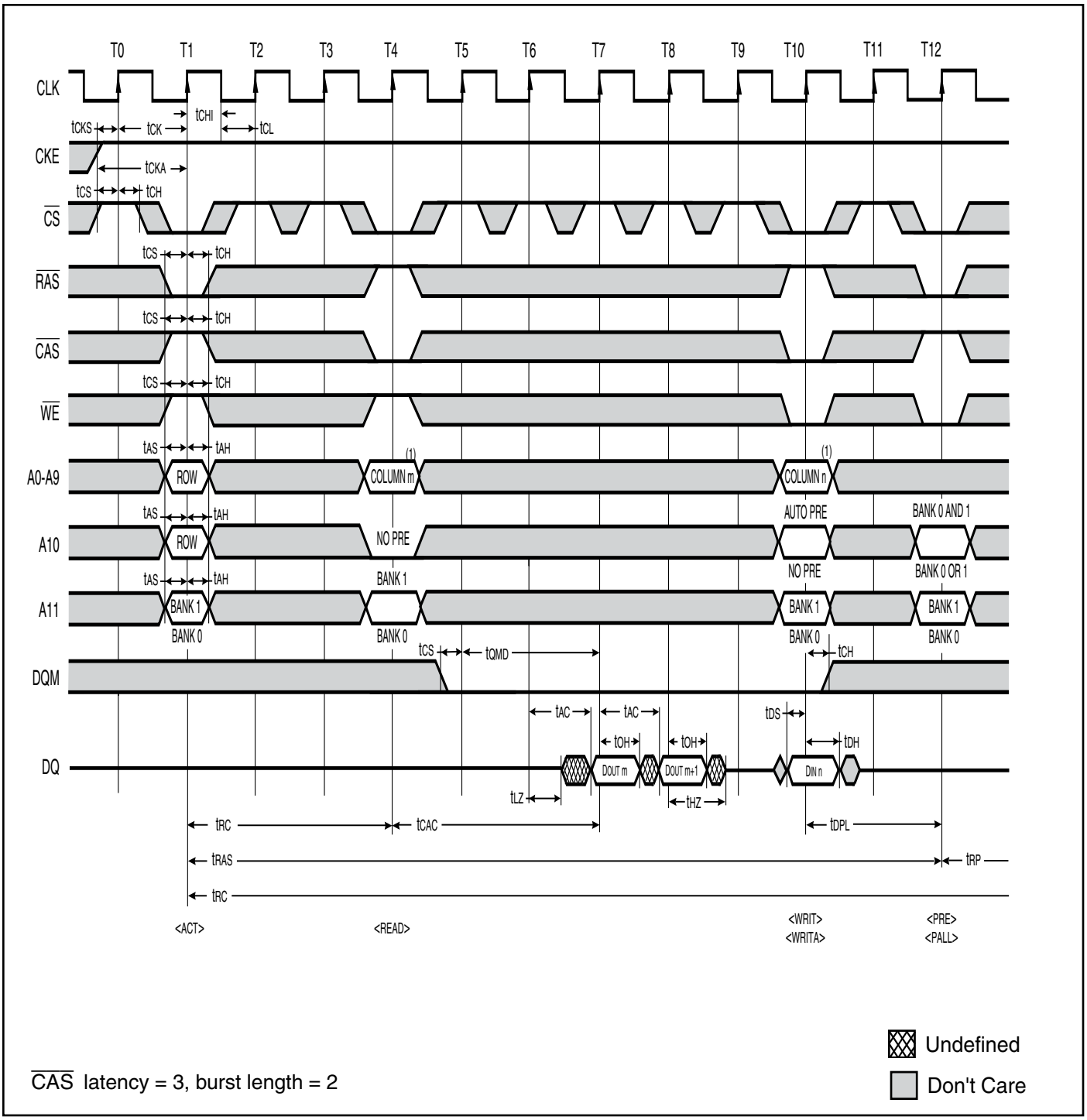
Write Cycle / Byte Operation



CAS latency = 3, burst length = 4

Note 1: A8,A9 = Don't Care.

Read Cycle, Write Cycle / Burst Read, Single Write



Note 1: A8,A9 = Don't Care.

ORDERING INFORMATION

Commercial Range: 0°C to 70°C

Frequency	Speed (ns)	Order Part No.	Package
200 MHz	5	IS42S16100H-5T	400-mil TSOP II
		IS42S16100H-5TL	400-mil TSOP II, Lead-free
		IS42S16100H-5BL	60-ball BGA, Lead-free
166 MHz	6	IS42S16100H-6T	400-mil TSOP II
		IS42S16100H-6TL	400-mil TSOP II, Lead-free
		IS42S16100H-6BL	60-ball BGA, Lead-free
143MHz	7	IS42S16100H-7T	400-mil TSOP II
		IS42S16100H-7TL	400-mil TSOP II, Lead-free
		IS42S16100H-7BL	60-ball BGA, Lead-free

Industrial Range: -40°C to +85°C

Frequency	Speed (ns)	Order Part No.	Package
166 MHz	6	IS42S16100H-6TLI	400-mil TSOP II, Lead-free
		IS42S16100H-6BLI	60-ball BGA, Lead-free
143MHz		IS42S16100H-7TLI	400-mil TSOP II, Lead-free
		IS42S16100H-7BLI	60-ball BGA, Lead-free

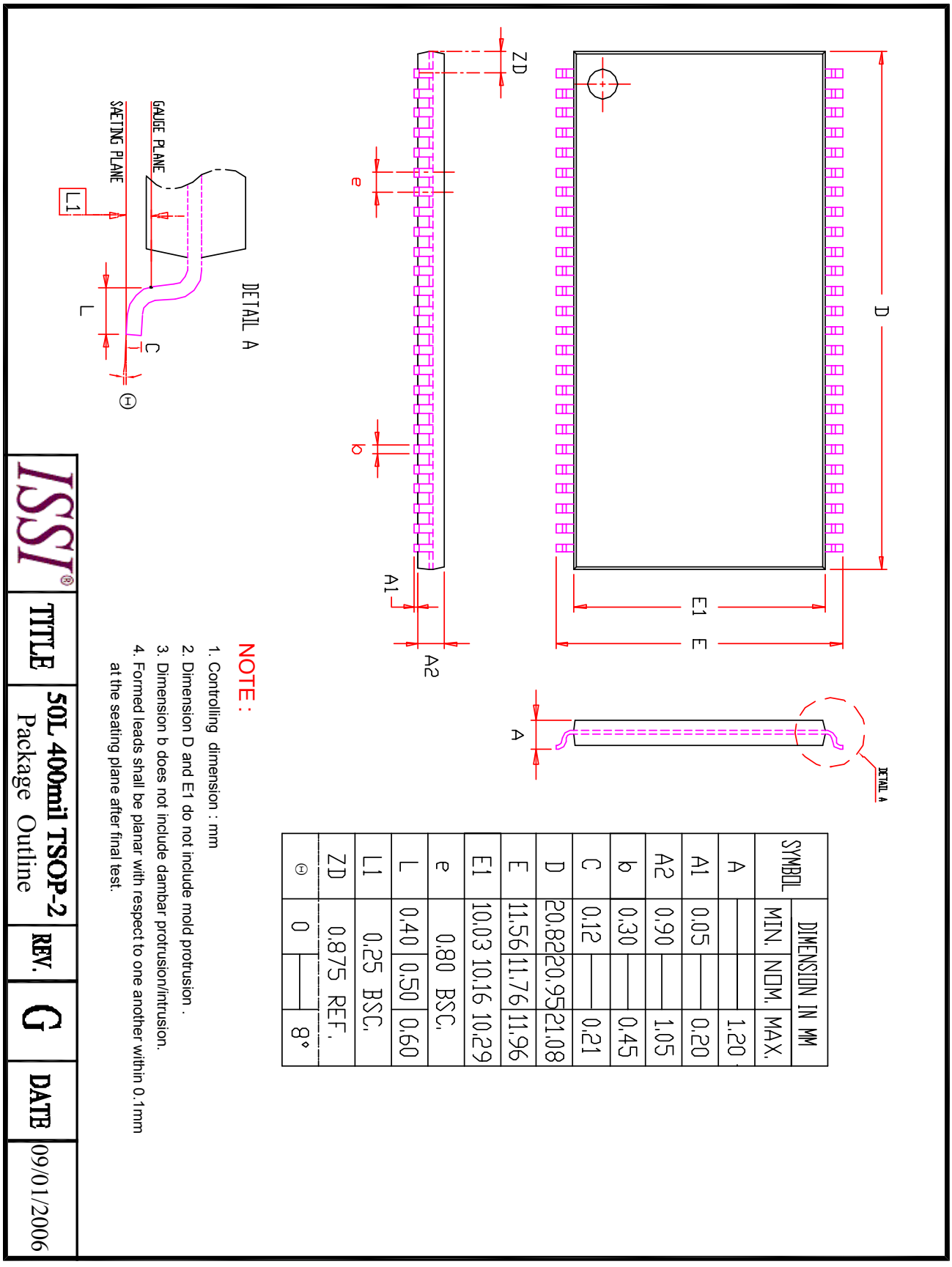
Please contact ISSI for leaded parts support.

Automotive Range: -40°C to +85°C

Frequency	Speed (ns)	Order Part No.	Package
166 MHz	6	IS45S16100H-6TLA1	400-mil TSOP II, Lead-free
		IS45S16100H-6BLAI	
143MHz	7	IS45S16100H-7TLA1	400-mil TSOP II, Lead-free
		IS45S16100H-7BLA1	60-ball BGA, Lead-free

Automotive Range: -40°C to +105°C

Frequency	Speed (ns)	Order Part No.	Package
143MHz	7	IS45S16100H-7TLA2	400-mil TSOP II, Lead-free
		IS45S16100H-7BLA2	60-ball BGA, Lead-free

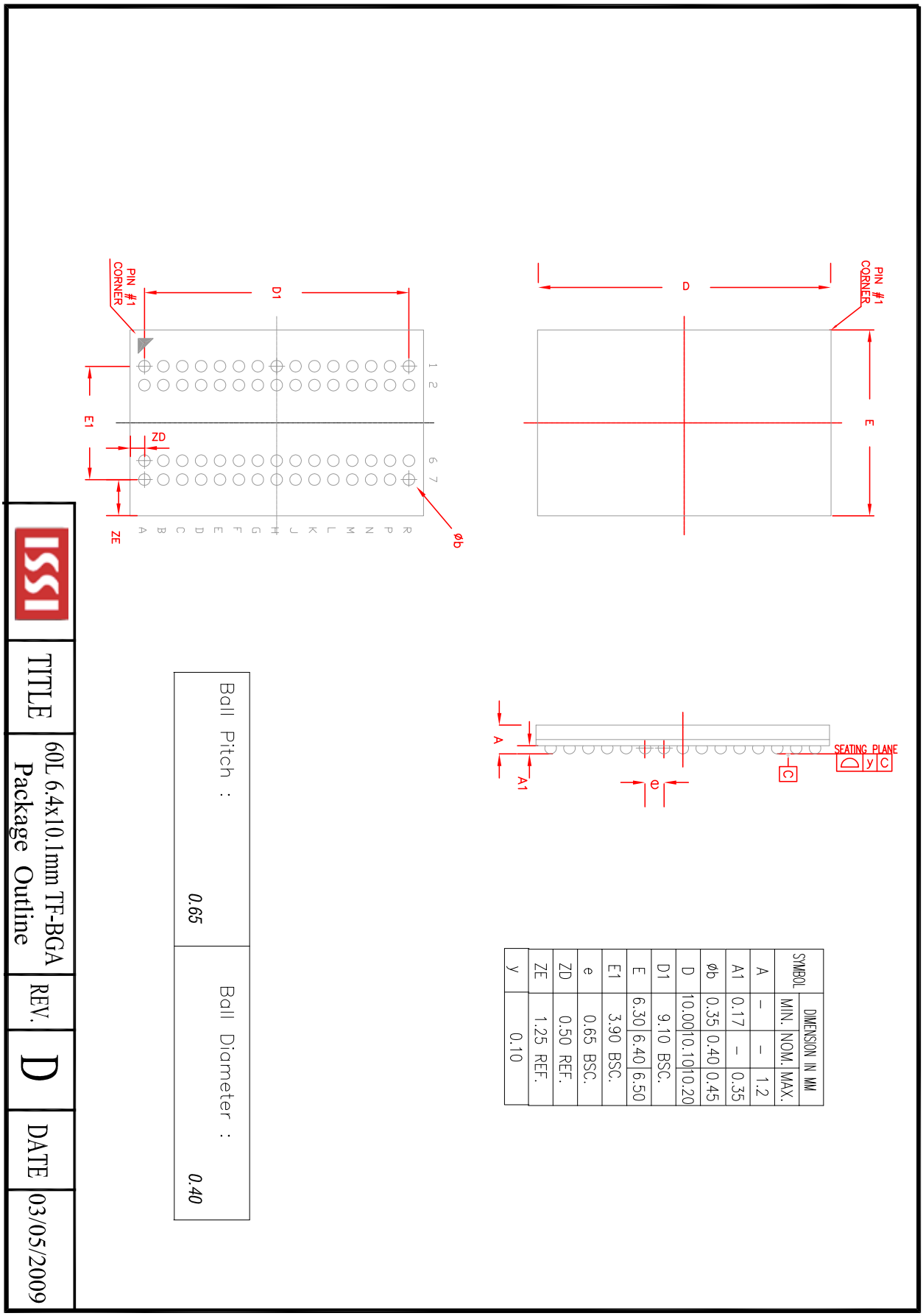


SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.05	---	0.20
A2	0.90	---	1.05
b	0.30	---	0.45
C	0.12	---	0.21
D	20.82	20.95	21.08
E	11.56	11.76	11.96
E1	10.03	10.16	10.29
e		0.80 BSC.	
L	0.40	0.50	0.60
L1		0.25 BSC.	
ZD		0.875 REF.	
θ	0	---	8°

NOTE :

1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

ISSI®	TITLE	50L 400mil TSOP-2 Package Outline	REV.	G	DATE	09/01/2006



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	–	–	1.2
A1	0.17	–	0.35
øb	0.35	0.40	0.45
D	10.00	10.10	10.20
D1	9.10 BSC.		
E	6.30	6.40	6.50
E1	3.90 BSC.		
e	0.65 BSC.		
ZD	0.50 REF.		
ZE	1.25 REF.		
y		0.10	

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