

# IS61C1024AL IS64C1024AL



## 128K x 8 HIGH-SPEED CMOS STATIC RAM

MAY 2012

### FEATURES

- High-speed access time: 12, 15 ns
- Low active power: 160 mW (typical)
- Low standby power: 1000  $\mu$ W (typical) CMOS standby
- Output Enable ( $\overline{OE}$ ) and two Chip Enable ( $\overline{CE1}$  and  $\overline{CE2}$ ) inputs for ease in applications
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V ( $\pm 10\%$ ) power supply
- Commercial, industrial, and automotive temperature ranges available
- Lead free available

### DESCRIPTION

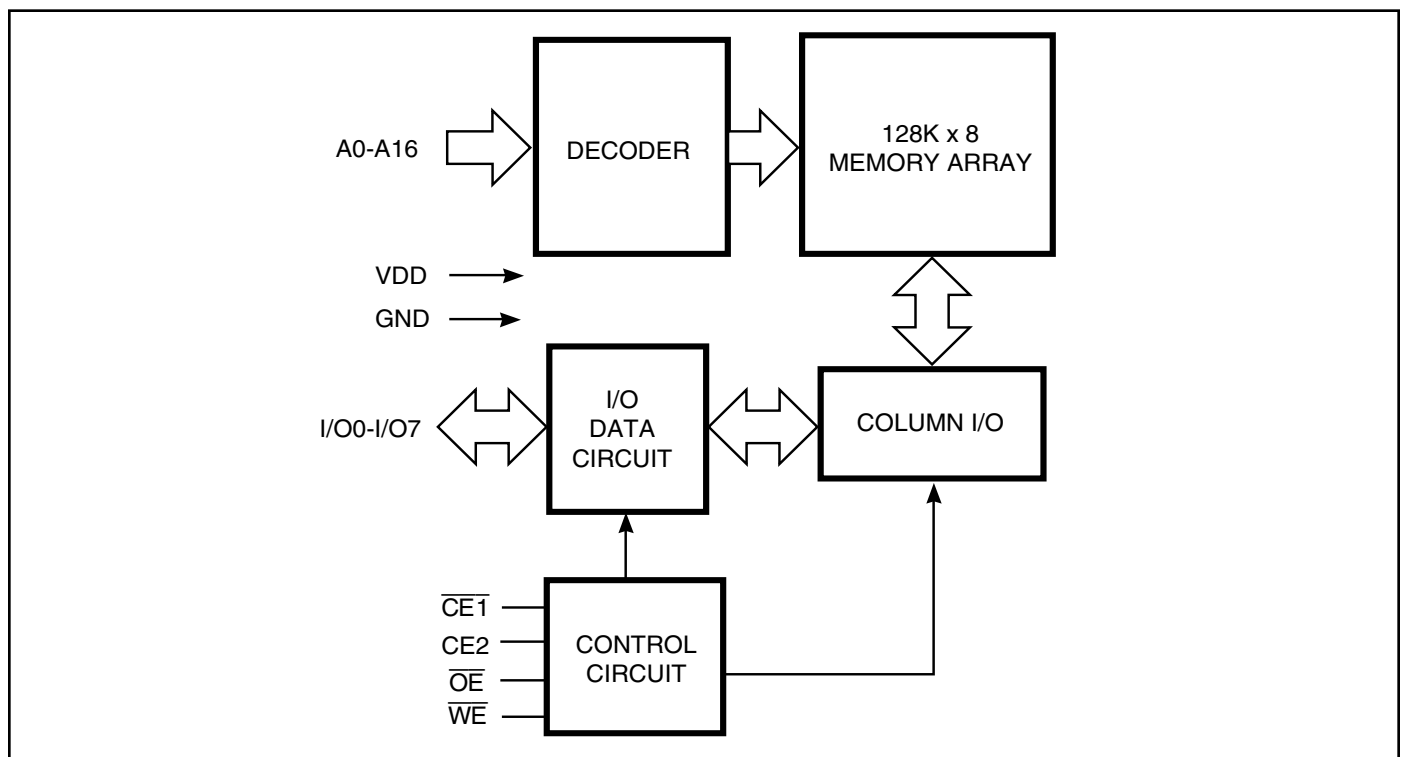
The *ISSI* IS61C1024AL/IS64C1024AL is a very high-speed, low power, 131,072-word by 8-bit CMOS static RAMs. They are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When  $\overline{CE1}$  is HIGH or  $\overline{CE2}$  is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

Easy memory expansion is provided by using two Chip Enable inputs,  $\overline{CE1}$  and  $\overline{CE2}$ . The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory.

The IS61C1024AL/IS64C1024AL is available in 32-pin 300-mil SOJ, 32-pin 400-mil SOJ, 32-pin TSOP (Type I, 8x20), and 32-pin sTSOP (Type I, 8 x 13.4) packages.

### FUNCTIONAL BLOCK DIAGRAM



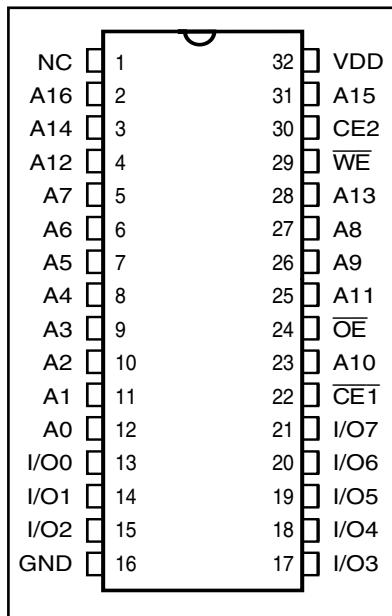
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- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

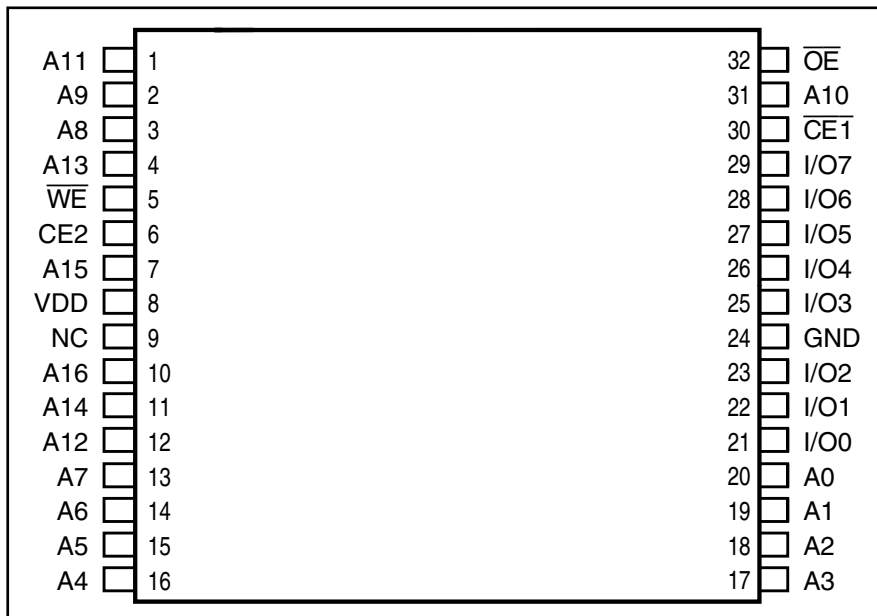
**PIN CONFIGURATION**

32-Pin SOJ



**PIN CONFIGURATION**

32-Pin TSOP (Type 1) (T) and sTSOP (Type 1) (H)



**PIN DESCRIPTIONS**

A0-A16	Address Inputs
$\overline{CE1}$	Chip Enable 1 Input
CE2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
VDD	Power
GND	Ground

**OPERATING RANGE (IS61C1024AL)**

Range	Ambient Temperature	VDD
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

**OPERATING RANGE (IS64C1024AL)**

Range	Ambient Temperature	VDD
Automotive	-40°C to +125°C	5V ± 10%

**TRUTH TABLE**

Mode	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{OE}$	I/O Operation	VDD Current
Not Selected	X	H	X	X	High-Z	ISB1, ISB2
(Power-down)	X	X	L	X	High-Z	ISB1, ISB2
Output Disabled	H	L	H	H	High-Z	Icc1, Icc2
Read	H	L	H	L	DOUT	Icc1, Icc2
Write	L	L	H	X	DIN	Icc1, Icc2

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.5	W
I <sub>OUT</sub>	DC Output Current (LOW)	20	mA

**Notes:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**CAPACITANCE<sup>(1,2)</sup>**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	7	pF

**Notes:**

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>DD</sub> = 5.0V.

**DC ELECTRICAL CHARACTERISTICS (Over Operating Range)**

Symbol	Parameter	Test Conditions	Min.	Max.	Unit	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DD</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4	—	V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>DD</sub> = Min., I <sub>OL</sub> = 8.0 mA	—	0.4	V	
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>DD</sub> + 0.5	V	
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V	
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	Com. Ind. Auto.	-1 -2 -5	1 2 5	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> Outputs Disabled	Com. Ind. Auto.	-1 -2 -5	1 2 5	μA

**Note:**

1. V<sub>IL</sub> = -3.0V for pulse width less than 10 ns.

**IS61C1024AL/IS64C1024AL POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Symbol	Parameter	Test Conditions		-12 ns		-15 ns		Unit
				Min.	Max.	Min.	Max.	
I <sub>CC1</sub>	V <sub>DD</sub> Operating Supply Current	V <sub>DD</sub> = V <sub>DD MAX.</sub> , $\overline{CE1} = V_{IL}$ I <sub>OUT</sub> = 0 mA, f = 0	Com.	—	35			mA
			Ind.	—	40			
			Auto.			—	45	
I <sub>CC2</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = V <sub>DD MAX.</sub> , $\overline{CE1} = V_{IL}$ I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com.	—	45			mA
			Ind.	—	50			
			Auto. typ. <sup>(2)</sup>	—	32	—	55	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = V <sub>DD MAX.</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CE1} \geq V_{IH}$ , f = 0 or CE2 ≤ V <sub>IL</sub> , f = 0	Com.	—	1			mA
			Ind.	—	1.5			
			Auto.			—	2	
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = V <sub>DD MAX.</sub> , $\overline{CE1} \geq V_{DD} - 0.2V$ , CE2 ≤ 0.2V V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Com.	—	400			μA
			Ind.	—	450			
			Auto. typ. <sup>(2)</sup>	—	200	—	500	

**Note:**

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical Values are measured at V<sub>DD</sub> = 5V, T<sub>A</sub> = 25°C and not 100% tested.

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)**

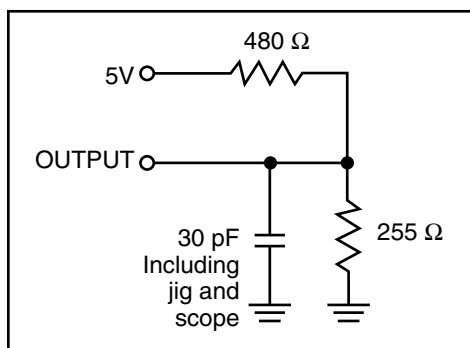
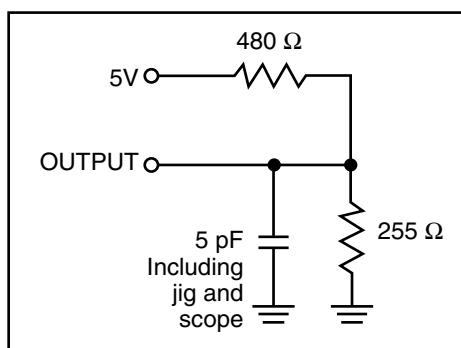
Symbol	Parameter	-12		-15		Unit
		Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	12	—	15	—	ns
t <sub>AA</sub>	Address Access Time	—	12	—	15	ns
t <sub>OHA</sub>	Output Hold Time	3	—	3	—	ns
t <sub>ACE1</sub>	$\overline{CE1}$ Access Time	—	12	—	15	ns
t <sub>ACE2</sub>	CE2 Access Time	—	12	—	15	ns
t <sub>DOE</sub>	$\overline{OE}$ Access Time	—	6	—	7	ns
t <sub>LZOE<sup>(2)</sup></sub>	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t <sub>HZOE<sup>(2)</sup></sub>	$\overline{OE}$ to High-Z Output	0	6	0	6	ns
t <sub>LZCE1<sup>(2)</sup></sub>	$\overline{CE1}$ to Low-Z Output	2	—	2	—	ns
t <sub>LZCE2<sup>(2)</sup></sub>	CE2 to Low-Z Output	2	—	2	—	ns
t <sub>HZCE<sup>(2)</sup></sub>	$\overline{CE1}$ or CE2 to High-Z Output	0	7	0	8	ns
t <sub>PU<sup>(3)</sup></sub>	$\overline{CE1}$ or CE2 to Power-Up	0	—	0	—	ns
t <sub>PD<sup>(3)</sup></sub>	$\overline{CE1}$ or CE2 to Power-Down	—	12	—	12	ns

**Notes:**

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

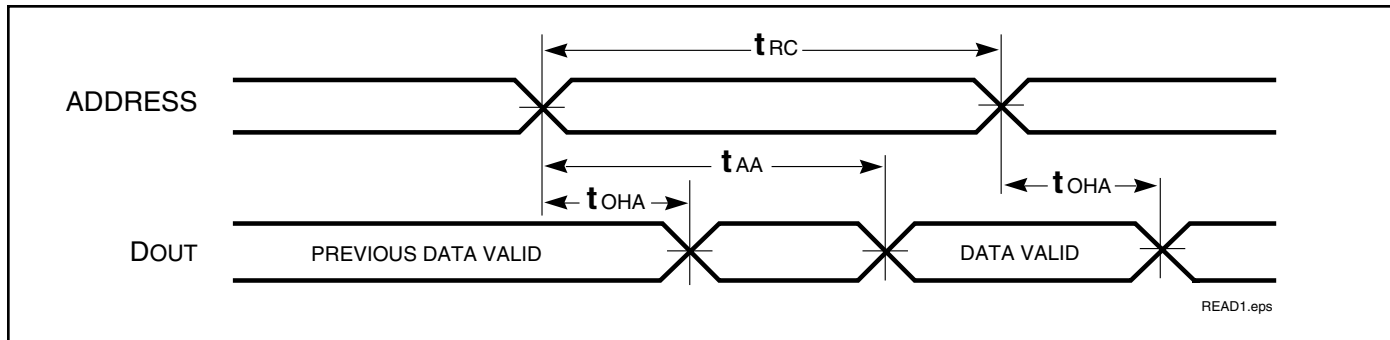
**AC TEST CONDITIONS**

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

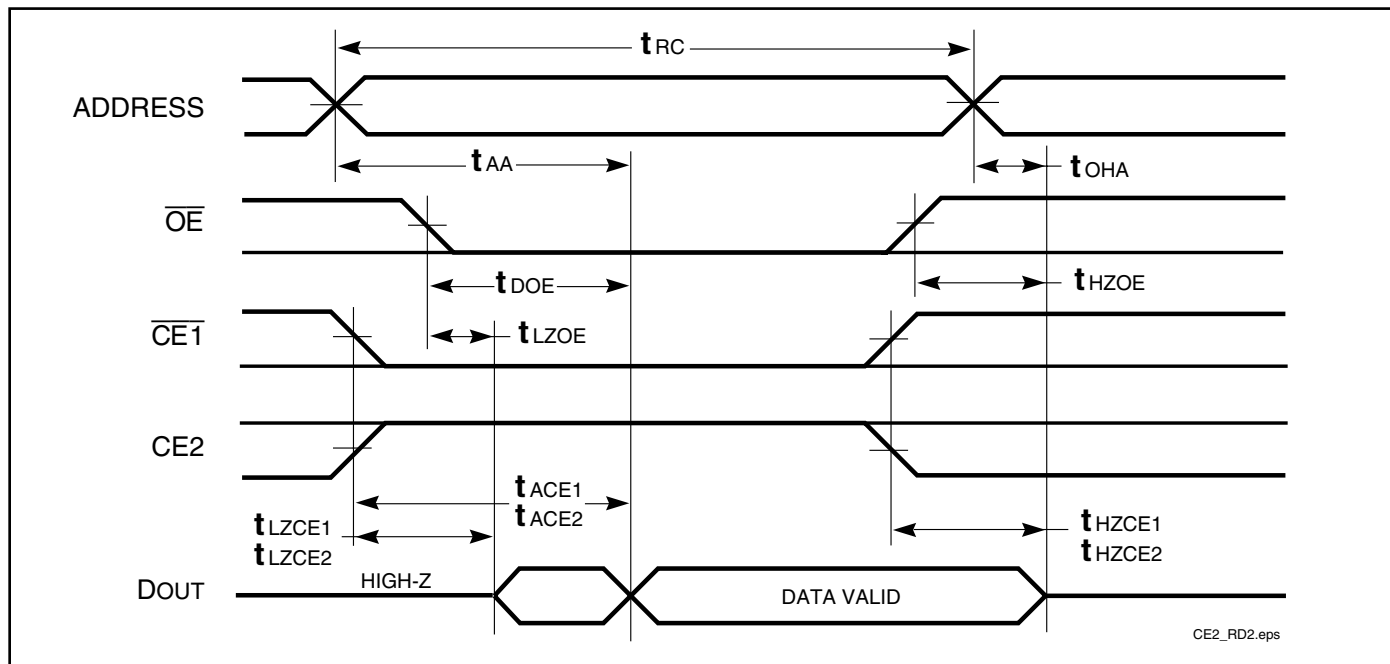
**AC TEST LOADS**

**Figure 1**

**Figure 2**

AC WAVEFORMS

READ CYCLE NO. 1<sup>(1,2)</sup>



READ CYCLE NO. 2<sup>(1,3)</sup>



Notes:

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE1} = V_{IL}$ ,  $CE2 = V_{IH}$ .
3. Address is valid prior to or coincident with  $\overline{CE1}$  LOW and CE2 HIGH transitions.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup>** (Over Operating Range, Standard and Low Power)

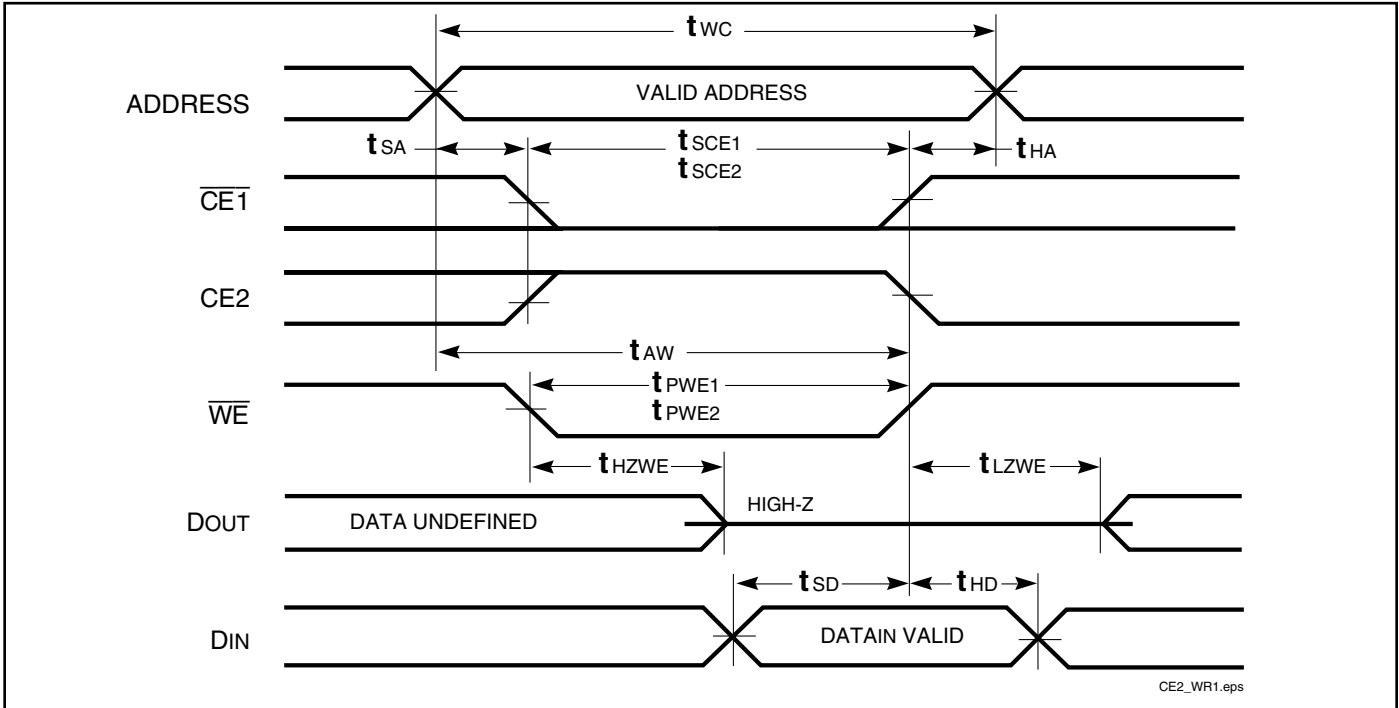
Symbol	Parameter	-12 ns		-15 ns		Unit
		Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	12	—	15	—	ns
t <sub>SCE1</sub>	$\overline{CE1}$ to Write End	10	—	12	—	ns
t <sub>SCE2</sub>	CE2 to Write End	10	—	12	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	10	—	12	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	ns
t <sub>PWE<sup>(3)</sup></sub>	$\overline{WE}$ Pulse Width	10	—	12	—	ns
t <sub>SD</sub>	Data Setup to Write End	7	—	10	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	ns
t <sub>HZWE<sup>(4)</sup></sub>	$\overline{WE}$ LOW to High-Z Output	—	7	—	7	ns
t <sub>LZWE<sup>(4)</sup></sub>	$\overline{WE}$ HIGH to Low-Z Output	2	—	2	—	ns

**Notes:**

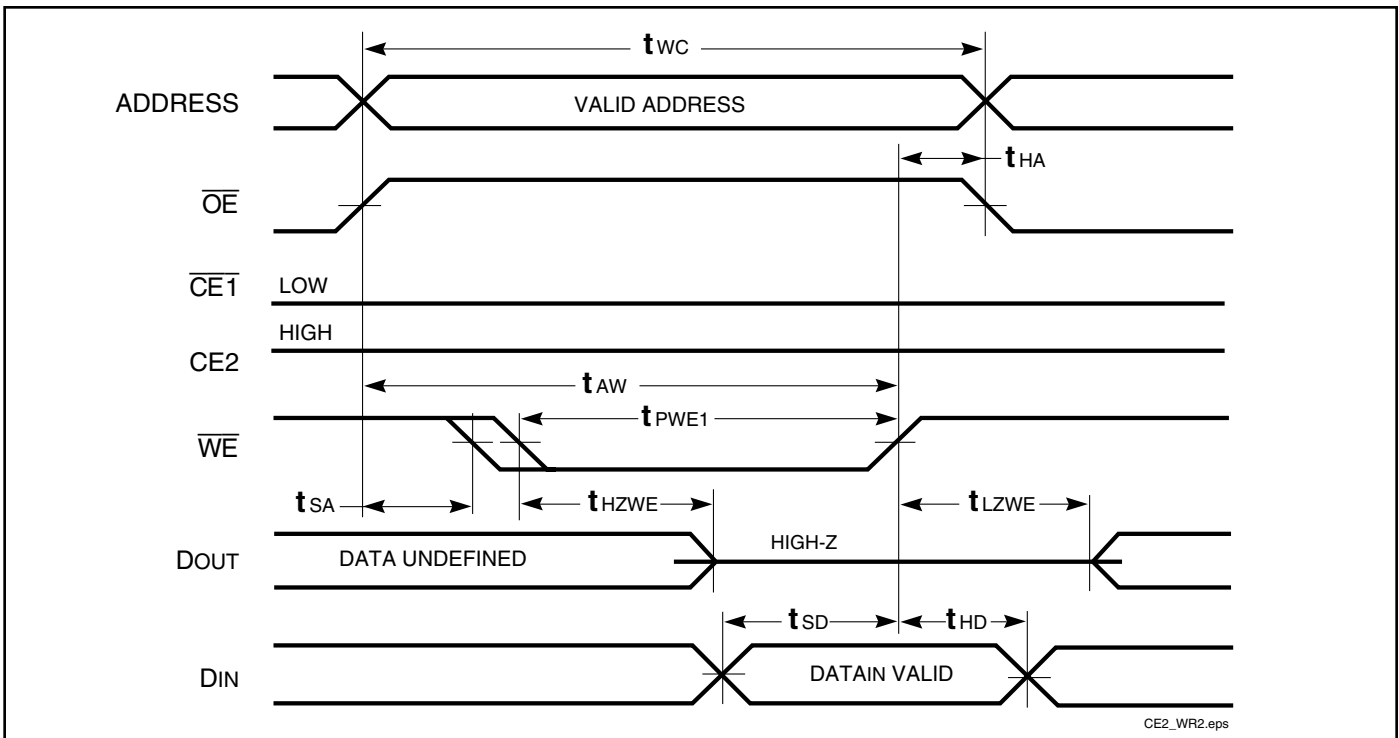
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of  $\overline{CE1}$  LOW, CE2 HIGH and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
3. Tested with OE HIGH.
4. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

**AC WAVEFORMS**

**WRITE CYCLE NO. 1** ( $\overline{CE1}$  Controlled,  $\overline{OE}$  is HIGH or LOW) <sup>(1)</sup>



**WRITE CYCLE NO. 2** ( $\overline{OE}$  is HIGH During Write Cycle) <sup>(1,2)</sup>

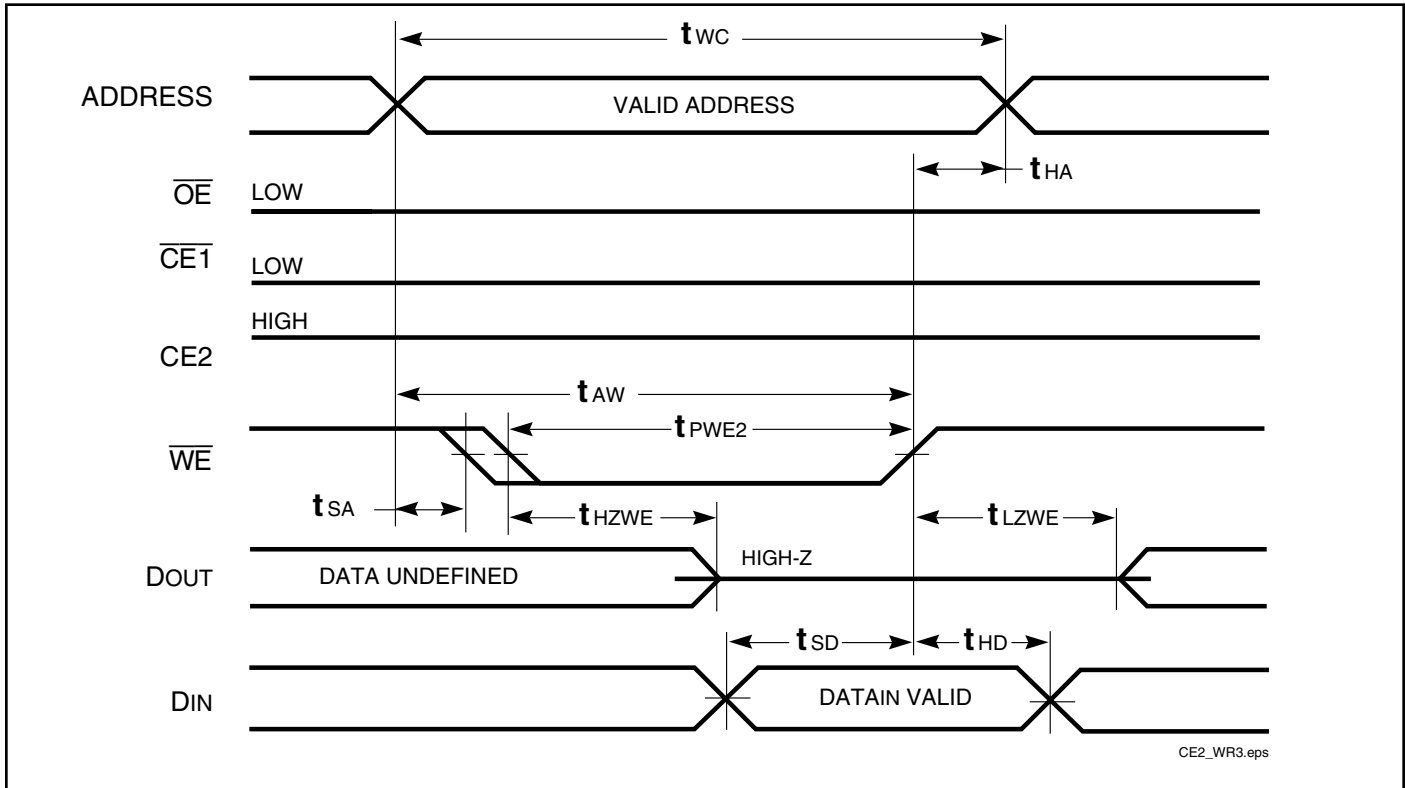


**Notes:**

1. The internal write time is defined by the overlap of  $\overline{CE1}$  LOW, CE2 HIGH and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if  $\overline{OE} = V_{IH}$ .



**WRITE CYCLE NO. 3** ( $\overline{OE}$  is LOW During Write Cycle) <sup>(1)</sup>



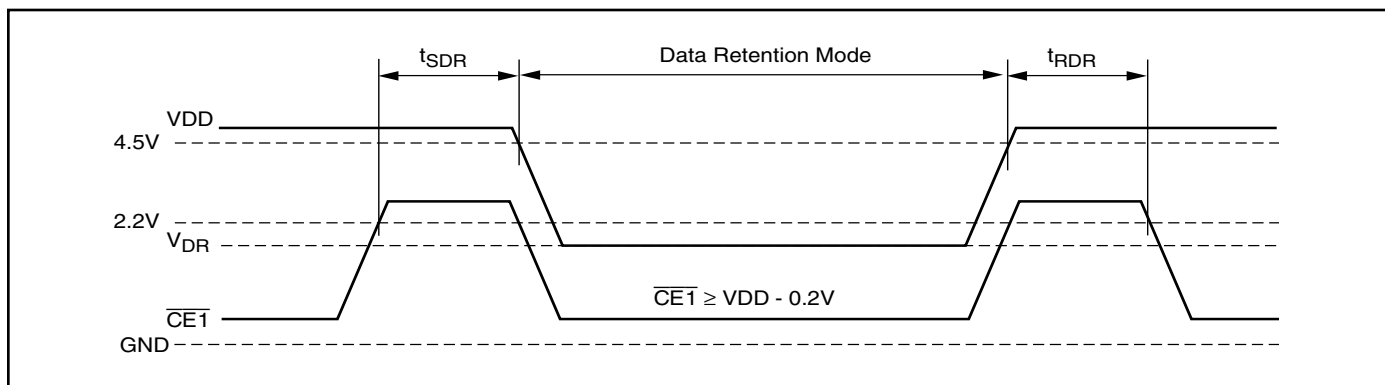
### DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>DD</sub> for Data Retention	See Data Retention Waveform	2.0		5.5	V
I <sub>DR</sub>	Data Retention Current	V <sub>DD</sub> = 2.0V, $\overline{CE1} \geq V_{DD} - 0.2V$ or $CE2 \leq 0.2V$ V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ V <sub>SS</sub> + 0.2V	Com. Ind. Auto.	— — —	200 400 450 500	μA
t <sub>SDR</sub>	Data Retention Setup Time	See Data Retention Waveform	0		—	ns
t <sub>RDR</sub>	Recovery Time	See Data Retention Waveform	t <sub>RC</sub>		—	ns

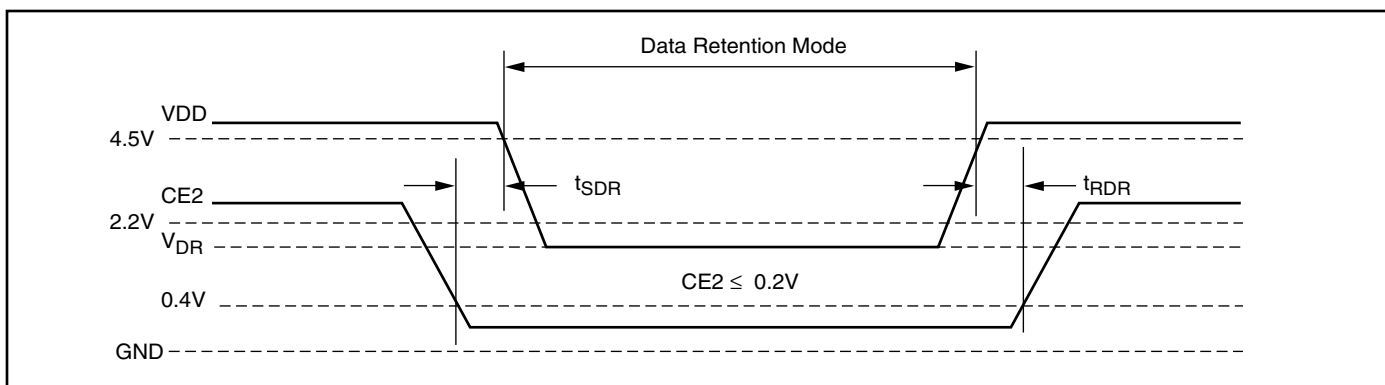
**Note:**

1. Typical Values are measured at V<sub>DD</sub> = 5V, T<sub>A</sub> = 25°C and not 100% tested.

### DATA RETENTION WAVEFORM ( $\overline{CE1}$ Controlled)



### DATA RETENTION WAVEFORM (CE2 Controlled)



## IS61C1024AL, IS64C1024AL

### ORDERING INFORMATION: IS61C1024AL

**Commercial Range: 0°C to +70°C**

Speed (ns)	Order Part No.	Package
12	IS61C1024AL-12T	TSOP (Type I)

### ORDERING INFORMATION: IS61C1024AL

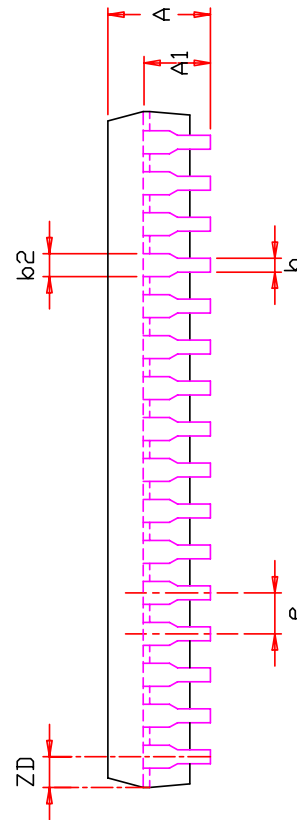
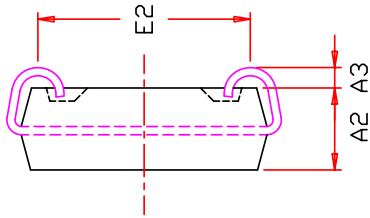
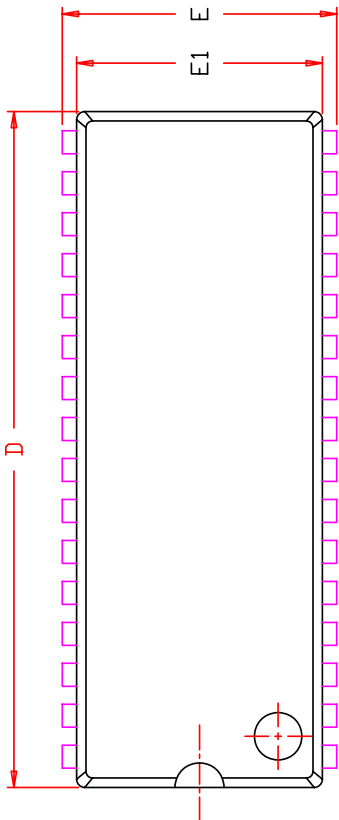
**Industrial Range: -40°C to +85°C**

Speed (ns)	Order Part No.	Package
12	IS61C1024AL-12JLI	300-mil Plastic SOJ, Lead-free
	IS61C1024AL-12KI	400-mil Plastic SOJ
	IS61C1024AL-12KLI	400-mil Plastic SOJ, Lead-free
	IS61C1024AL-12HI	sTSOP (Type I)
	IS61C1024AL-12HLI	sTSOP (Type I), Lead-free
	IS61C1024AL-12TI	TSOP (Type I)
	IS61C1024AL-12TLI	TSOP (Type I), Lead-free

### ORDERING INFORMATION: IS64C1024AL

**Automotive Range: -40°C to +125°C**

Speed (ns)	Order Part No.	Package
15	IS64C1024AL-15KA3	400-mil Plastic SOJ
	IS64C1024AL-15TA3	TSOP (Type I)



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.05		3.76	0.120		0.148
A1	2.08		2.41	0.082		0.095
A2	2.41	2.54	2.67	0.095	0.100	0.105
A3	0.64		1.09	0.025		0.043
b	0.41		0.51	0.016		0.020
b2	0.66		0.81	0.026		0.032
D	20.82		21.09	0.820		0.830
E	8.38	8.51	8.64	0.330	0.335	0.340
E1	7.49	7.62	7.75	0.295	0.300	0.305
E2	6.48		6.99	0.255		0.275
e	1.27	BSC.	0.050	BSC.		
ZD	0.95	REF.	0.037	REF.		

**NOTE :**

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.



TITLE

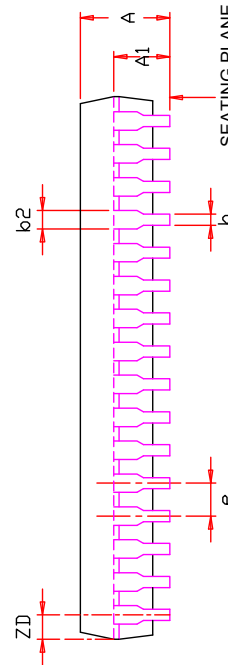
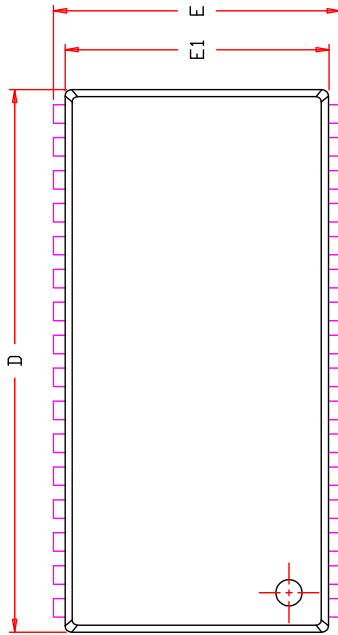
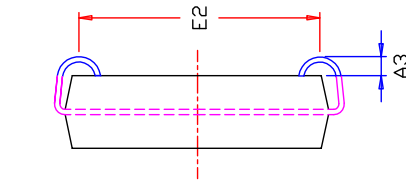
32L 300mil SOJ  
Package Outline

REV. C

DATE

08/14/2009

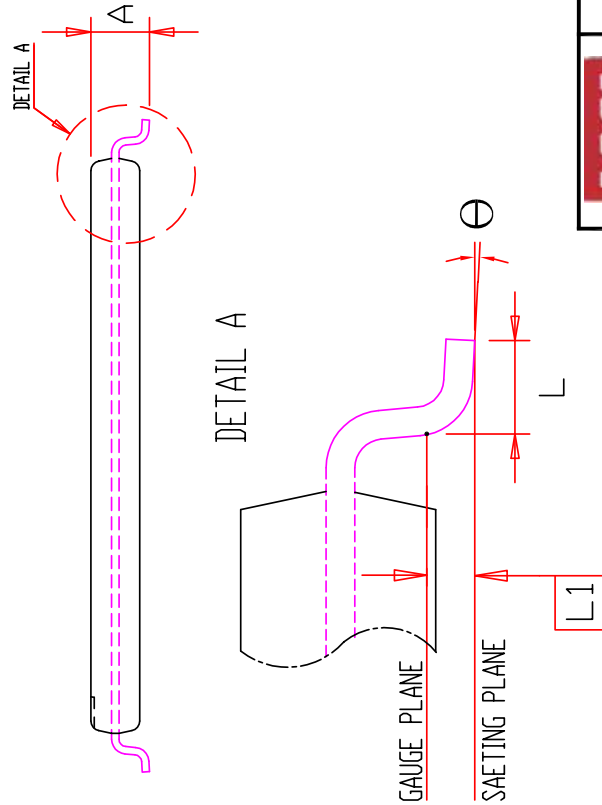
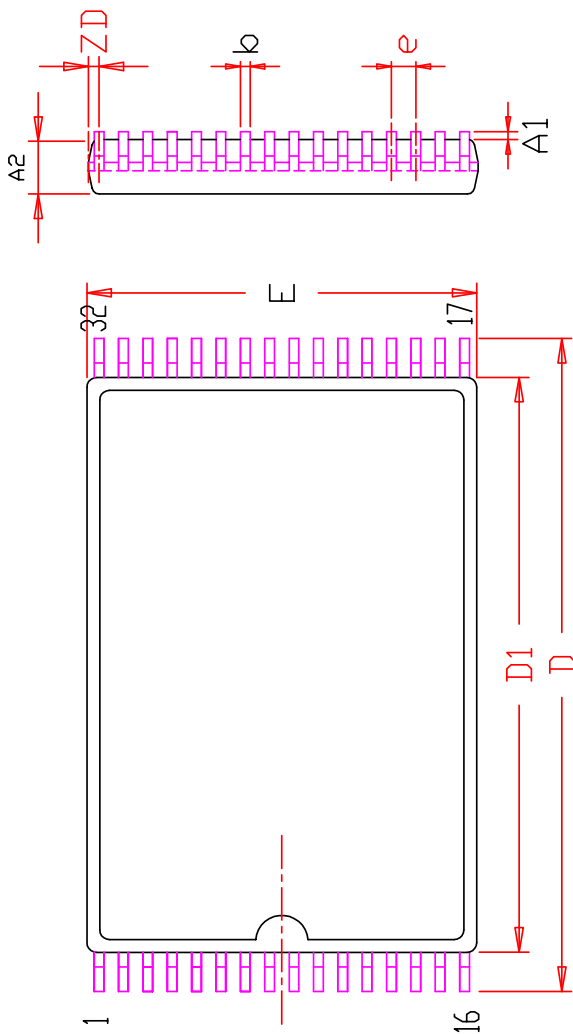
SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	NOM. MAX.	MIN.	NOM. MAX.
A	3.25	3.76	0.128	0.148
A1	2.08		0.082	
A3	0.635		0.025	
b	0.38	0.51	0.015	0.020
b2	0.66	0.71	0.026	0.028
D	20.82	20.95	0.820	0.825
E	11.05	11.18	0.435	0.440
E1	10.03	10.16	0.395	0.400
E2	9.40	BSC	0.370	BSC
e	1.27	BSC.	0.050	BSC.
ZD	0.95	REF	0.037	REF



**NOTE :**

1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b2 does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.
5. Reference document : JEDEC SPEC MS-027.

	TITLE	32L 400mil SOJ Package Outline	REV.	E	DATE	12/19/2007
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SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.95		1.25	0.037		0.049
A1	0.05		0.15	0.002		0.008
A2	0.90		1.05	0.035		0.041
b	0.16		0.27	0.006		0.011
D	13.10	13.40	13.70	0.516	0.528	0.539
D1	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	0.50 BSC.			0.020 BSC.		
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.25 BSC.			0.010 BSC.		
ZD	0.25 REF.			0.010 REF.		
Θ	0	3°	5°	0	3°	5°

**NOTE :**

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
4. Reference Document : JEDEC MO-183



TITLE

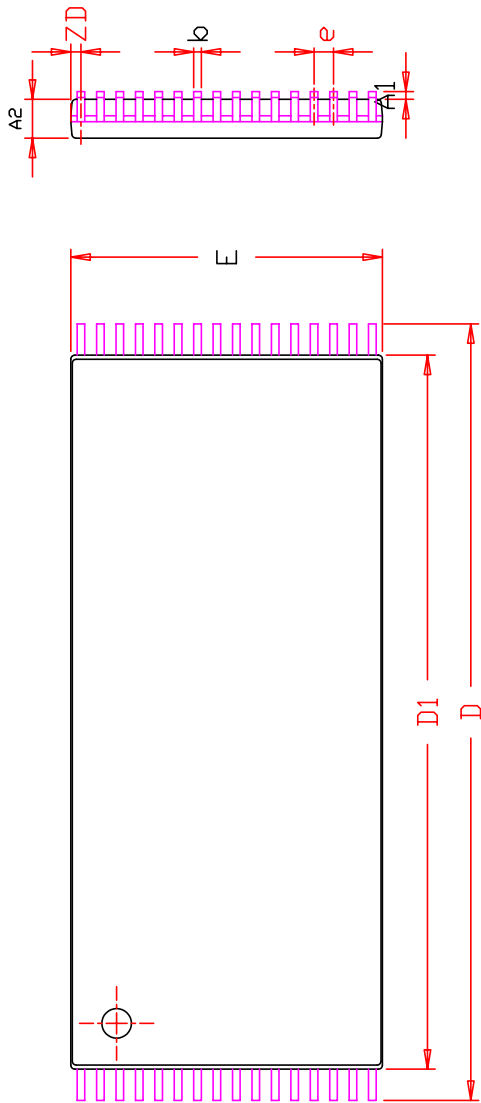
32L 8x13.4mm TSOP-1  
Package Outline

REV.

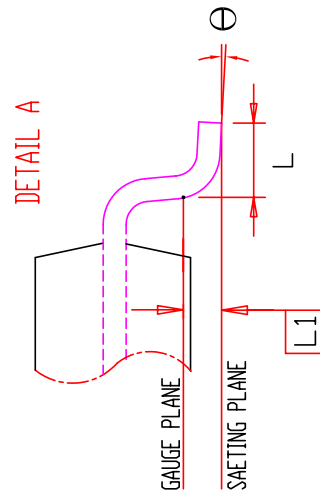
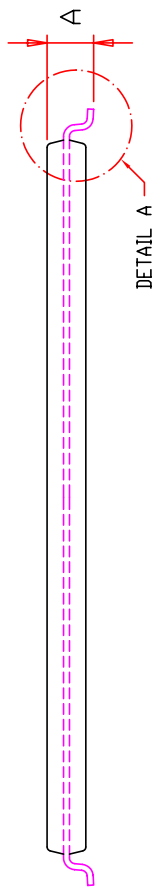
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DATE

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SYMBOL	DIMENSION IN MM		
	MIN	NOM	MAX
A	1.00		1.20
A1	0.05		0.20
A2	0.95	1.00	1.05
b	0.17		0.27
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	7.80	8.00	8.20
e	0.50 BSC.		
L	0.40		0.70
L1	0.25 BSC.		
ZD	0.25 REF.		
Θ	0	5°	8°



**NOTE :**

1. Controlling dimension : mm
2. Dimension D1 adn E do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

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