

# 1M x 8 HIGH-SPEED CMOS STATIC RAM

JANUARY 2019

## FEATURES

- High-speed access times: 8, 10, 20 ns
- High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with CE and OE options
- CE power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single power supply
  - V<sub>DD</sub> 1.65V to 2.2V (IS61WV10248ALL)  
 speed = 20ns for V<sub>cc</sub> = 1.65V to 2.2V
  - V<sub>DD</sub> 2.4V to 3.6V (IS61/64WV10248BLL)  
 speed = 10ns for V<sub>cc</sub> = 2.4V to 3.6V  
 speed = 8ns for V<sub>cc</sub> = 3.3V ± 5%
- Packages available:
  - 48-ball miniBGA (9mm x 11mm)
  - 44-pin TSOP (Type II)
- Industrial and Automotive Temperature Support
- Lead-free available

## DESCRIPTION

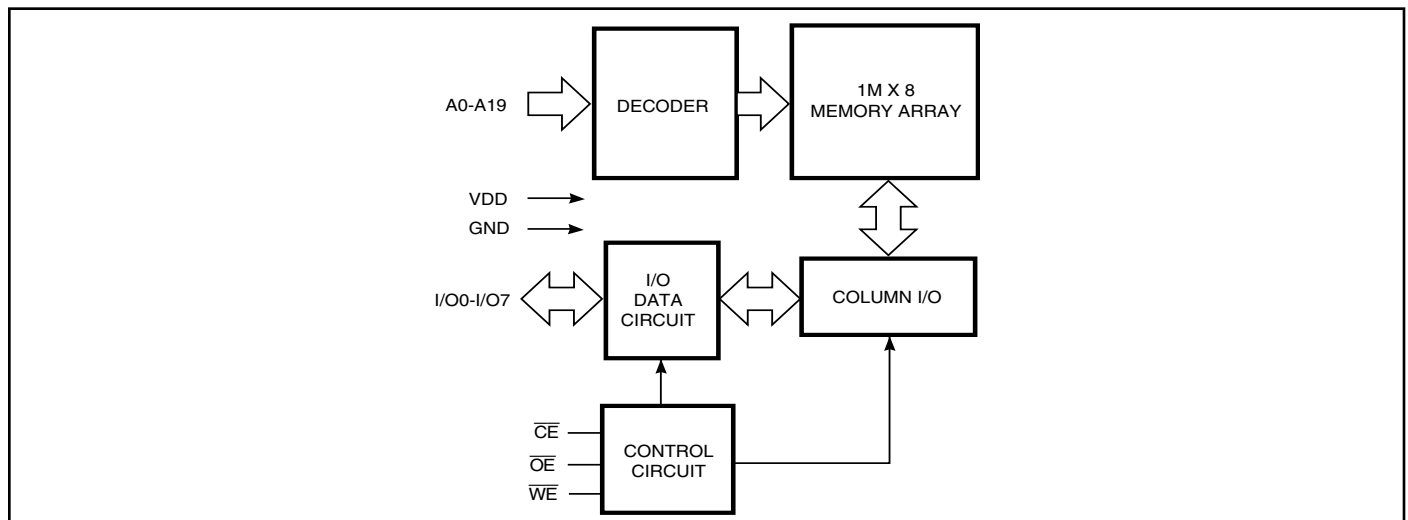
The ISSI IS61WV10248ALL/BLL and IS64WV10248BLL are very high-speed, low power, 1M-word by 8-bit CMOS static RAM. The IS61WV10248ALL/BLL and IS64WV10248BLL are fabricated using ISSI's high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When CE is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

The IS61WV10248ALL/BLL and IS64WV10248BLL operate from a single power supply and all inputs are TTL-compatible.

The IS61WV10248ALL/BLL and IS64WV10248BLL are available in 48 ball mini BGA and 44-pin TSOP (Type II) packages.

## FUNCTIONAL BLOCK DIAGRAM



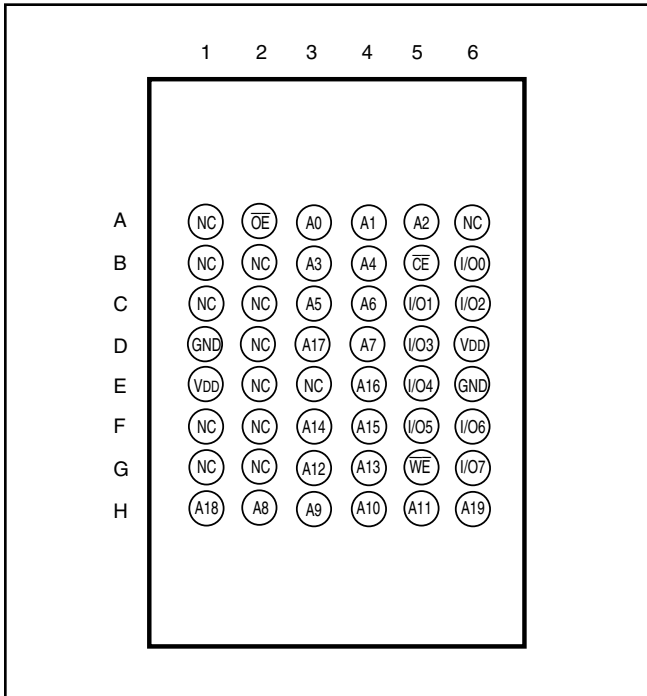
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Integrated Silicon Solution, Inc. does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless Integrated Silicon Solution, Inc. receives written assurance to its satisfaction, that:

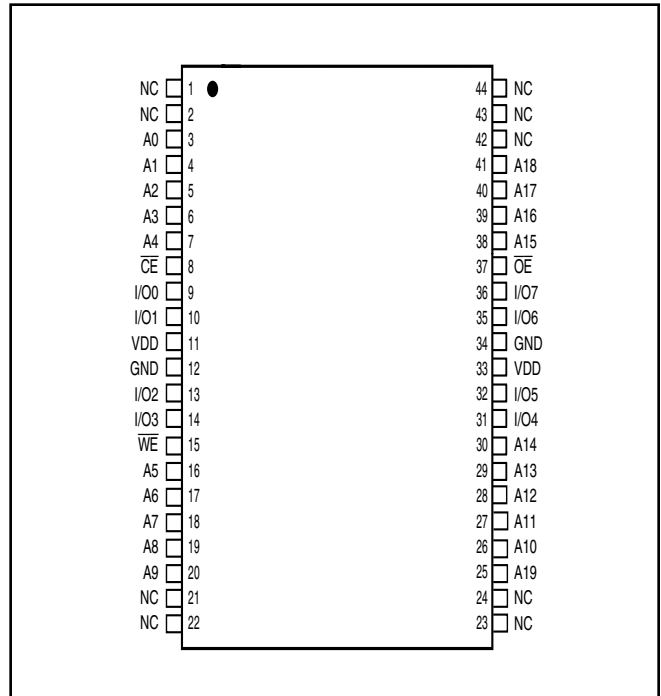
- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

**PIN CONFIGURATION**

**48-pin Mini BGA (M ) (9mm x 11mm)**



**44-pin TSOP (Type II )**



**PIN DESCRIPTIONS**

A0-A19	Address Inputs
CE	Chip Enable Input
OE	Output Enable Input
WE	Write Enable Input
I/O0-I/O7	Data Input / Output
VDD	Power
GND	Ground
NC	No Connection

## TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	V <sub>DD</sub> Current
Not Selected (Power-down)	X	H	X	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
Output Disabled	H	L	H	High-Z	I <sub>CC</sub>
Read	H	L	L	D <sub>OUT</sub>	I <sub>CC</sub>
Write	L	L	X	D <sub>IN</sub>	I <sub>CC</sub>

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to V <sub>DD</sub> + 0.5	V
V <sub>DD</sub>	V <sub>DD</sub> Relates to GND	-0.3 to 4.0	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W

### Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE<sup>(1,2)</sup>

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>OUT</sub> = 0V	8	pF

### Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>DD</sub> = 3.3V.



**OPERATING RANGE (V<sub>DD</sub>) (IS61WV10248ALL)**

Range	Ambient Temperature	V <sub>DD</sub> (20 ns)
Commercial	0°C to +70°C	1.65V-2.2V
Industrial	-40°C to +85°C	1.65V-2.2V
Automotive	-40°C to +125°C	1.65V-2.2V

**OPERATING RANGE (V<sub>DD</sub>) (IS61WV10248BLL)<sup>(1)</sup>**

Range	Ambient Temperature	V <sub>DD</sub> (8 ns)	V <sub>DD</sub> (10 ns)
Commercial	0°C to +70°C	3.3V ± 5%	2.4V-3.6V
Industrial	-40°C to +85°C	3.3V ± 5%	2.4V-3.6V

**Note:**

1. When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V ± 5%, the device meets 8ns.

**OPERATING RANGE (V<sub>DD</sub>) (IS64WV10248BLL)**

Range	Ambient Temperature	V <sub>DD</sub> (10 ns)
Automotive	-40°C to +125°C	2.4V-3.6V

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

**V<sub>DD</sub> = 3.3V ± 5%**

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DD</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>DD</sub> = Min., I <sub>OL</sub> = 8.0 mA	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	-1	1	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled	-1	1	μA

**Note:**

- V<sub>IL</sub> (min.) = -0.3V DC; V<sub>IL</sub> (min.) = -2.0V AC (pulse width ≤ 2 ns). Not 100% tested.  
 V<sub>IH</sub> (max.) = V<sub>DD</sub> + 0.3V DC; V<sub>IH</sub> (max.) = V<sub>DD</sub> + 2.0V AC (pulse width ≤ 2 ns). Not 100% tested.

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

**V<sub>DD</sub> = 2.4V-3.6V**

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DD</sub> = Min., I <sub>OH</sub> = -1.0 mA	1.8	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>DD</sub> = Min., I <sub>OL</sub> = 1.0 mA	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	-1	1	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled	-1	1	μA

**Note:**

- V<sub>IL</sub> (min.) = -0.3V DC; V<sub>IL</sub> (min.) = -2.0V AC (pulse width ≤ 2 ns). Not 100% tested.  
 V<sub>IH</sub> (max.) = V<sub>DD</sub> + 0.3V DC; V<sub>IH</sub> (max.) = V<sub>DD</sub> + 2.0V AC (pulse width ≤ 2 ns). Not 100% tested.

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

**V<sub>DD</sub> = 1.65V-2.2V**

Symbol	Parameter	Test Conditions	V <sub>DD</sub>	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	1.65-2.2V	1.4	—	V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA	1.65-2.2V	—	0.2	V
V <sub>IH</sub>	Input HIGH Voltage		1.65-2.2V	1.4	V <sub>DD</sub> + 0.2	V
V <sub>IL</sub> <sup>(1)</sup>	Input LOW Voltage		1.65-2.2V	-0.2	0.4	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>		-1	1	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled		-1	1	μA

**Note:**

- V<sub>IL</sub> (min.) = -0.3V DC; V<sub>IL</sub> (min.) = -2.0V AC (pulse width ≤ 2 ns). Not 100% tested.  
 V<sub>IH</sub> (max.) = V<sub>DD</sub> + 0.3V DC; V<sub>IH</sub> (max.) = V<sub>DD</sub> + 2.0V AC (pulse width ≤ 2 ns). Not 100% tested.

**AC TEST CONDITIONS (HIGH SPEED)**

Parameter	Unit (2.4V-3.6V)	Unit (3.3V ± 5%)	Unit (1.65V-2.2V)
Input Pulse Level	0.4V to $V_{DD}-0.3V$	0.4V to $V_{DD}-0.3V$	0.4V to $V_{DD}-0.2V$
Input Rise and Fall Times	1.5ns	1.5ns	1.5ns
Input and Output Timing and Reference Level ( $V_{Ref}$ )	$V_{DD}/2$	$V_{DD}/2 + 0.05$	$V_{DD}/2$
Output Load	See Figures 1 and 2	See Figures 1 and 2	See Figures 1 and 2

**AC TEST LOADS**

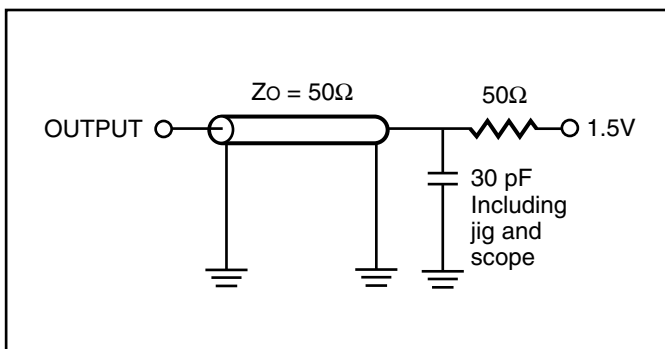


Figure 1.

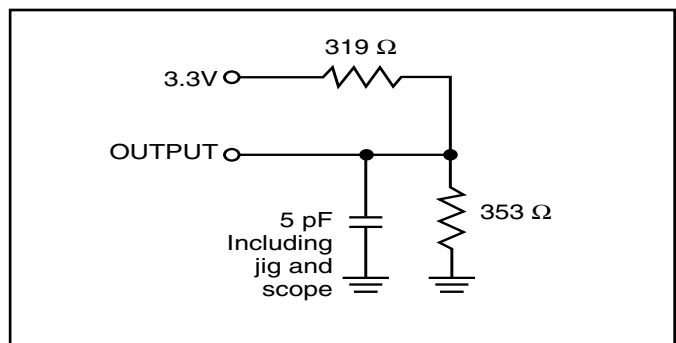


Figure 2.



**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Symbol	Parameter	Test Conditions		-8		-10		-20		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>CC</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com.	—	110	—	95	—	90	mA
			Ind.	—	120	—	100	—	100	
			Auto. typ. <sup>(2)</sup>	—	—	—	140	—	140	
						60				
I <sub>CC1</sub>	Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = 0	Com.	—	30	—	30	—	30	mA
			Ind.	—	35	—	35	—	35	
			Auto.	—	—	—	60	—	70	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> CE ≥ V <sub>IH</sub> , f = 0	Com.	—	30	—	30	—	30	mA
			Ind.	—	35	—	35	—	35	
			Auto.	—	—	—	70	—	70	
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max., CE ≥ V <sub>DD</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Com.	—	20	—	20	—	15	mA
			Ind.	—	25	—	25	—	20	
			Auto.	—	—	—	70	—	70	
			typ. <sup>(2)</sup>			4				

**Note:**

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.



**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Symbol	Parameter	-8		-10		Unit
		Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	8	—	10	—	ns
t <sub>AA</sub>	Address Access Time	—	8	—	10	ns
t <sub>OHA</sub>	Output Hold Time	2	—	2	—	ns
t <sub>ACE</sub>	$\overline{CE}$ Access Time	—	8	—	10	ns
t <sub>DOE</sub>	$\overline{OE}$ Access Time	—	5.5	—	6.5	ns
t <sub>HZOE<sup>(2)</sup></sub>	$\overline{OE}$ to High-Z Output	—	3	—	4	ns
t <sub>LZOE<sup>(2)</sup></sub>	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t <sub>HZCE<sup>(2)</sup></sub>	$\overline{CE}$ to High-Z Output	0	3	0	4	ns
t <sub>LZCE<sup>(2)</sup></sub>	$\overline{CE}$ to Low-Z Output	3	—	3	—	ns
t <sub>PU</sub>	Power Up Time	0	—	0	—	ns
t <sub>PD</sub>	Power Down Time	—	8	—	10	ns

**Notes:**

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage.



**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

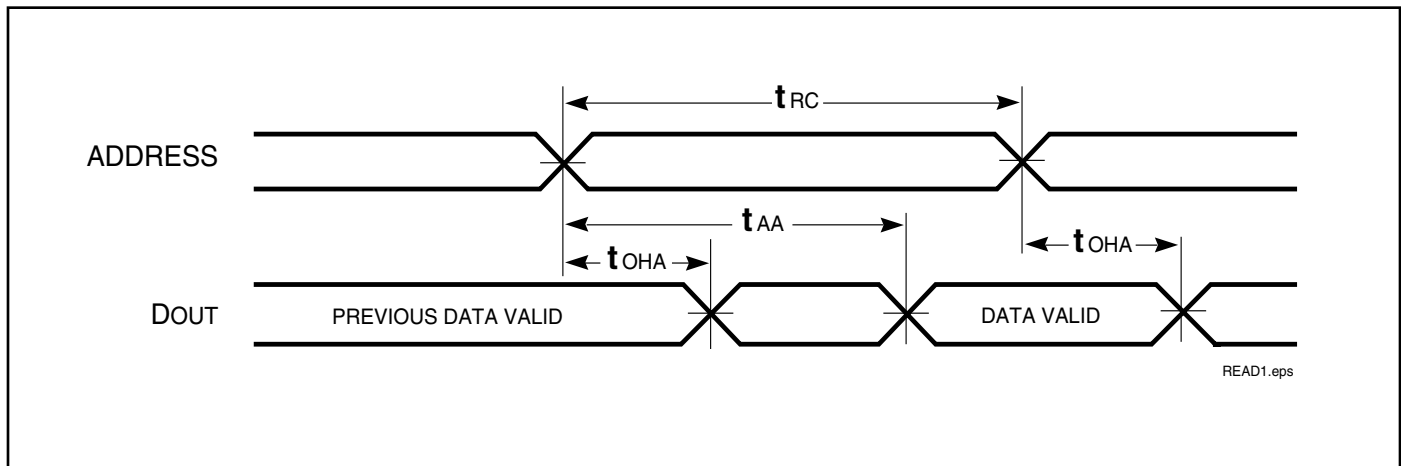
Symbol	Parameter	-20 ns		Unit
		Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	20	—	ns
t <sub>AA</sub>	Address Access Time	—	20	ns
t <sub>OHA</sub>	Output Hold Time	2.5	—	ns
t <sub>ACE</sub>	$\overline{CE}$ Access Time	—	20	ns
t <sub>DOE</sub>	$\overline{OE}$ Access Time	—	8	ns
t <sub>HZOE<sup>(2)</sup></sub>	$\overline{OE}$ to High-Z Output	0	8	ns
t <sub>LZOE<sup>(2)</sup></sub>	$\overline{OE}$ to Low-Z Output	0	—	ns
t <sub>HZCE<sup>(2)</sup></sub>	$\overline{CE}$ to High-Z Output	0	8	ns
t <sub>LZCE<sup>(2)</sup></sub>	$\overline{CE}$ to Low-Z Output	3	—	ns
t <sub>PU</sub>	Power Up Time	0	—	ns
t <sub>PD</sub>	Power Down Time	—	20	ns

**Notes:**

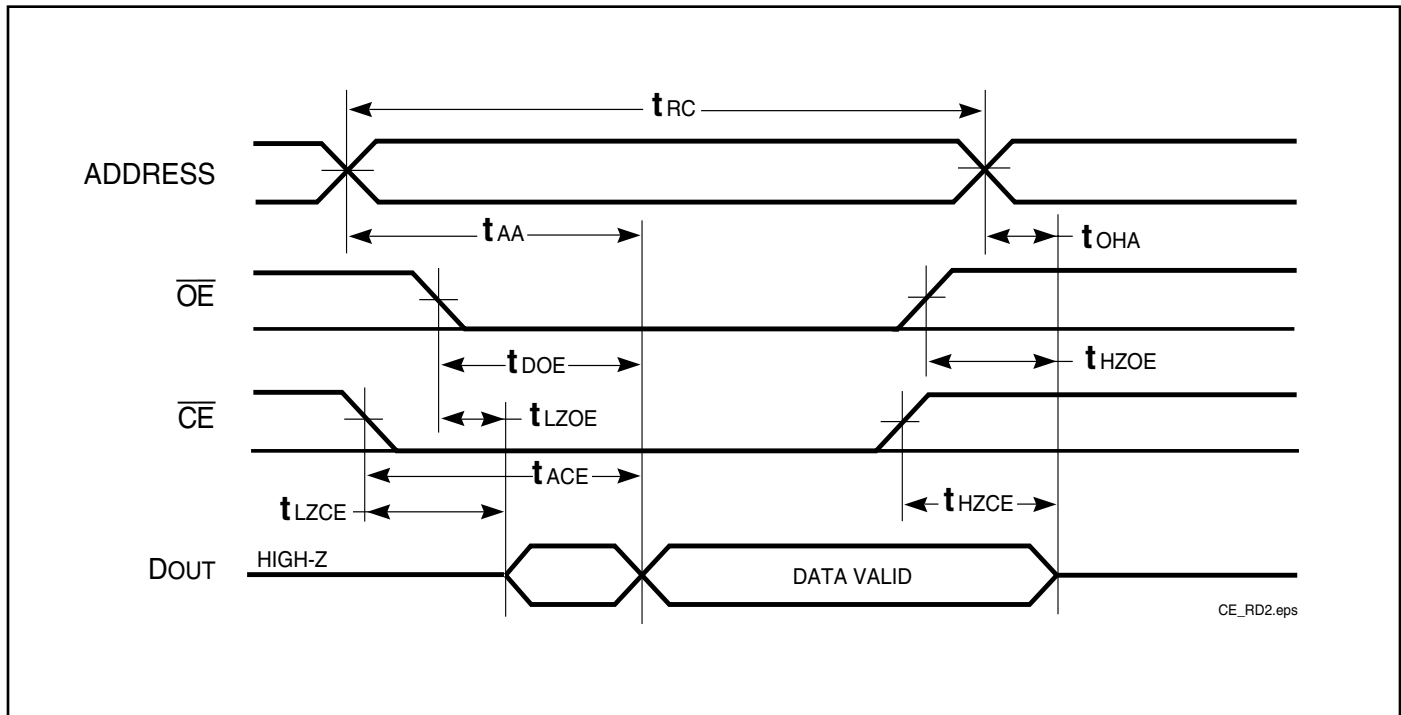
1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V<sub>DD</sub>-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

**AC WAVEFORMS**

**READ CYCLE NO. 1<sup>(1,2)</sup>** ( $\overline{CE} = \overline{OE} = V_{IL}$ )



**READ CYCLE NO. 2<sup>(1,3)</sup>** ( $\overline{CE}$  and  $\overline{OE}$  Controlled)



**Notes:**

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
3. Address is valid prior to or coincident with  $\overline{CE}$  LOW transitions.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,3)</sup>** (Over Operating Range)

Symbol	Parameter	-8		-10		Unit
		Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	8	—	10	—	ns
t <sub>SCE</sub>	$\overline{CE}$ to Write End	6.5	—	8	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	6.5	—	8	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	ns
t <sub>PWE1</sub>	$\overline{WE}$ Pulse Width ( $\overline{OE}$ = HIGH)	6.5	—	8	—	ns
t <sub>PWE2</sub>	$\overline{WE}$ Pulse Width ( $\overline{OE}$ = LOW)	8.0	—	10	—	ns
t <sub>SD</sub>	Data Setup to Write End	5	—	6	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	ns
t <sub>HZWE<sup>(2)</sup></sub>	$\overline{WE}$ LOW to High-Z Output	—	3.5	—	5	ns
t <sub>LZWE<sup>(2)</sup></sub>	$\overline{WE}$ HIGH to Low-Z Output	2	—	2	—	ns

**Notes:**

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development



**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup>** (Over Operating Range)

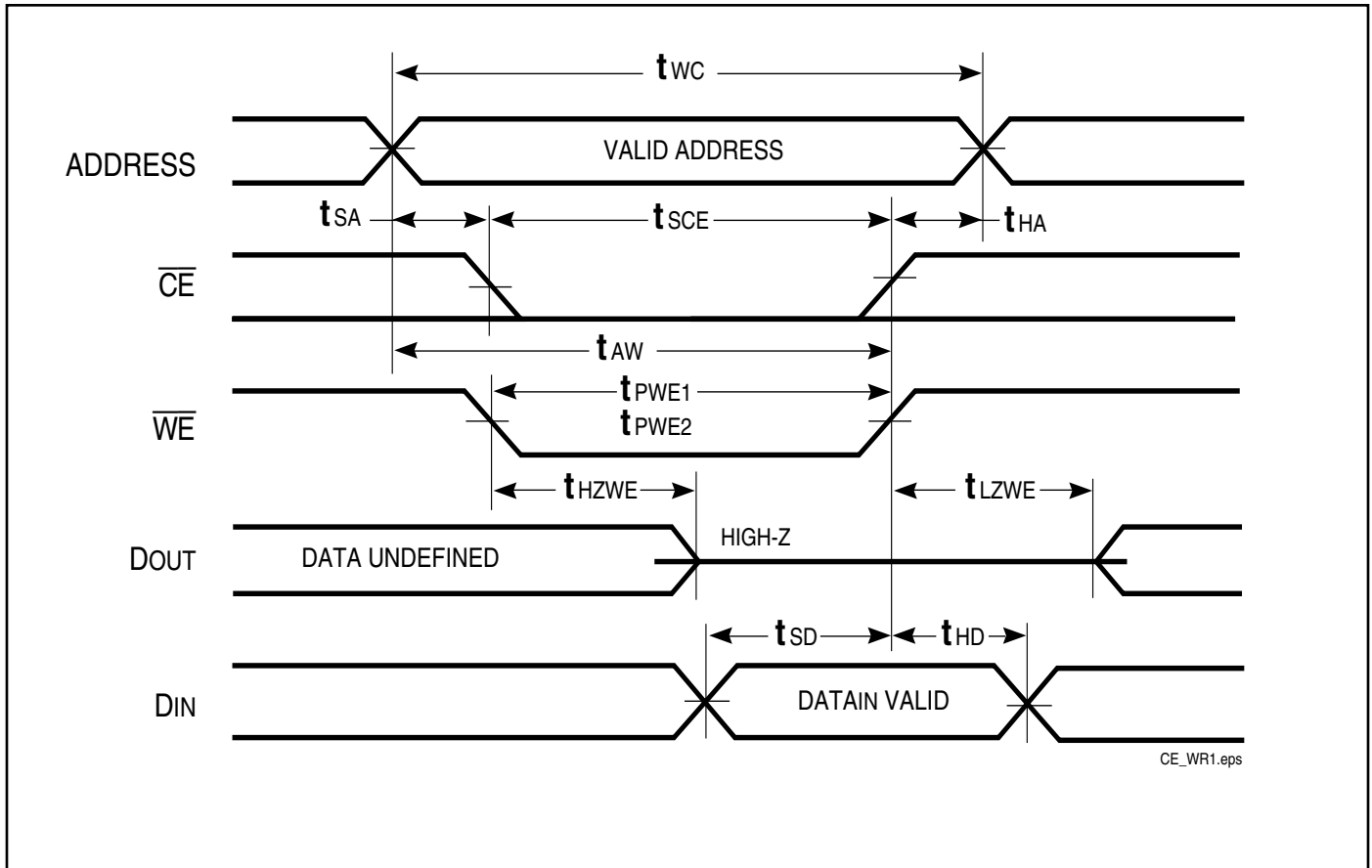
Symbol	Parameter	-20 ns		Unit
		Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	20	—	ns
t <sub>SCE</sub>	$\overline{CE}$ to Write End	12	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	12	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	ns
t <sub>PWE1</sub>	$\overline{WE}$ Pulse Width ( $\overline{OE}$ = HIGH)	12	—	ns
t <sub>PWE2</sub>	$\overline{WE}$ Pulse Width ( $\overline{OE}$ = LOW)	17	—	ns
t <sub>SD</sub>	Data Setup to Write End	9	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	ns
t <sub>HZWE<sup>(3)</sup></sub>	$\overline{WE}$ LOW to High-Z Output	—	9	ns
t <sub>LZWE<sup>(3)</sup></sub>	$\overline{WE}$ HIGH to Low-Z Output	3	—	ns

**Notes:**

1. Test conditions assume signal transition times of 1.5ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V<sub>DD</sub>-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

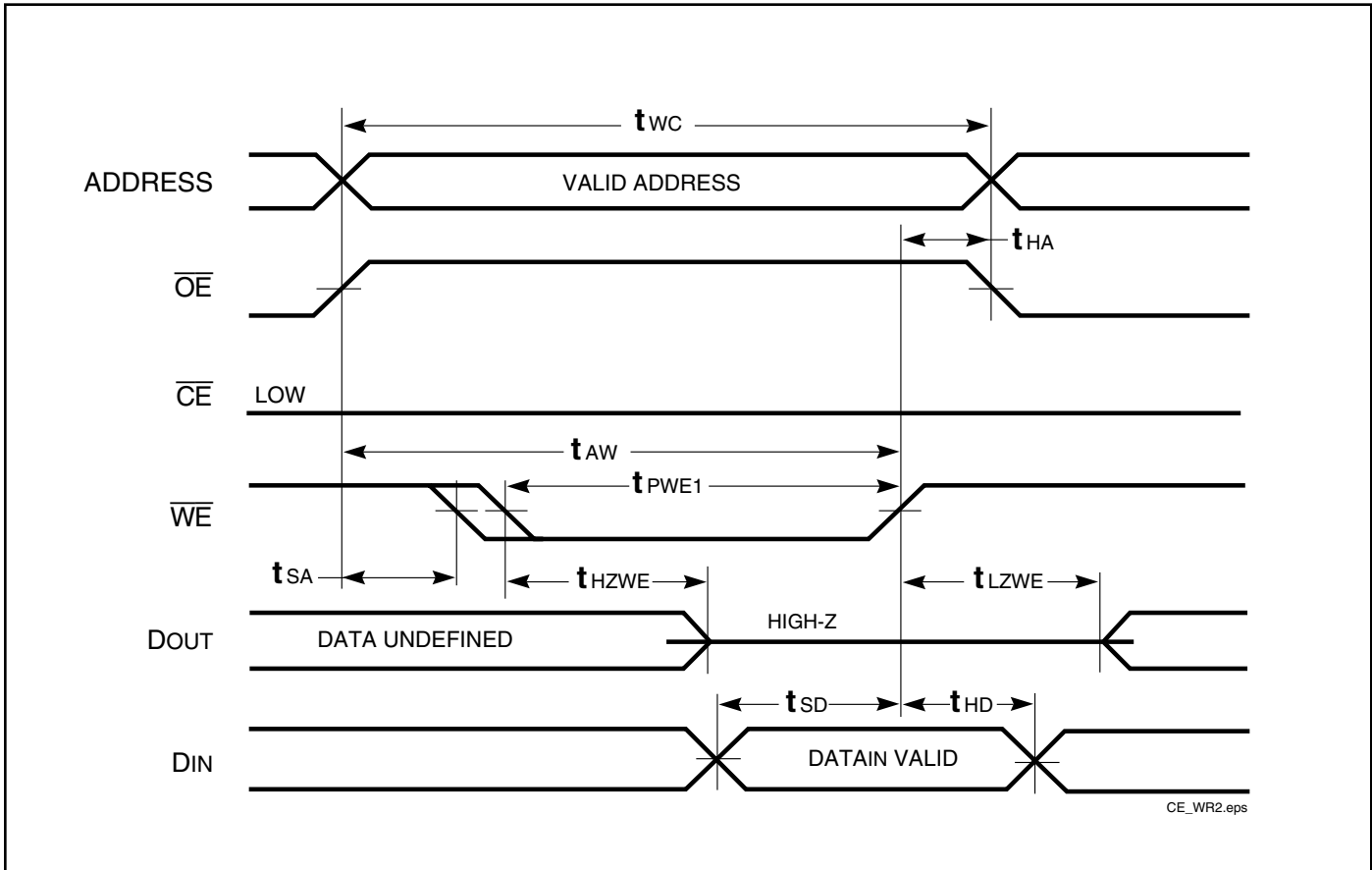
**AC WAVEFORMS**

**WRITE CYCLE NO. 1**<sup>(1,2)</sup> ( $\overline{CE}$  Controlled,  $\overline{OE}$  = HIGH or LOW)



**AC WAVEFORMS**

**WRITE CYCLE NO. 2**<sup>(1,2)</sup> ( $\overline{WE}$  Controlled:  $\overline{OE}$  is HIGH During Write Cycle)

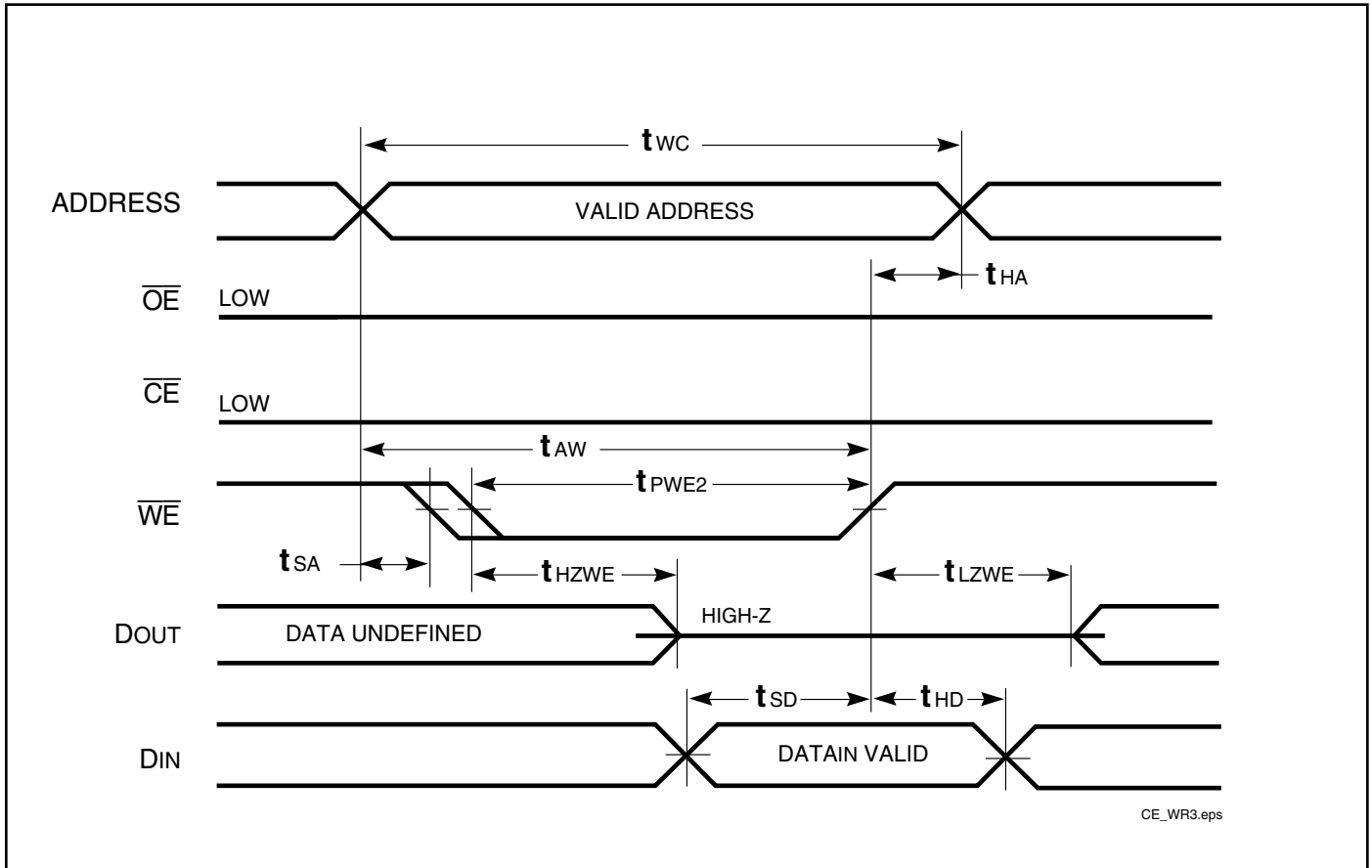


**Notes:**

1. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if  $\overline{OE} > V_{IH}$ .

### AC WAVEFORMS

**WRITE CYCLE NO. 3** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is LOW During Write Cycle)



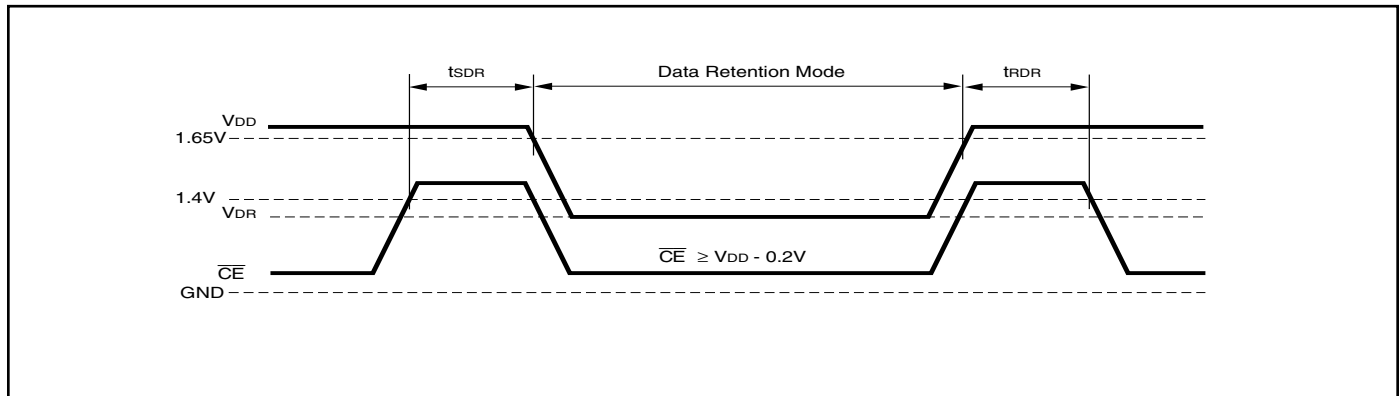
**DATA RETENTION SWITCHING CHARACTERISTICS**

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V <sub>DR</sub>	V <sub>DD</sub> for Data Retention	See Data Retention Waveform	1.2	3.6	V
I <sub>DR</sub>	Data Retention Current	V <sub>DD</sub> = 1.2V, $\overline{CE} \geq V_{DD} - 0.2V$	—	25	mA
		Ind.	—	70	
		Auto.	—	4	
		typ. <sup>(1)</sup>			
t <sub>SDR</sub>	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t <sub>RDR</sub>	Recovery Time	See Data Retention Waveform	t <sub>RC</sub>	—	ns

**Note:**

1. Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

**DATA RETENTION WAVEFORM ( $\overline{CE}$  Controlled)**





## ORDERING INFORMATION

**Industrial Range: -40°C to +85°C**

**Voltage Range: 2.4V to 3.6V**

Speed (ns)	Order Part No.	Package
10 (8 <sup>1</sup> )	IS61WV10248BLL-10MI	48 mini BGA (9mm x 11mm)
	IS61WV10248BLL-10MLI	48 mini BGA (9mm x 11mm), Lead-free
	IS61WV10248BLL-10TI	TSOP (Type II)
	IS61WV10248BLL-10TLI	TSOP (Type II), Lead-free

**Note:**

1. Speed = 8ns for  $V_{DD} = 3.3V \pm 5\%$ . Speed = 10ns for  $V_{DD} = 2.4V$  to 3.3V.

**Industrial Range: -40°C to +85°C**

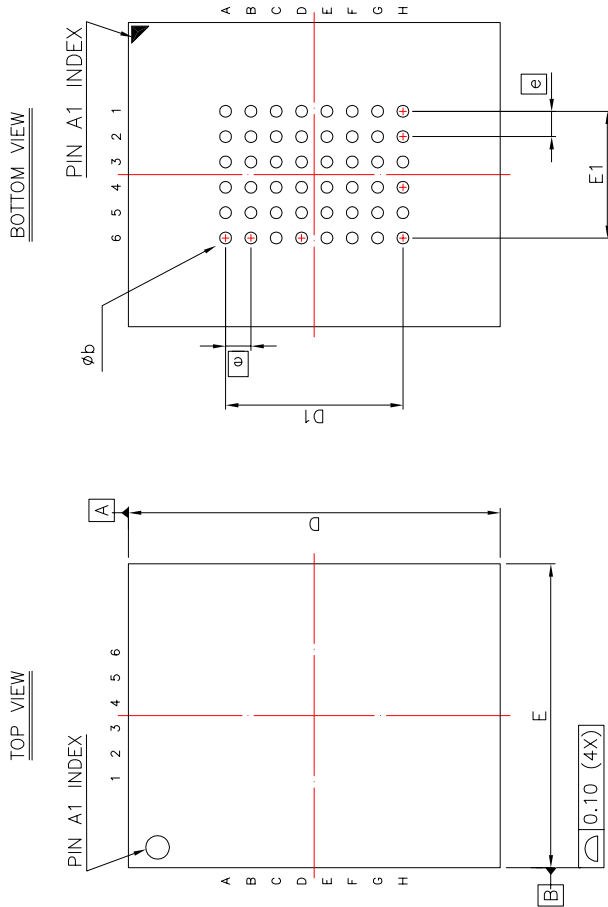
**Voltage Range: 1.65V to 2.2V**

Speed (ns)	Order Part No.	Package
20	IS61WV10248ALL-20MI	48 mini BGA (9mm x 11mm)
	IS61WV10248ALL-20MLI	48 mini BGA (9mm x 11mm), Lead-free
	IS61WV10248ALL-20TI	TSOP (Type II)

**Automotive Range: -40°C to +125°C**

**Voltage Range: 2.4V to 3.6V**

Speed (ns)	Order Part No.	Package
10	IS64WV10248BLL-10MA3	48 mini BGA (9mm x 11mm)
	IS64WV10248BLL-10TA3	TSOP (Type II)
	IS64WV10248BLL-10CTLA3	TSOP (Type II), Lead-free, Copper Leadframe



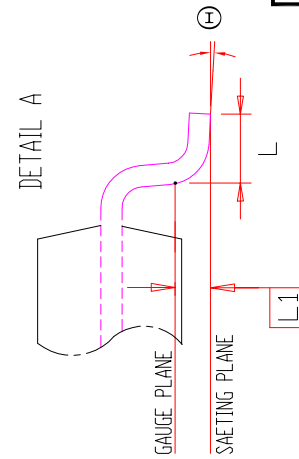
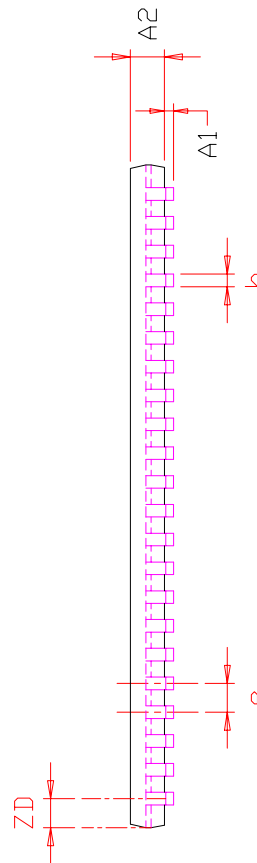
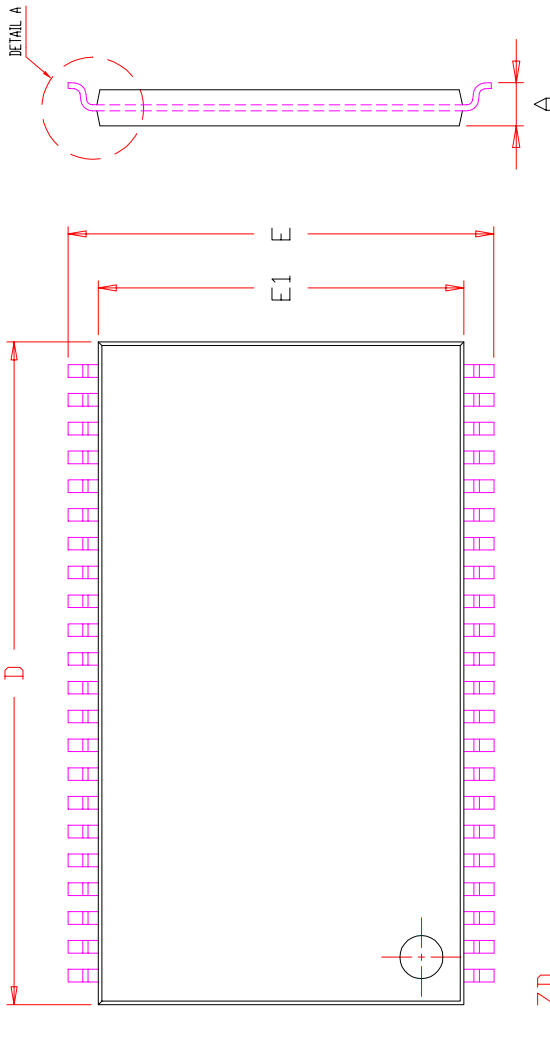
**NOTE :**

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

SYM.	DIMENSION (mm)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.20	—	0.30	0.008	—	0.012
b	0.30	0.35	0.40	0.012	0.014	0.016
D	10.90	11.00	11.10	0.429	0.433	0.437
D1	5.25 BSC			0.207 BSC		
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	3.75 BSC			0.148 BSC		
e	0.75 BSC			0.030 BSC		



<b>ISSI</b>	TITLE	48L 9x11mm TF-BGA Package Outline	REV. <b>B</b>	DATE <b>08/21/2008</b>
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SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00		1.20	0.039		0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.45	0.012		0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80	BSC.	0.031	BSC.		
L	0.40		0.69	0.016		0.027
L1	0.25	BSC.	0.010	BSC.		
ZD	0.805	REF.	0.032	REF.		
⊕	0		8°	0		8°

**NOTE :**

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

TITLE	44L 400mil TSOP-2 Package Outline	REV.	F	DATE	06/04/2008
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