

1M x 8 HIGH-SPEED ASYNCHRONOUS CMOS STATIC RAM WITH ECC

APRIL 2020

FEATURES

- High-speed access times: 8, 10, 20 ns
- High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with CE and OE options
- CE power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- · Packages available:
 - 48-ball miniBGA (6mm x 8mm)
 - 44-pin TSOP (Type II)
- Industrial and Automotive Temperature Support
- Lead-free available

DESCRIPTION

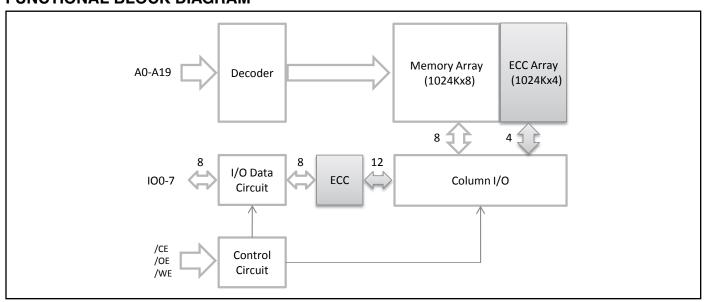
The *ISSI* IS61/64WV10248EDBLL are very high-speed, low power, 1M-word by 8-bit CMOS static RAM. The IS61/64WV10248EDBLL are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{\text{CE}}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

The IS61/64WV10248EDBLL operate from a single power supply and all inputs are TTL-compatible.

The IS61/64WV10248EDBLL are available in 48 ball mini BGA (6mm x 8mm) and 44-pin TSOP (Type II) packages.

FUNCTIONAL BLOCK DIAGRAM



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a.) the risk of injury or damage has been minimized;

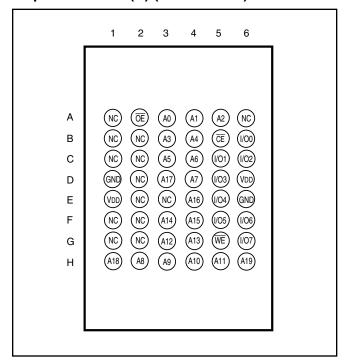
b.) the user assume all such risks; and

c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

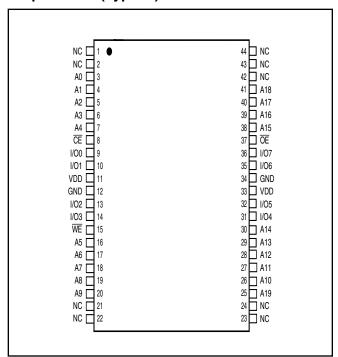


PIN CONFIGURATION

48-pin Mini BGA (B) (6mm x 8mm)



44-pin TSOP (Type II)



PIN DESCRIPTIONS

A0-A19	Address Inputs
CE	Chip Enable Input
ŌĒ	Output Enable Input
WE	Write Enable Input
I/O0-I/O	7 Data Input / Output
VDD	Power
GND	Ground
NC	No Connection



TRUTH TABLE

Mode	WE	CE	ŌĒ	I/O Operation	VDD Current
Not Selected (Power-down)	Х	Н	Х	High-Z	ISB1, ISB2
Output Disable	ed H	L	Н	High-Z	Icc
Read	Н	L	L	D оит	Icc
Write	L	L	Х	Din	Icc

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V TERM	Terminal Voltage with Respect to GND	-0.5 to $V_{DD} + 0.5$	V
VDD	VDD Relates to GND	-0.3 to 4.0	V
Тѕтс	Storage Temperature	-65 to +150	°C
Рт	Power Dissipation	1.0	W

Notes:

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit	
Cin	Input Capacitance	$V_{IN} = 0V$	6	pF	
$C_{I/O}$	Input/Output Capacitance	Vout = $0V$	8	pF	

Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

^{1.} Tested initially and after any design or process changes that may affect these parameters.

^{2.} Test conditions: $TA = 25^{\circ}C$, f = 1 MHz, VDD = 3.3V.



OPERATING RANGE (VDD)1

Range	Ambient Temperature	IS61WV10248EDBLL Vdd (8, 10ns)	IS64WV10248EDBLL Vdd (10ns)
Industrial	–40°C to +85°C	2.4V-3.6V	_
Automotive (A1)	–40°C to +85°C	_	2.4V-3.6V
Automotive (A3)	–40°C to +125°C	_	2.4V-3.6V

Note:

ERROR DETECTION AND ERROR CORRECTION

- Independent ECC with hamming code for each byte
- Detect and correct one bit error per byte
- Better reliability than parity code schemes which can only detect an error but not correct an error
- Backward Compatible: Drop in replacement to current in industry standard devices (without ECC)

^{1.} Contact SRAM@issi.com for 1.8V option



DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

$V_{DD} = 2.4V-3.6V$

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
Vон	Output HIGH Voltage	$V_{DD} = Min., I_{OH} = -1.0 \text{ mA}$	1.8	_	V
Vol	Output LOW Voltage	VDD = Min., IOL = 1.0 mA	_	0.4	V
VIH	Input HIGH Voltage		2.0	VDD + 0.3	V
VIL	Input LOW Voltage(1)		-0.3	0.8	V
lu	Input Leakage	$GND \leq Vin \leq Vdd$	-1	1	μA
ILO	Output Leakage	GND ≤ Vout ≤ Vdd, Outputs Disabled	-1	1	μA

Note:

ACTEST CONDITIONS (HIGH SPEED)

Parameter	Unit (2.4V-3.6V)	
Input Pulse Level	0.4V to VDD-0.3V	
Input Rise and Fall Times	1.5ns	
Input and Output Timing and Reference Level (VRef)	VDD/2	
Output Load	See Figures 1 and 2	

ACTEST LOADS

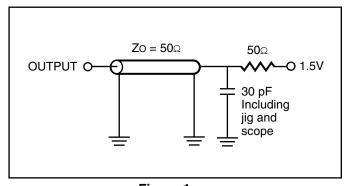


Figure 1.

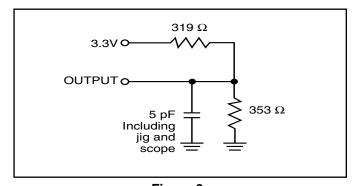


Figure 2.

^{1.} V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width ≤ 2 ns). Not 100% tested. V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width ≤ 2 ns). Not 100% tested.



POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

				-	8	-10	-2	.0	
Symbol	Parameter	Test Conditions		Min.	Max.	Min. Max.	Min.	Max.	Unit
Icc	VDD Dynamic Operating	$V_{DD} = Max.,$	Com.	_	50	— 45	_	35	mA
	Supply Current	IOUT = 0 mA, f = fMAX	Ind.	_	60	- 55	_	45	
			Auto.	_	_	- 65	_	60	
			typ.(2)			15			
lcc1	Operating	V _{DD} = Max.,	Com.	_	20	— 20	_	20	mA
	Supply Current	IOUT = 0 mA, f = 0	Ind.	_	25	— 25	_	25	
	,		Auto.	_	_	- 50	_	50	
ISB1	TTL Standby Current	V _{DD} = Max.,	Com.	_	20	— 20	_	20	mA
	(TTL Inputs)	VIN = VIH or VIL	Ind.	_	25	- 25	_	25	
		$\overline{CE} \ge V_{IH}, f = 0$	Auto.	_	_	- 45	_	45	
IsB2	CMOS Standby	V _{DD} = Max.,	Com.	_	10	— 10	_	10	mA
	Current (CMOS Inputs)	$\overline{CE} \ge V_{DD} - 0.2V$,	Ind.	_	15	— 15	_	15	
	, ,	$V_{IN} \ge V_{DD} - 0.2V$, or	Auto.	_	_	- 35	_	35	
		$Vin \leq 0.2V, f = 0$	typ.(2)			2			

^{1.} At f = fmax, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

^{2.} Typical values are measured at $V_{DD} = 3.0V$, $T_A = 25^{\circ}C$ and not 100% tested.



READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

		-	8	-10		
Symbol	Parameter	Min.	Max.	Min. M	lax. Unit	
trc	Read Cycle Time	8	_	10	— ns	
taa	Address Access Time	_	8	_	10 ns	
tона	Output Hold Time	2.5	_	2.5	— ns	
tACE	CE Access Time	_	8	_	10 ns	
t DOE	OE Access Time	_	5.5	_ (6.5 ns	
t HZOE ⁽²⁾	OE to High-Z Output	_	3	_	4 ns	
tLZOE ⁽²⁾	OE to Low-Z Output	0	_	0	— ns	
thzce(2	CE to High-Z Output	0	3	0	4 ns	
tLZCE ⁽²⁾	CE to Low-Z Output	3	_	3	— ns	
tpu	Power Up Time	0	_	0	— ns	
t PD	Power Down Time	_	8	_	10 ns	

^{1.} Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).

^{2.} Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage.



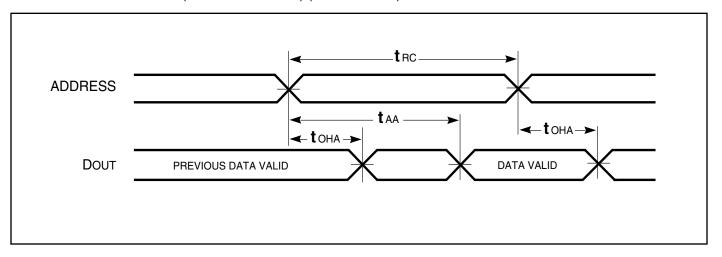
READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

		-20 n	ıs		
Symbol	Parameter	Min.	Max.	Unit	
trc	Read Cycle Time	20	_	ns	
taa	Address Access Time	_	20	ns	
tона	Output Hold Time	2.5	_	ns	
tace	CE Access Time	_	20	ns	
t DOE	OE Access Time	_	8	ns	
thzoe(2)	OE to High-Z Output	0	8	ns	
tLZOE ⁽²⁾	OE to Low-Z Output	0	_	ns	
thzce(2	CE to High-Z Output	0	8	ns	
tLZCE ⁽²⁾	CE to Low-Z Output	3	_	ns	
t PU	Power Up Time	0	_	ns	
t PD	Power Down Time	_	20	ns	

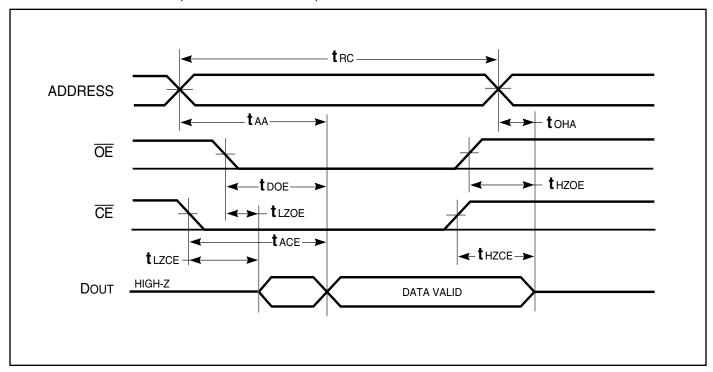
- Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).
 Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
- 3. Not 100% tested.



AC WAVEFORMS READ CYCLE NO. 1(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$)



READ CYCLE NO. 2^(1,3) ($\overline{\text{CE}}$ and $\overline{\text{OE}}$ Controlled)



- 1. WE is HIGH for a Read Cycle.
- The device is continuously selected. OE, CE = VIL.
 Address is valid prior to or coincident with CE LOW transitions.



WRITE CYCLE SWITCHING CHARACTERISTICS(1,3) (Over Operating Range)

		-8		-1(-10	
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
twc	Write Cycle Time	8	_	10	_	ns
tsce	CE to Write End	6.5	_	8	_	ns
taw	Address Setup Time to Write End	6.5	_	8	_	ns
tha	Address Hold from Write End	0	_	0	_	ns
t sa	Address Setup Time	0	_	0	_	ns
tpwe1	$\overline{\text{WE}}$ Pulse Width ($\overline{\text{OE}} = \text{HIGH}$)	6.5	_	8	_	ns
tpwE2	$\overline{\text{WE}}$ Pulse Width $(\overline{\text{OE}} = \text{LOW})$	8.0	_	10	_	ns
tsd	Data Setup to Write End	5	_	6	_	ns
t HD	Data Hold from Write End	0	_	0	_	ns
thzwe ⁽²⁾	WE LOW to High-Z Output	_	3.5	_	5	ns
tLZWE ⁽²⁾	WE HIGH to Low-Z Output	2	_	2	_	ns

^{1.} Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).

^{2.} Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

^{3.} The internal write time is defined by the overlap of CE LOW and WE LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development



WRITE CYCLE SWITCHING CHARACTERISTICS(1,2) (Over Operating Range)

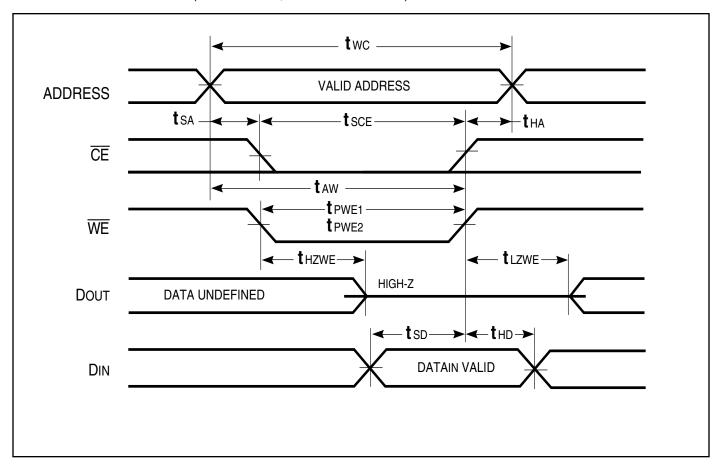
		-20) ns	
Symbol	Parameter	Min.	Max.	Unit
twc	Write Cycle Time	20	_	ns
tsce	CE to Write End	12	_	ns
taw	Address Setup Time to Write End	12	_	ns
tha	Address Hold from Write End	0	_	ns
t sa	Address Setup Time	0	_	ns
tpwE1	$\overline{\text{WE}}$ Pulse Width ($\overline{\text{OE}}$ = HIGH)	12	_	ns
tpwE2	$\overline{\text{WE}}$ Pulse Width ($\overline{\text{OE}}$ = LOW)	17	_	ns
tsp	Data Setup to Write End	9	_	ns
thd	Data Hold from Write End	0	_	ns
thzwe ⁽²⁾	WE LOW to High-Z Output	_	9	ns
tLZWE ⁽²⁾	WE HIGH to Low-Z Output	3	_	ns

- 1. Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).
- Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
- 3. The internal write time is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.



AC WAVEFORMS

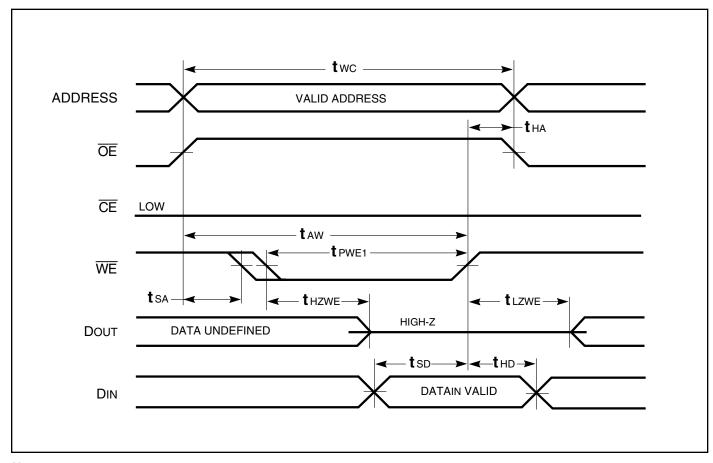
WRITE CYCLE NO. $1^{(1,2)}$ (\overline{CE} Controlled, \overline{OE} = HIGH or LOW)





AC WAVEFORMS

WRITE CYCLE NO. 2^(1,2) (WE Controlled: OE is HIGH During Write Cycle)

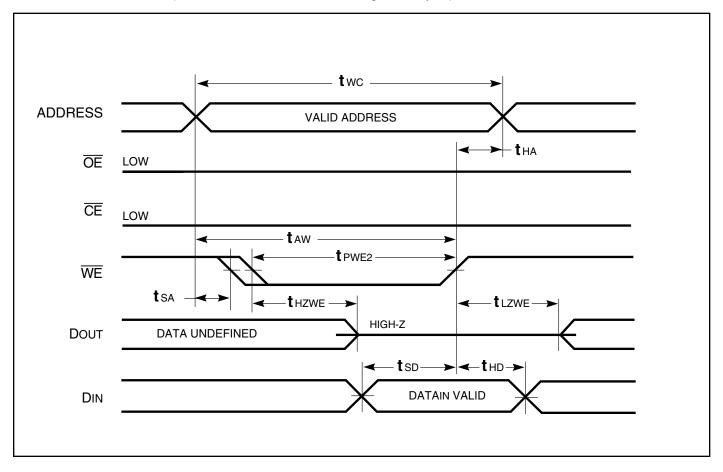


- 1. The internal write time is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
- 2. I/O will assume the High-Z state if $\overline{OE} > V_{IH}$.



AC WAVEFORMS

WRITE CYCLE NO. 3 (WE Controlled: OE is LOW During Write Cycle)



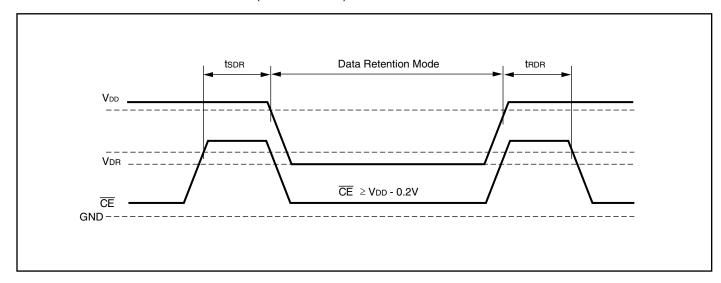


DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{DR}	VDD for Data Retention	See Data Retention Waveform		2.0	_	3.6	V
IDR	Data Retention Current	$V_{DD} = 2.0V, \overline{CE} \geq V_{DD} - 0.2V$	Com.	_	2	10	mA
			Ind. Auto.	_	_	15 35	
tsdr	Data Retention Setup Time	See Data Retention Waveform		0	_	_	ns
trdr	Recovery Time	See Data Retention Waveform		trc	_	_	ns

Note 1: Typical values are measured at VDD = VDR(min), TA = 25°C and not 100% tested.

DATA RETENTION WAVEFORM (CE Controlled)





ORDERING INFORMATION

Industrial Range: -40°C to +85°C Voltage Range: 2.4V to 3.6V

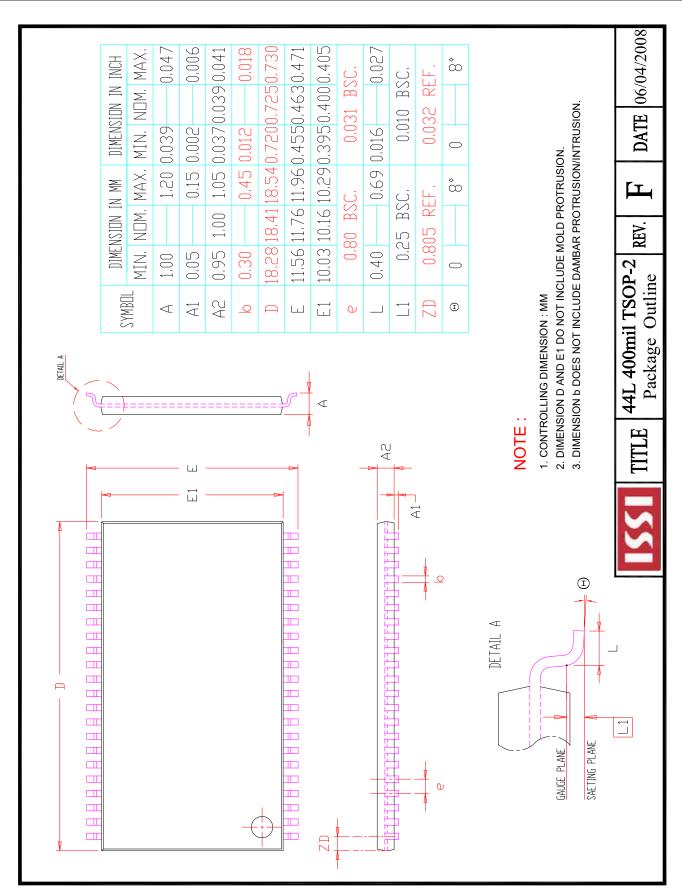
Speed (ns)	Order Part No.	Package
8	IS61WV10248EDBLL-8BLI	48 mini BGA (6mm x 8mm), Lead-free
	IS61WV10248EDBLL-8TLI	TSOP (Type II), Lead-free
10	IS61WV10248EDBLL-10BI	48 mini BGA (6mm x 8mm)
	IS61WV10248EDBLL-10BLI	48 mini BGA (6mm x 8mm), Lead-free
	IS61WV10248EDBLL-10TI	TSOP (Type II)
	IS61WV10248EDBLL-10TLI	TSOP (Type II), Lead-free

Automotive Range: -40°C to +125°C

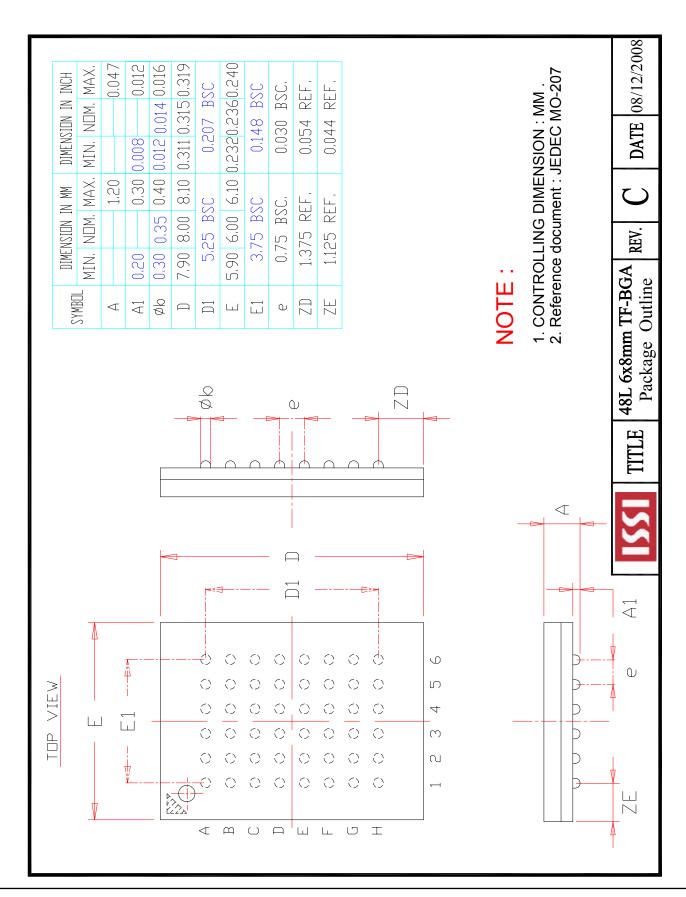
Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10	IS64WV10248EDBLL-10BA3	48 mini BGA (6mm x 8mm)
	IS64WV10248EDBLL-10BLA3	48 mini BGA (6mm x 8mm), Lead-free
	IS64WV10248EDBLL-10CTA3	TSOP (Type II), Copper Leadframe
	IS64WV10248EDBLL-10CTLA	3 TSOP (Type II), Lead-free, Copper Leadframe









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