IS62C51216AL
IS65C51216AL

512K x 16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

DECEMBER 2010

FEATURES

- High-speed access time: 45ns, 55ns
- CMOS low power operation
  - 36 mW (typical) operating
  - 12 µW (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
  - 4.5V--5.5V V_{DD}
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Automotive temperature (-40°C to +125°C)
- Lead-free available

DESCRIPTION

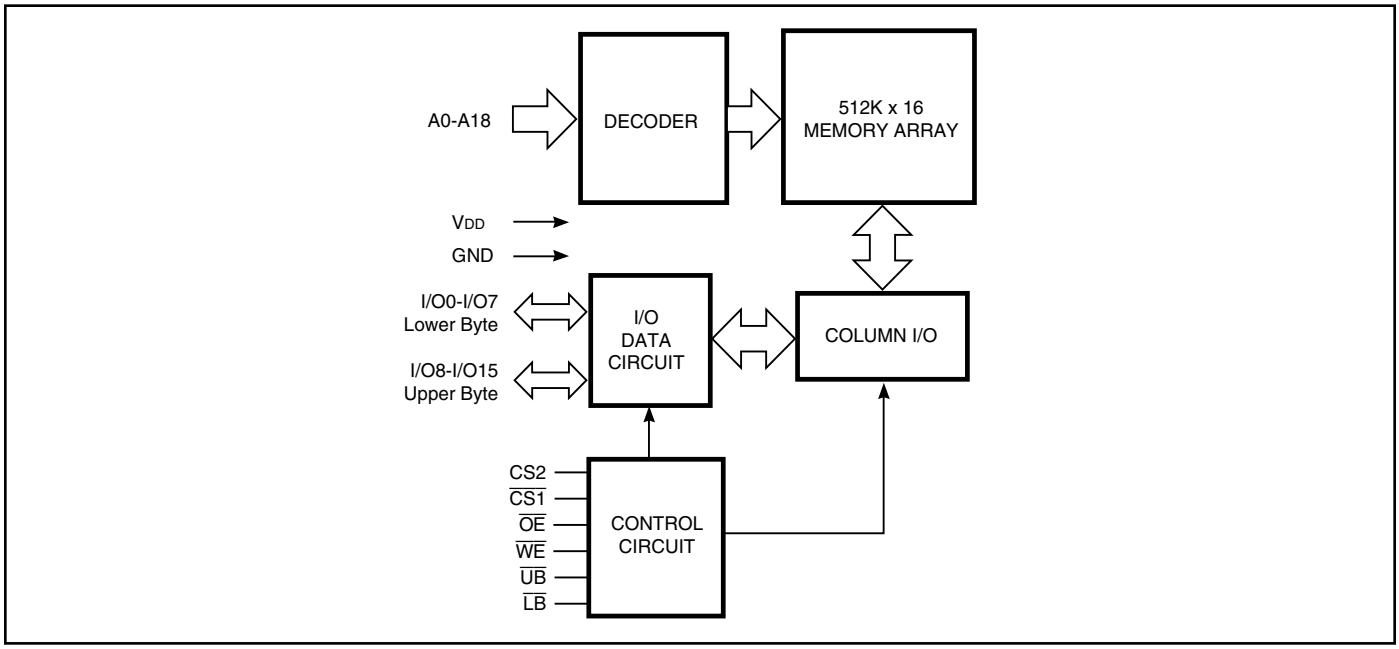
The *ISSI* IS62C51216AL and IS65C51216AL are high-speed, 8M bit static RAMs organized as 512K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) or when CS2 is LOW (deselected) or when $\overline{CS1}$ is LOW, CS2 is HIGH and both $\overline{LB}$ and $\overline{UB}$ are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

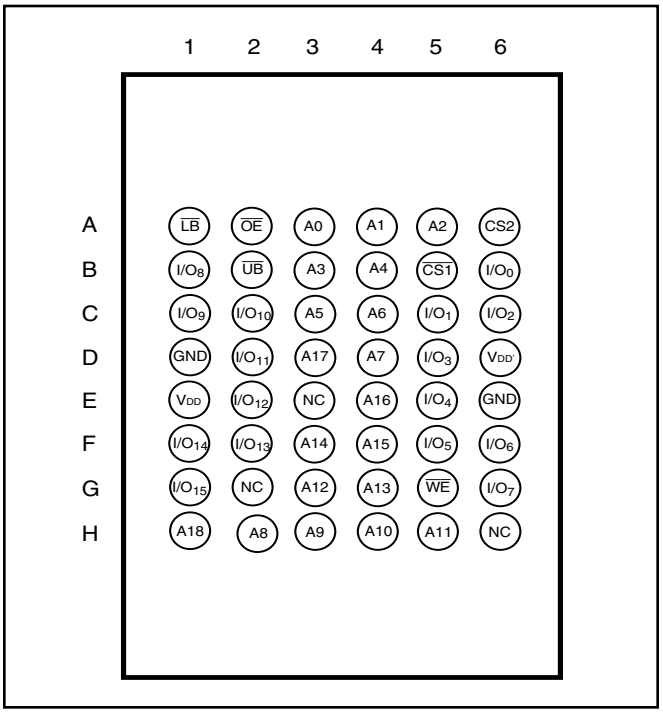
The IS62C51216AL and IS65C51216AL are packaged in the JEDEC standard 48-pin mini BGA (9mm x 11mm) and 44-Pin TSOP (TYPE II).

FUNCTIONAL BLOCK DIAGRAM

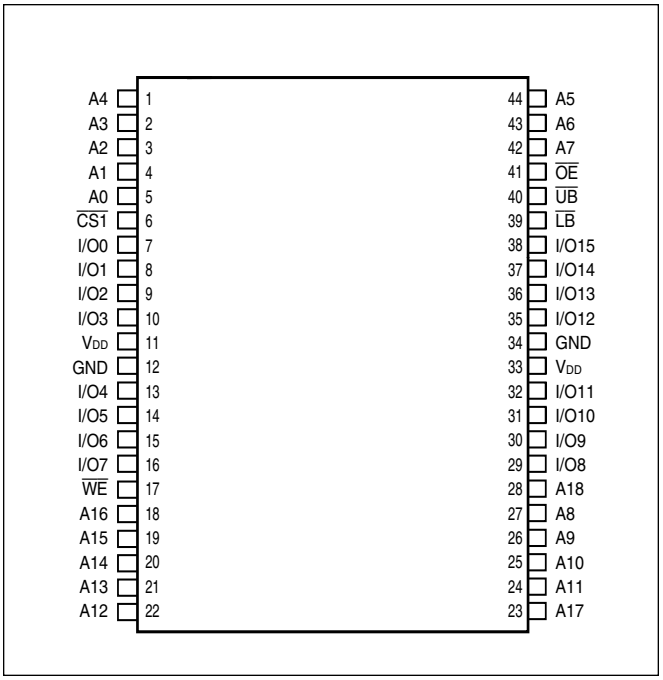


PIN CONFIGURATIONS

48-Pin mini BGA (9mmx11mm)



44-Pin TSOP (Type II)



PIN DESCRIPTIONS

A0-A18	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CS1}$, CS2	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V_{DD}	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN I/O0-I/O7	I/O PIN I/O8-I/O15	V_{DD} Current
Not Selected	X	H	X	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	X	X	L	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	X	X	X	X	H	H	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	H	L	X	High-Z	High-Z	I_{CC}
	H	L	H	H	X	L	High-Z	High-Z	I_{CC}
Read	H	L	H	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	H	L	H	L	High-Z	D_{OUT}	
	H	L	H	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	H	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	H	X	H	L	High-Z	D_{IN}	
	L	L	H	X	L	L	D_{IN}	D_{IN}	

OPERATING RANGE (V_{DD})

Range	Ambient Temperature	VDD	Speed
Commercial	0°C to +70°C	4.5V - 5.5V	45ns
Industrial	–40°C to +85°C	4.5V - 5.5V	55ns
Automotive	–40°C to +125°C	4.5V - 5.5V	55ns

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 2.1 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{DD} + 0.5	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	Com.	–1	1	µA
			Ind.	–2	2	
			Auto.	–5	5	
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}	Com.	–1	1	µA
		Outputs Disabled	Ind.	–2	2	
			Auto.	–5	5	

Note:
1. V_{IL} (min) = -0.3V DC; V_{IL} (min) = -2.0V AC (pulse width -2.0 ns). Not 100% tested.
   V_{IH} (max) = V_{DD} + 0.3V DC; V_{IH} (max) = V_{DD} + 2.0V AC (pulse width -2.0 ns). Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

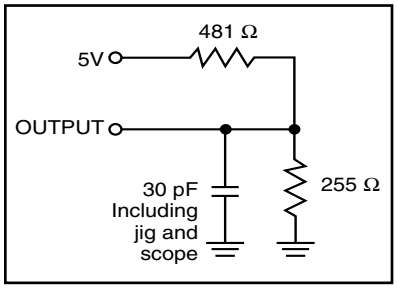


Figure 1

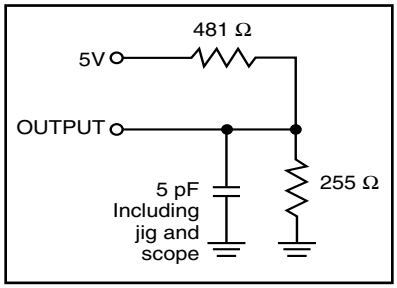


Figure 2

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-45 ns Min.	-45 ns Max.	-55 ns Min.	-55 ns Max.	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., $\overline{CE}$ = V_{IL}	Com.	—	25			mA
		I_{OUT} = 0 mA, f = f_{MAX}	Ind.			—	25	
		V_{IN} = V_{IH} or V_{IL}	Auto.			—	40	
			typ.[2]	13		12		
$I_{CC}1$	Average operating Current	$\overline{CE}$ = V_{IL},	Com.	—	10			mA
		V_{IN} = V_{IH} or V_{IL},	Ind.			—	10	
		$I_{I/O}$= 0 mA	Auto.			—	20	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max.,	Com.	—	1			mA
		V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ ≥ V_{IH},	Ind.			—	1.5	
		f = 0	Auto.			—	2	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max.,	Com.	—	40			µA
		$\overline{CE}$ ≥ V_{DD} – 0.2V,	Ind.			—	60	
		V_{IN} ≥ V_{DD} – 0.2V,	Auto.			—	180	
		or V_{IN} ≤ V_{SS} + 0.2V, f = 0	typ.[2]	15				

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical Values are measured at Vcc = 5V, T_A = 25°C and not 100% tested.

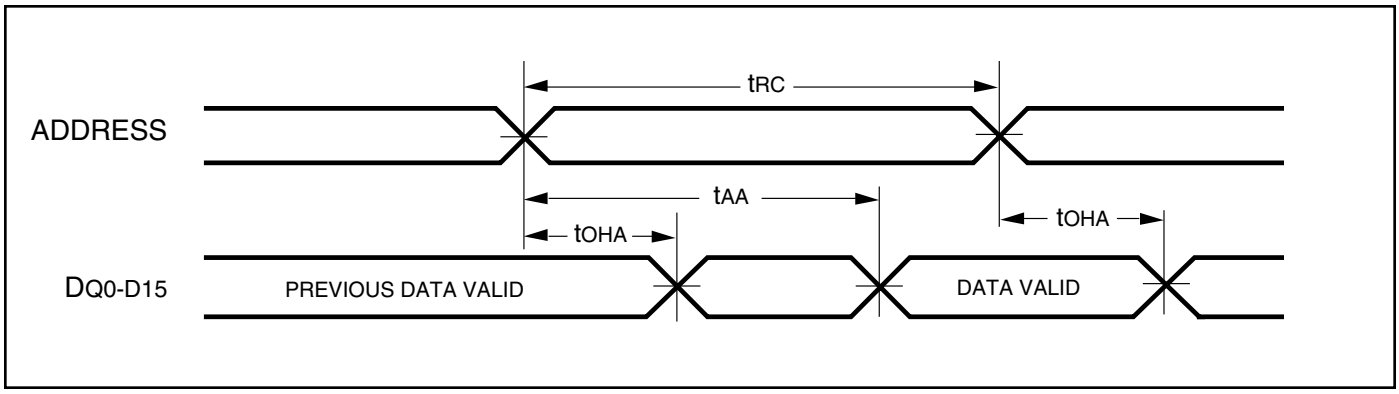
READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	45 ns Min.	45 ns Max.	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	Unit
t_{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	ns
t_{OHA}[3]	Output Hold Time	10	—	10	—	10	—	ns
t_{ACS1}/t_{ACS2}	$\overline{CS1}$/CS2 Access Time	—	45	—	55	—	70	ns
t_{DOE}	$\overline{OE}$ Access Time	—	20	—	25	—	35	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	15	—	20	—	25	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	5	—	ns
t_{HZCS1}/t_{HZCS2}[2]	$\overline{CS1}$/CS2 to High-Z Output	0	15	0	20	0	25	ns
t_{LZCS1}/t_{LZCS2}[2]	$\overline{CS1}$/CS2 to Low-Z Output	10	—	10	—	10	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	45	—	55	—	70	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	15	0	20	0	25	ns
t_{LZB}	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. 10ns for CMOS Loading. 8ns @ AC Loading.

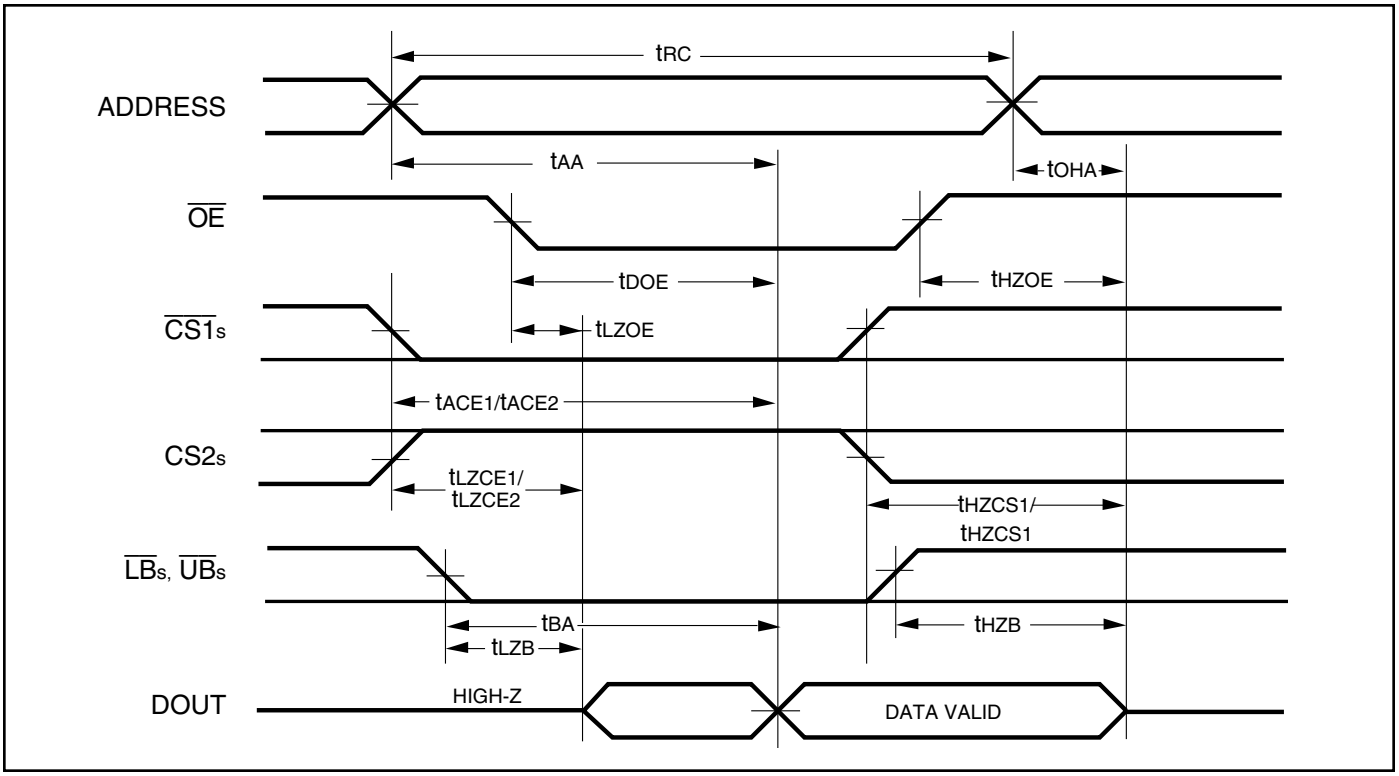
AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CS1}$ = $\overline{OE}$ = V_{IL}, CS2 = $\overline{WE}$ = V_{IH}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



AC WAVEFORMS

READ CYCLE NO. 2[1,3] ($\overline{CS1}$, CS2, $\overline{OE}$, AND $\overline{UB}$/$\overline{LB}$ Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS1}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}. CS2=$\overline{WE}$=V_{IH}.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

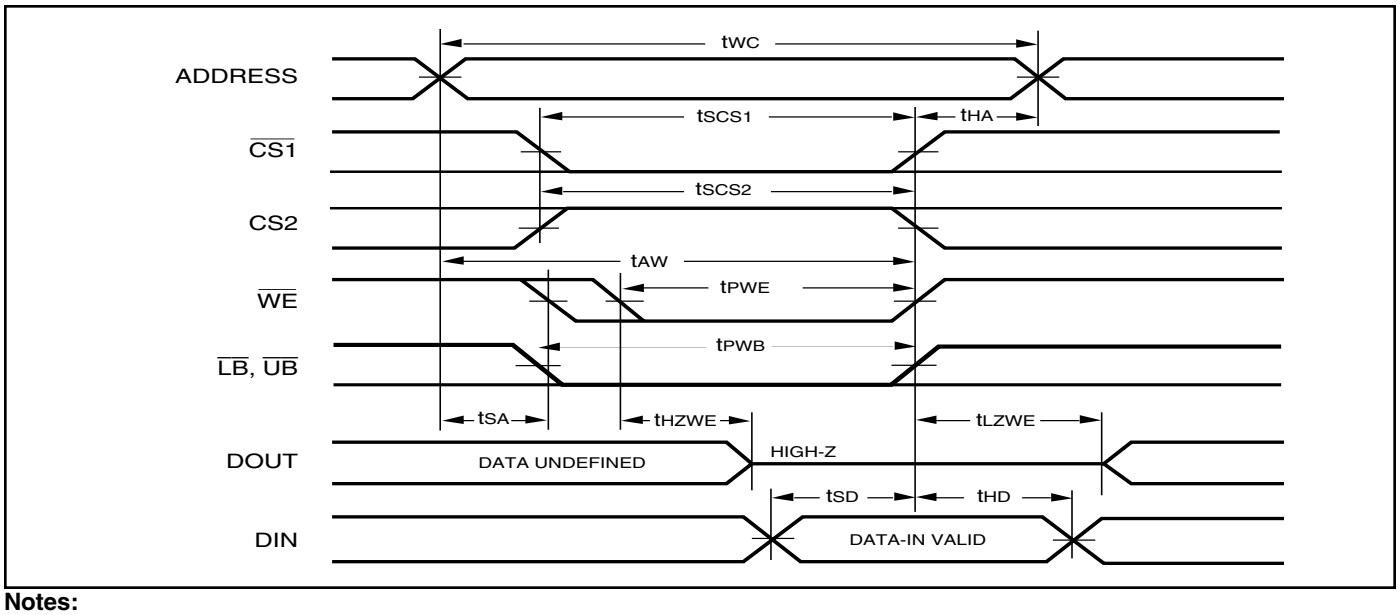
Symbol	Parameter	45ns Min.	45ns Max.	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	Unit
t_{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t_{SCS1}/t_{SCS2}	$\overline{CS1}$/CS2 to Write End	35	—	45	—	60	—	ns
t_{AW}	Address Setup Time to Write End	35	—	45	—	60	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	35	—	45	—	60	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	35	—	40	—	50	—	ns
t_{SD}	Data Setup to Write End	25	—	30	—	30	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	20	—	20	—	30	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW, CS2 HIGH and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
4. $t_{PWE} > t_{HZWE} + t_{SD}$ when $\overline{OE}$ is LOW.

AC WAVEFORMS

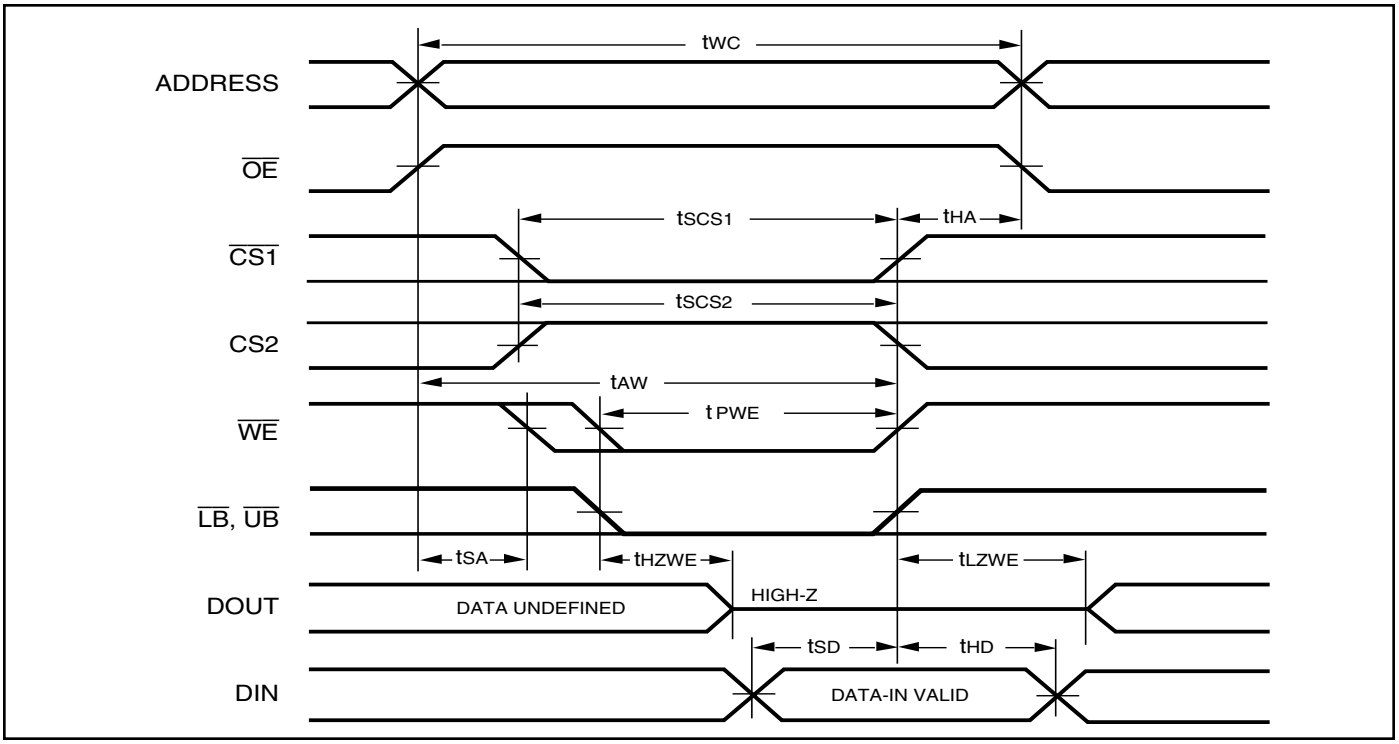
WRITE CYCLE NO. 1[1,2] ($\overline{CS1}$ Controlled, $\overline{OE}$ = HIGH or LOW)



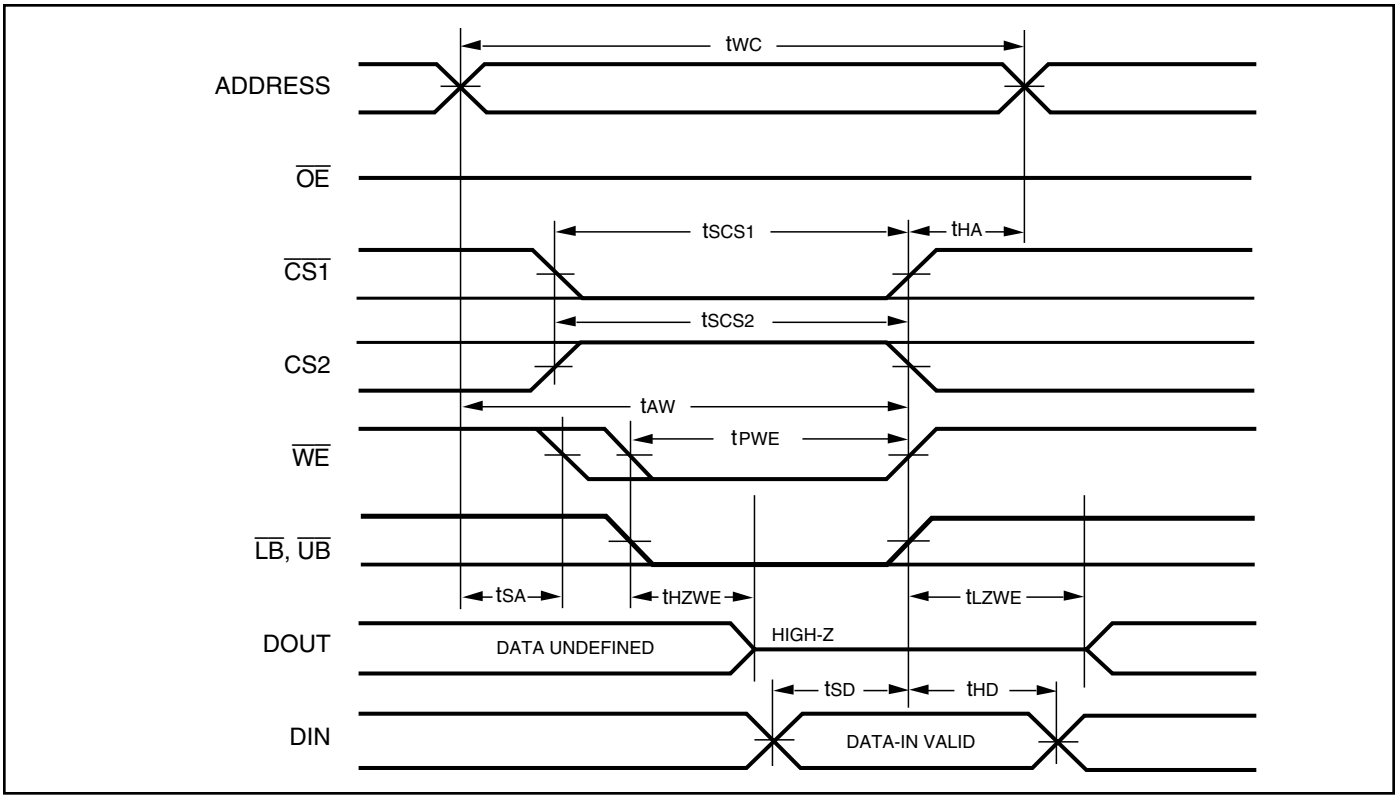
Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CS1}$, CS2 and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CS1}$) [($\overline{LB}$) = ($\overline{UB}$)] ($\overline{WE}$).

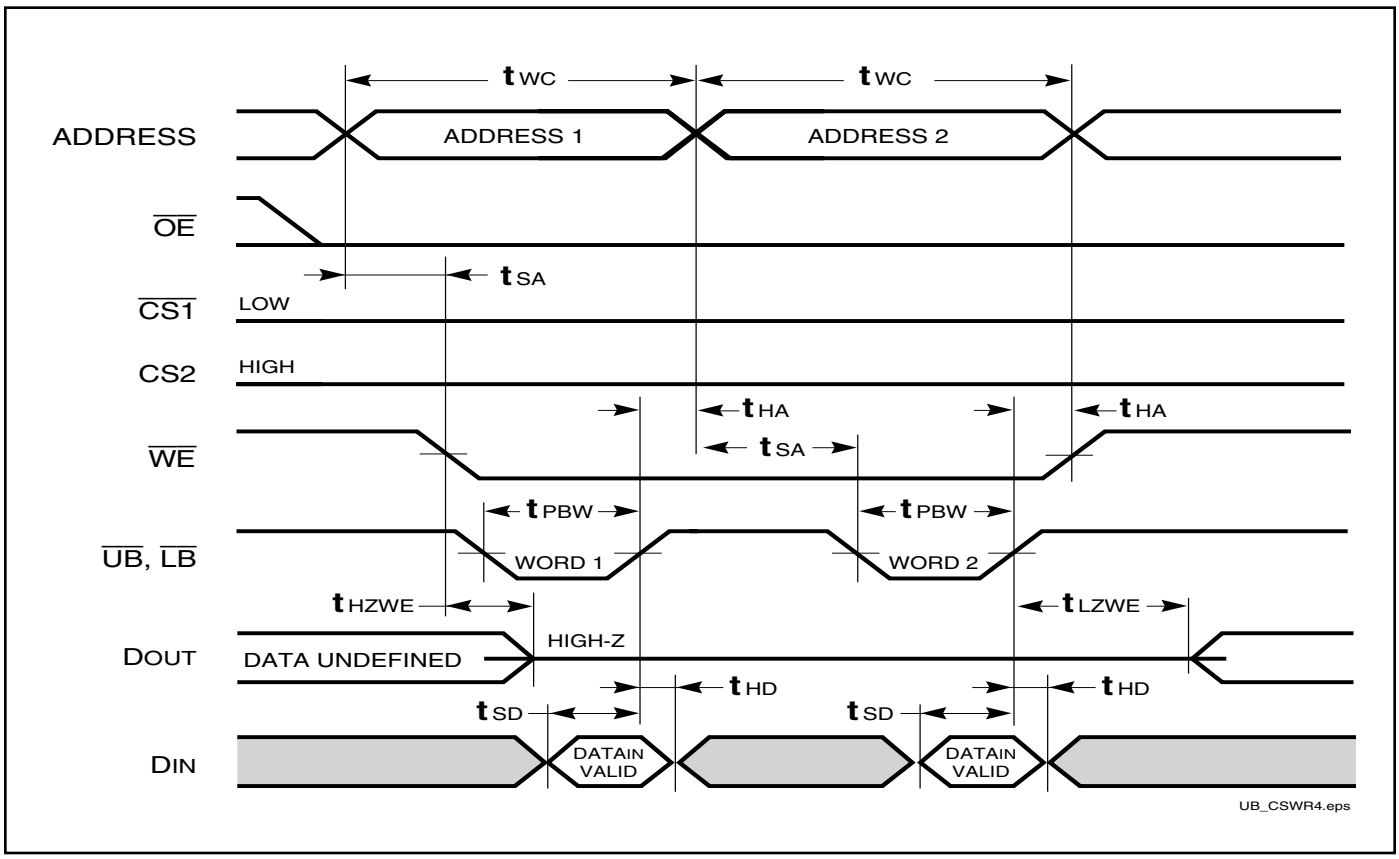
WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



WRITE CYCLE NO. 4 ($\overline{UB}$/$\overline{LB}$ Controlled)

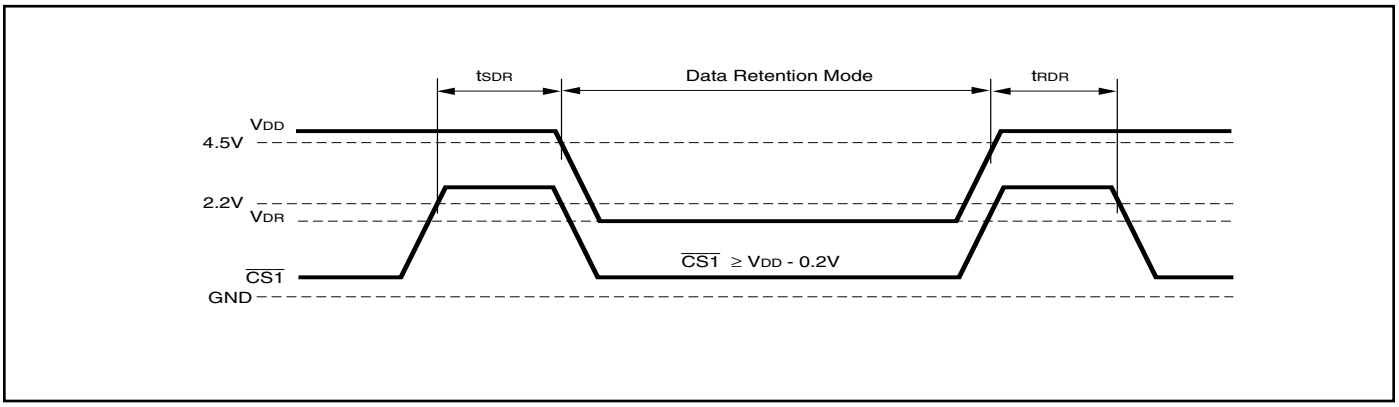


DATA RETENTION SWITCHING CHARACTERISTICS (4.5V - 5.5V)

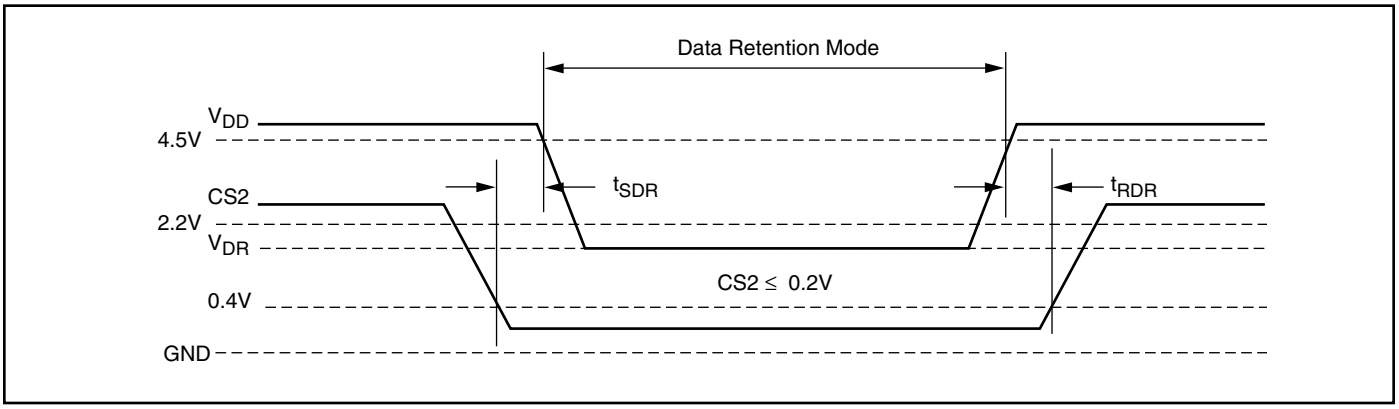
Symbol	Parameter	Test Condition		Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0		5.5	V
I_{DR}	Data Retention Current	V_{DD} = 2.0V and		—		20	µA
		$\overline{CS1} \geq V_{DD} - 0.2V$ and	Com.	—	15	40	
		(a) $CS2 \geq V_{DD} - 0.2V$ or	Ind.	—	—	60	
		(b) $CS2 \leq GND + 0.2V$	Auto.	—	—	180	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0		—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}		—	ns

Note:
1. Typical Values are measured at Vcc = 5V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM (CS2 Controlled)



IS62C51216AL (4.5V - 5.5V)
Industrial Range: –40°C to +85°C

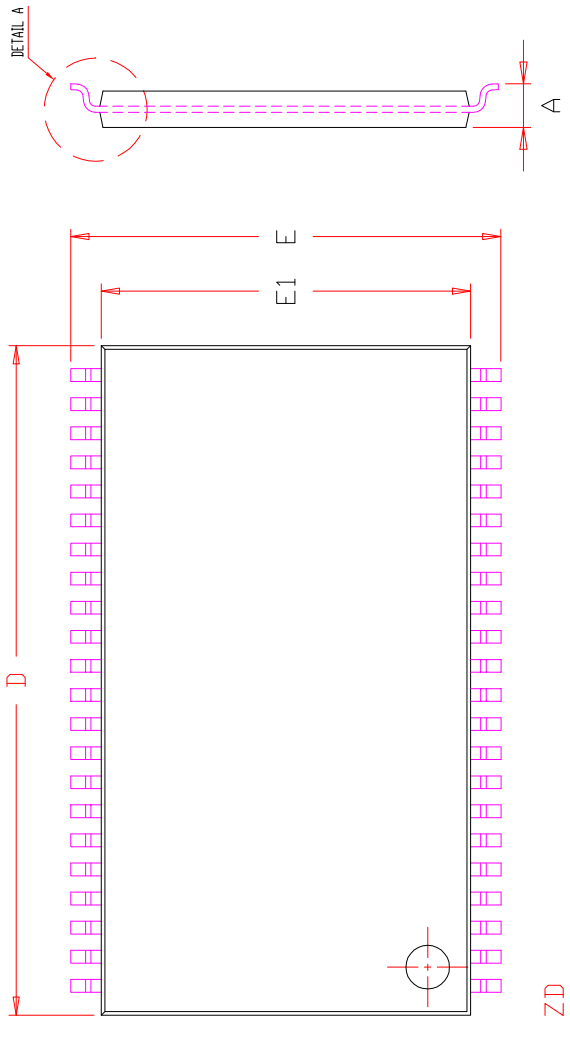
Speed (ns)	Order Part No.*	Package
55	IS62C51216AL-55TLI	TSOP-II, Lead-free
	IS62C51216AL-55MLI	mini BGA, Lead-free (9mmx11mm)

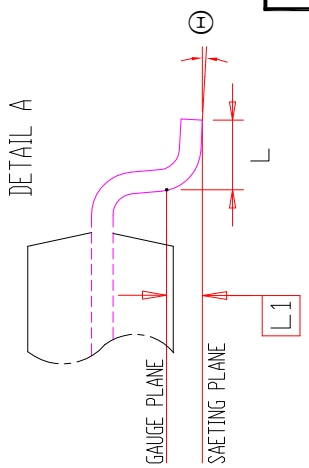
*Devices will meet 45ns when used in 0ºC to +70ºC temperature range.

IS65C51216AL (4.5V - 5.5V)
Automotive Range: –40°C to +125°C

Speed (ns)	Order Part No.	Package
55	IS65C51216AL-55CTLA3	TSOP-II, Lead-free, Copper Lead-frame
	IS65C51216AL-55MLA3	mini BGA, Lead-free (9mmx11mm)

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	—	1.20	0.039	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	—	0.45	0.012	—	0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80 BSC.			0.031 BSC.		
L	0.40	—	0.69	0.016	—	0.027
L1	0.25 BSC.			0.010 BSC.		
ZD	0.805 REF.			0.032 REF.		
Θ	0	—	8°	0	—	8°





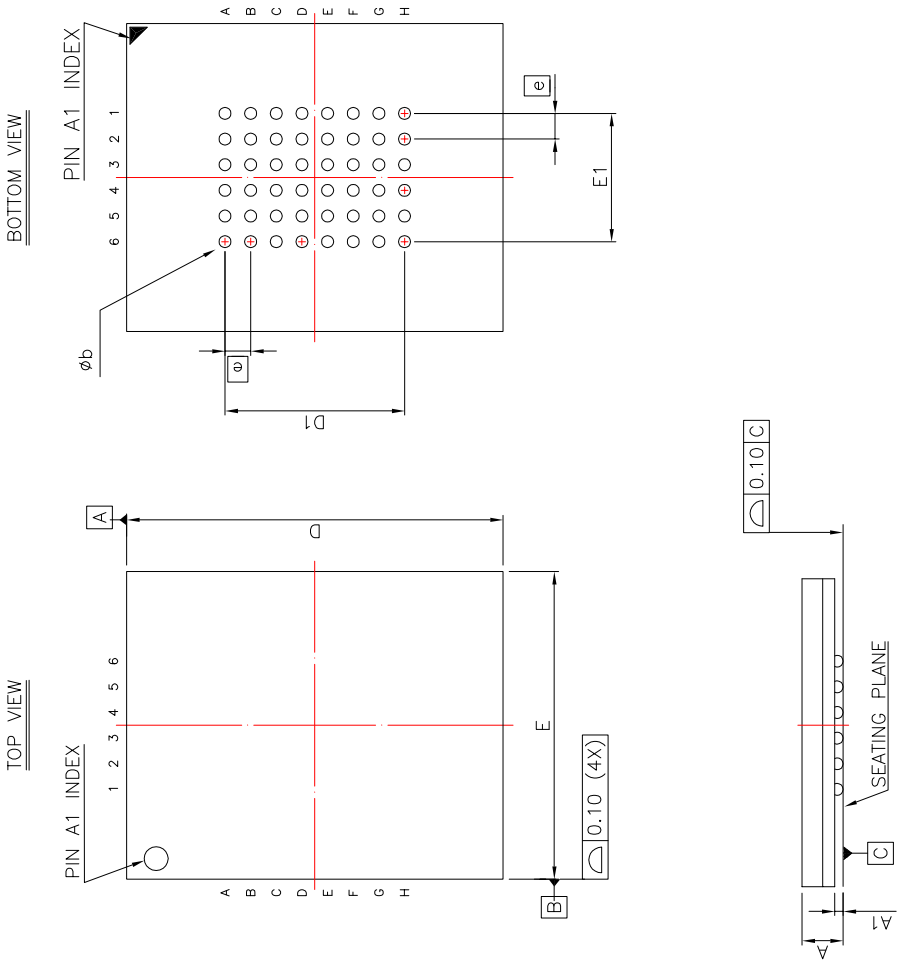
NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

	TITLE	44L 400mil TSOP-2 Package Outline	REV.	F	DATE	06/04/2008

SYM.	DIMENSION (mm)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.20	—	0.30	0.008	—	0.012
b	0.30	0.35	0.40	0.012	0.014	0.016
D	10.90	11.00	11.10	0.429	0.433	0.437
D1	5.25 BSC			0.207 BSC		
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	3.75 BSC			0.148 BSC		
e	0.75 BSC			0.030 BSC		

NOTE :
1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207



ISSI	TITLE	48L 9x11mm TF-BGA Package Outline	REV.	B	DATE	08/21/2008

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