

# 128K x 8 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

NOVEMBER 2016

## FEATURES

- High-speed access time: 35ns, 45ns, 55ns
- CMOS low power operation:
  - 12 mW (typical) operating
  - 4  $\mu$ W (typical) CMOS standby
- TTL compatible interface levels
- Single power supply:
  - 1.65V--2.2V  $V_{DD}$  (62WV1288DALL)
  - 2.3V--3.6V  $V_{DD}$  (62WV1288DBLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial and automotive temperature support
- Lead-free available

## DESCRIPTION

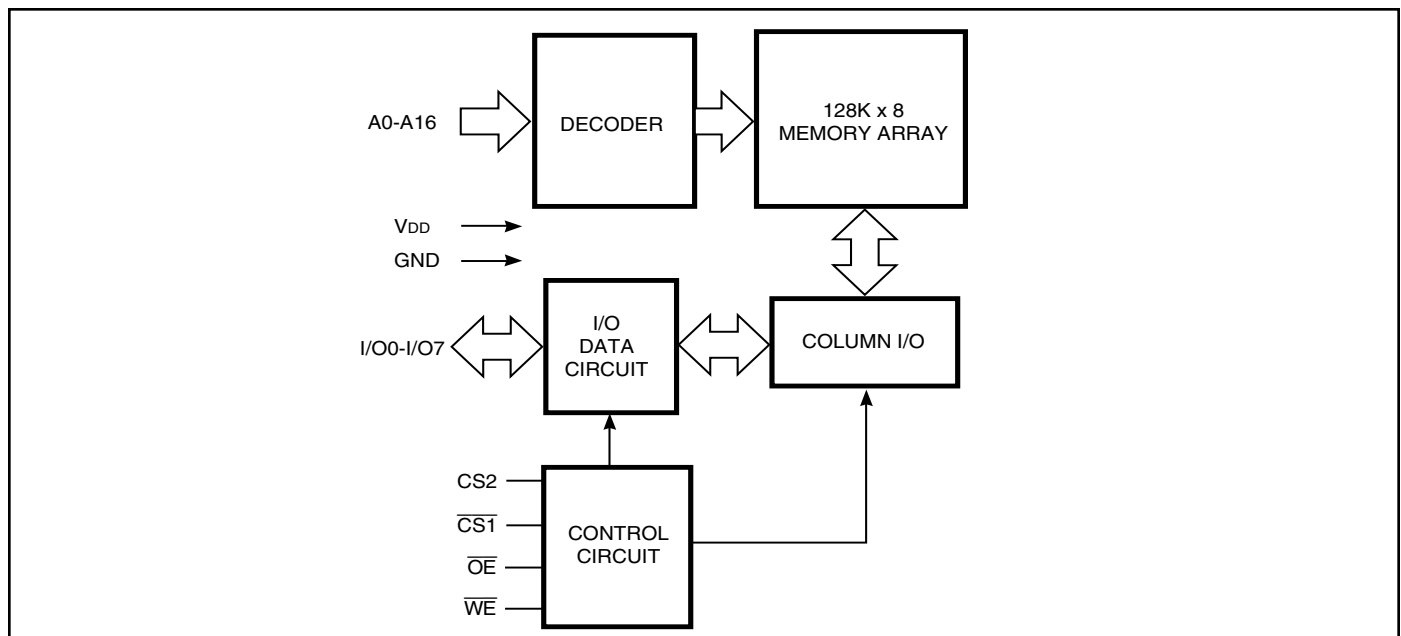
The *ISSI* IS62/65WV1288DALL and IS62/65WV1288DBLL are high-speed, 1M bit static RAMs organized as 128K words by 8 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When  $\overline{CS1}$  is HIGH (deselected) or when CS2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory.

The IS62/65WV1288DALL and IS62/65WV1288DBLL are packaged in the JEDEC standard 32-pin TSOP (TYPEI), sTSOP (TYPEI), SOP, and 36-pin mini BGA.

## FUNCTIONAL BLOCK DIAGRAM



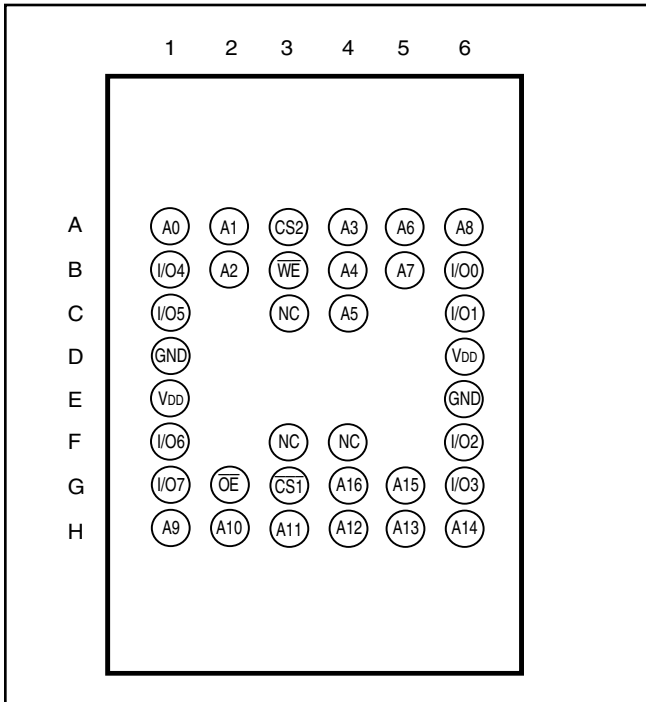
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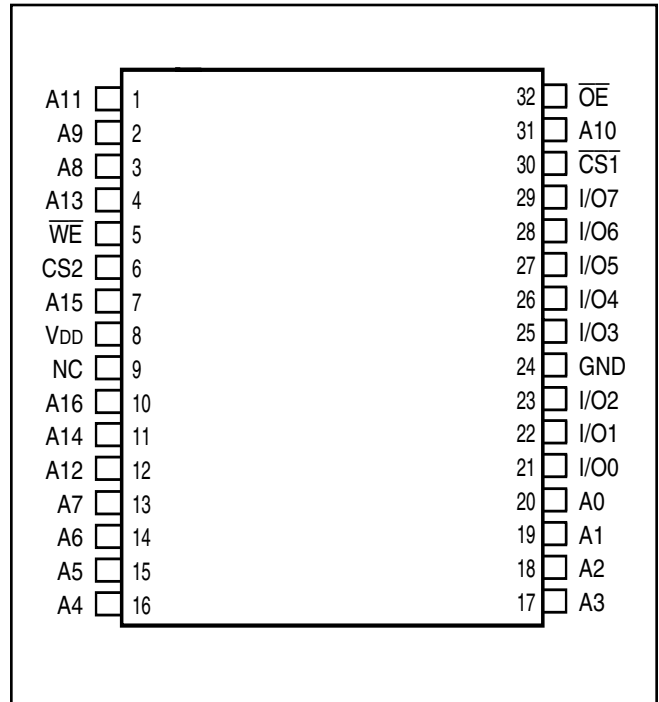
- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

**PIN CONFIGURATION**

**36-pin mini BGA (B) (6mm x 8mm)**



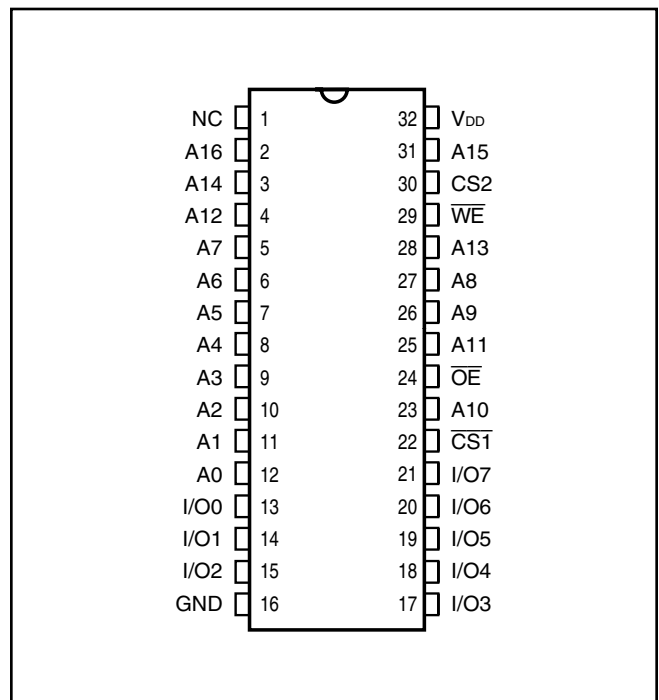
**32-pin TSOP (TYPE I) (T),  
32-pin sTSOP (TYPE I) (H)**



**PIN DESCRIPTIONS**

A0-A16	Address Inputs
CS1	Chip Enable 1 Input
CS2	Chip Enable 2 Input
OE	Output Enable Input
WE	Write Enable Input
I/O0-I/O7	Input/Output
NC	No Connection
VDD	Power
GND	Ground

**32-pin SOP (Q)**



**TRUTH TABLE**

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	I/O Operation	V <sub>DD</sub> Current
Not Selected	X	H	X	X	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
(Power-down)	X	X	L	X	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
Output Disabled	H	L	H	H	High-Z	I <sub>CC</sub>
Read	H	L	H	L	D <sub>OUT</sub>	I <sub>CC</sub>
Write	L	L	H	X	D <sub>IN</sub>	I <sub>CC</sub>

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to V <sub>DD</sub> + 0.5	V
V <sub>DD</sub>	V <sub>DD</sub> Relates to GND	-0.3 to 4.0	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W

**Notes:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**CAPACITANCE<sup>(1,2)</sup>**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>OUT</sub> = 0V	8	pF

**Notes:**

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>DD</sub> = 3.3V.

### AC TEST CONDITIONS

Parameter	Unit (2.3V-3.6V)	Unit (3.3V ± 5%)	Unit (1.65V-2.2V)
Input Pulse Level	0.4V to $V_{DD} - 0.3V$	0.4V to $V_{DD} - 0.3V$	0.4V to $V_{DD} - 0.3V$
Input Rise and Fall Times	1V/ ns	1V/ ns	1V/ ns
Input and Output Timing and Reference Level ( $V_{Ref}$ )	$V_{DD} / 2$	$\frac{V_{DD}}{2} + 0.05$	0.9V
Output Load	See Figures 1 and 2	See Figures 1 and 2	See Figures 1 and 2
R1 ( $\Omega$ )	317	317	13500
R2 ( $\Omega$ )	351	351	10800
$V_{TM}$ (V)	3.3V	3.3V	1.8V

### AC TEST LOADS

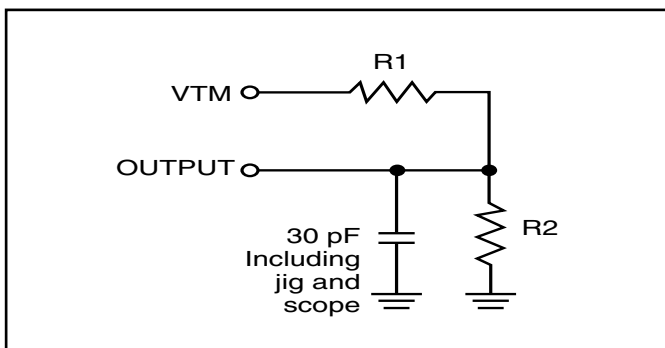


Figure 1.

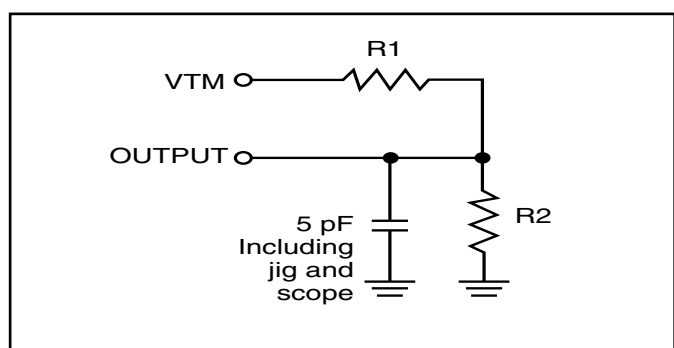


Figure 2.

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

$V_{DD} = 3.3V \pm 5\%$

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$V_{DD} = \text{Min.}, I_{OH} = -1 \text{ mA}$	2.4	—	V
$V_{OL}$	Output LOW Voltage	$V_{DD} = \text{Min.}, I_{OL} = 2.1 \text{ mA}$	—	0.4	V
$V_{IH}$	Input HIGH Voltage		2	$V_{DD} + 0.3$	V
$V_{IL}$	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V
$I_{LI}$	Input Leakage	$GND \leq V_{IN} \leq V_{DD}$	-1	1	$\mu\text{A}$
$I_{LO}$	Output Leakage	$GND \leq V_{OUT} \leq V_{DD}$ , Outputs Disabled	-1	1	$\mu\text{A}$

**Note:**

- $V_{IL}$  (min.) = -0.3V DC;  $V_{IL}$  (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.  
 $V_{IH}$  (max.) =  $V_{DD} + 0.3V$  DC;  $V_{IH}$  (max.) =  $V_{DD} + 2.0V$  AC (pulse width < 10 ns). Not 100% tested.

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

$V_{DD} = 2.3V-3.6V$

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$V_{DD} = \text{Min.}, I_{OH} = -1.0 \text{ mA}$	1.8	—	V
$V_{OL}$	Output LOW Voltage	$V_{DD} = \text{Min.}, I_{OL} = 2.1 \text{ mA}$	—	0.4	V
$V_{IH}$	Input HIGH Voltage		2.0	$V_{DD} + 0.3$	V
$V_{IL}$	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V
$I_{LI}$	Input Leakage	$GND \leq V_{IN} \leq V_{DD}$	-1	1	$\mu\text{A}$
$I_{LO}$	Output Leakage	$GND \leq V_{OUT} \leq V_{DD}$ , Outputs Disabled	-1	1	$\mu\text{A}$

**Note:**

- $V_{IL}$  (min.) = -0.3V DC;  $V_{IL}$  (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.  
 $V_{IH}$  (max.) =  $V_{DD} + 0.3V$  DC;  $V_{IH}$  (max.) =  $V_{DD} + 2.0V$  AC (pulse width < 10 ns). Not 100% tested.

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

$V_{DD} = 1.65V-2.2V$

Symbol	Parameter	Test Conditions	$V_{DD}$	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -0.1 \text{ mA}$	1.65-2.2V	1.4	—	V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 0.1 \text{ mA}$	1.65-2.2V	—	0.2	V
$V_{IH}$	Input HIGH Voltage		1.65-2.2V	1.4	$V_{DD} + 0.2$	V
$V_{IL}^{(1)}$	Input LOW Voltage		1.65-2.2V	-0.2	0.4	V
$I_{LI}$	Input Leakage	$GND \leq V_{IN} \leq V_{DD}$		-1	1	$\mu\text{A}$
$I_{LO}$	Output Leakage	$GND \leq V_{OUT} \leq V_{DD}$ , Outputs Disabled		-1	1	$\mu\text{A}$

**Note:**

- $V_{IL}$  (min.) = -0.3V DC;  $V_{IL}$  (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.  
 $V_{IH}$  (max.) =  $V_{DD} + 0.3V$  DC;  $V_{IH}$  (max.) =  $V_{DD} + 2.0V$  AC (pulse width < 10 ns). Not 100% tested.

**OPERATING RANGE (V<sub>DD</sub>)**

Range	Ambient Temperature	V <sub>DD</sub>	Speed
Commercial	0°C to +70°C	1.65V-2.2V	45ns
Industrial	-40°C to +85°C	1.65V-2.2V	55ns
Automotive	-40°C to +125°C	1.65V-2.2V	55ns

**OPERATING RANGE (V<sub>DD</sub>)**

Range	Ambient Temperature	V <sub>DD</sub> (45 ns)	V <sub>DD</sub> (35 ns)
Commercial	0°C to +70°C	2.3V-3.6V	3.3V±5%
Industrial	-40°C to +85°C	2.3V-3.6V	3.3V±5%

**OPERATING RANGE (V<sub>DD</sub>)**

Range	Ambient Temperature	V <sub>DD</sub> (45 ns)
Automotive	-40°C to +125°C	2.3V-3.6V

**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)**

Symbol	Parameter	Test Conditions		-35		-45		-55		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>CC</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max.,	Com.	—	8	—	6	—	5	mA
		I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Ind.	—	12	—	8	—	7	
		$\overline{CS1} = V_{IL}$	Auto.	—	15	—	12	—	12	
		V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.4V	typ. <sup>(2)</sup>	4						
I <sub>CC1</sub>	Operating Supply Current	V <sub>DD</sub> = Max.,	Com.	—	2.5	—	2.5	—	2.5	mA
		I <sub>OUT</sub> = 0 mA, f = 0	Ind.	—	2.5	—	2.5	—	2.5	
		$\overline{CS1} = V_{IL}$	Auto.	—	3	—	3	—	3	
		V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.4V								
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max.,	Com.	—	2	—	2	—	2	μA
		$\overline{CS1} \geq V_{DD} - 0.2V$ ,	Ind.	—	4	—	4	—	4	
		V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or	Auto.	—	18	—	18	—	18	
		V <sub>IN</sub> ≤ 0.2V, f = 0	typ. <sup>(2)</sup>	0.6						

**Note:**

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

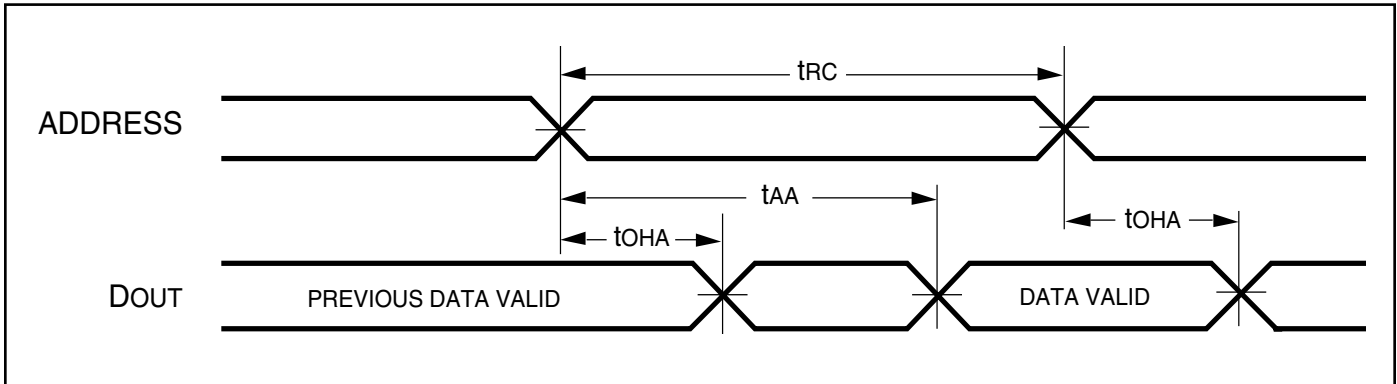
Symbol	Parameter	35 ns		45 ns		55 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	35	—	45	—	55	—	ns
t <sub>AA</sub>	Address Access Time	—	35	—	45	—	55	ns
t <sub>OHA</sub>	Output Hold Time	10	—	10	—	10	—	ns
t <sub>ACS1</sub> /t <sub>ACS2</sub>	$\overline{CS1}/\overline{CS2}$ Access Time	—	35	—	45	—	55	ns
t <sub>DOE</sub>	$\overline{OE}$ Access Time	—	10	—	20	—	25	ns
t <sub>HZOE<sup>(2)</sup></sub>	$\overline{OE}$ to High-Z Output	—	10	—	15	—	20	ns
t <sub>LZOE<sup>(2)</sup></sub>	$\overline{OE}$ to Low-Z Output	3	—	5	—	5	—	ns
t <sub>HZCS1</sub> /t <sub>HZCS2<sup>(2)</sup></sub>	$\overline{CS1}/\overline{CS2}$ to High-Z Output	0	10	0	15	0	20	ns
t <sub>LZCS1</sub> /t <sub>LZCS2<sup>(2)</sup></sub>	$\overline{CS1}/\overline{CS2}$ to Low-Z Output	5	—	10	—	10	—	ns

**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V<sub>DD</sub>-0.2V/V<sub>DD</sub>-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

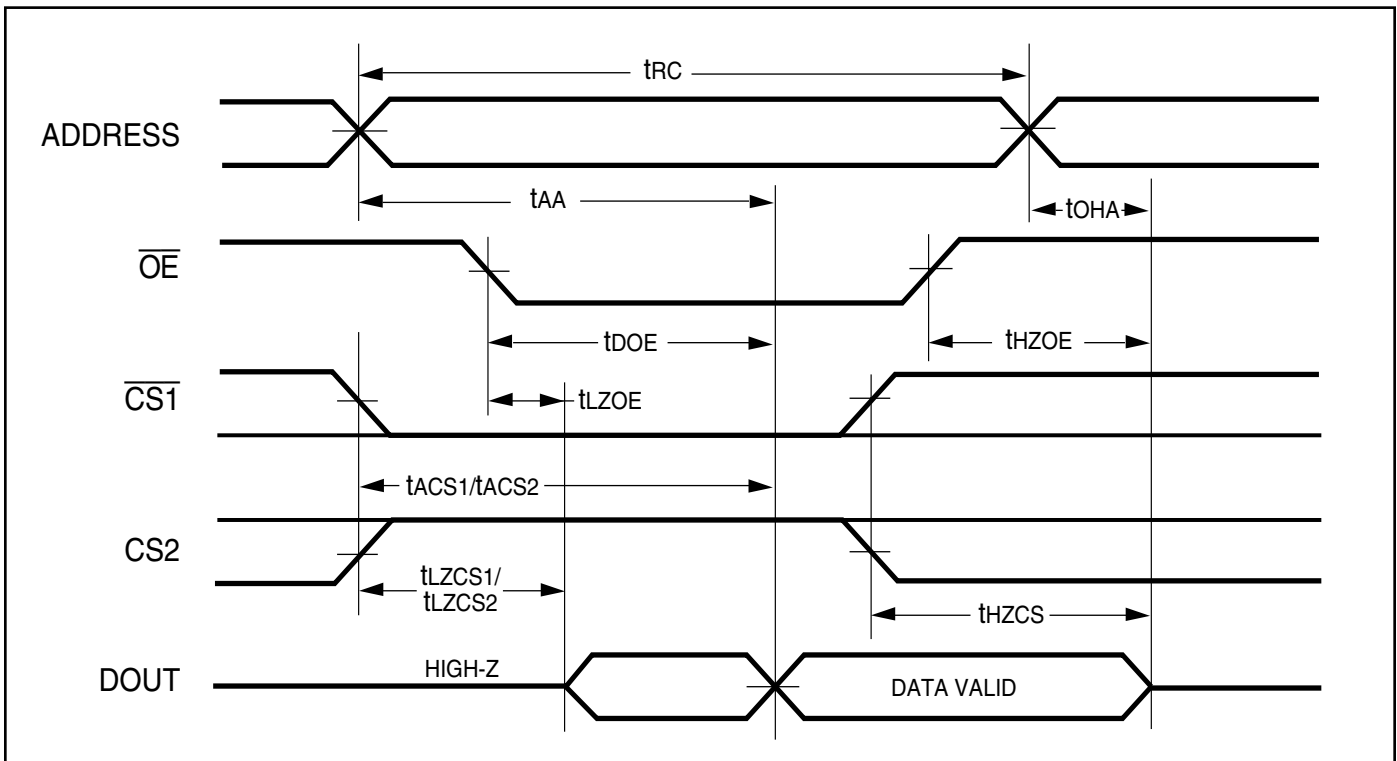
**AC WAVEFORMS**

**READ CYCLE NO. 1<sup>(1,2)</sup>** (Address Controlled) ( $\overline{CS1} = \overline{OE} = V_{IL}$ ,  $CS2 = \overline{WE} = V_{IH}$ )



**AC WAVEFORMS**

**READ CYCLE NO. 2<sup>(1,3)</sup>** ( $\overline{CS1}$ ,  $CS2$ ,  $\overline{OE}$  Controlled)



**Notes:**

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CS1} = V_{IL}$ .  $CS2 = \overline{WE} = V_{IH}$ .
3. Address is valid prior to or coincident with  $\overline{CS1}$  LOW and  $CS2$  HIGH transition.



**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup>** (Over Operating Range)

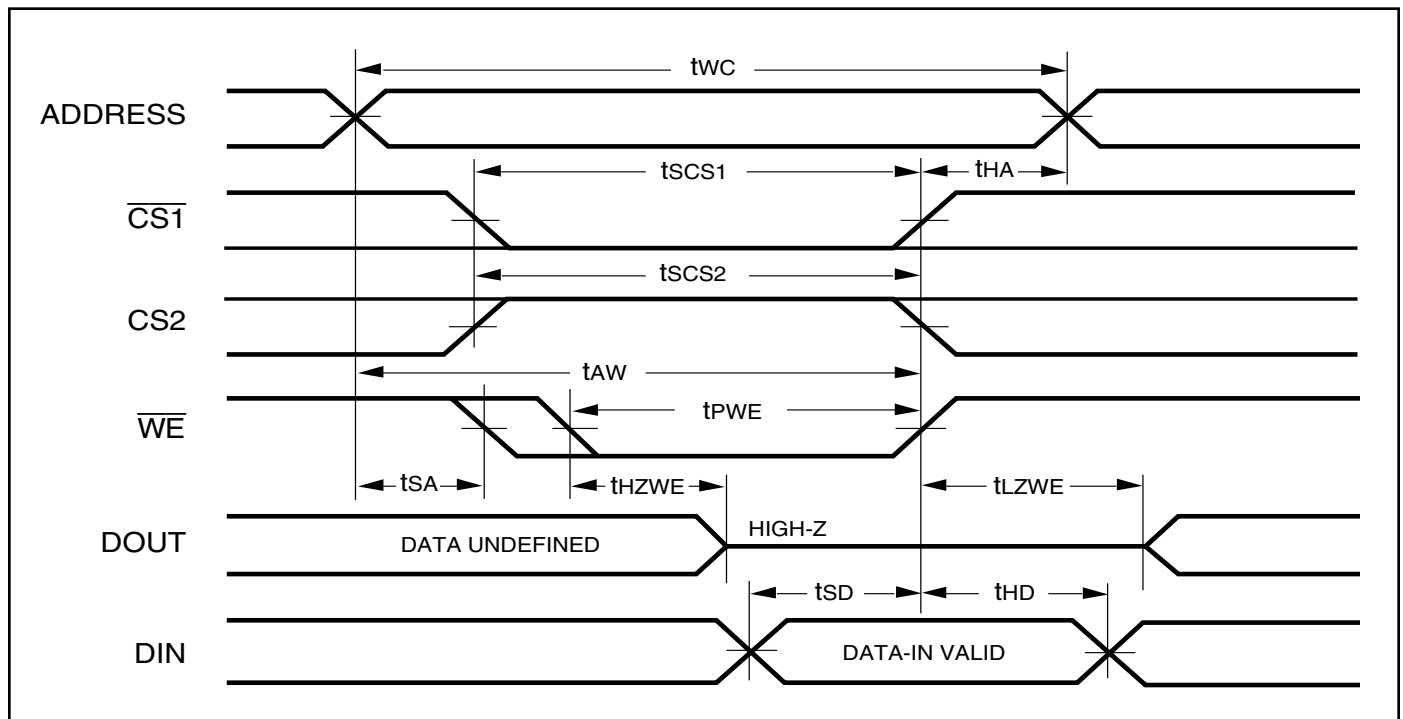
Symbol	Parameter	35ns		45ns		55 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	35	—	45	—	55	—	ns
t <sub>SCS1</sub> /t <sub>SCS2</sub>	$\overline{CS1}/\overline{CS2}$ to Write End	25	—	35	—	45	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	25	—	35	—	45	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	0	—	ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	25	—	35	—	40	—	ns
t <sub>SD</sub>	Data Setup to Write End	20	—	20	—	25	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	0	—	ns
t <sub>HZWE</sub> <sup>(3)</sup>	$\overline{WE}$ LOW to High-Z Output	—	10	—	20	—	20	ns
t <sub>LZWE</sub> <sup>(3)</sup>	$\overline{WE}$ HIGH to Low-Z Output	3	—	5	—	5	—	ns

**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4V to V<sub>DD</sub>-0.2V/V<sub>DD</sub>-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of  $\overline{CS1}$  LOW, CS2 HIGH and  $\overline{UB}$  or  $\overline{LB}$ , and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

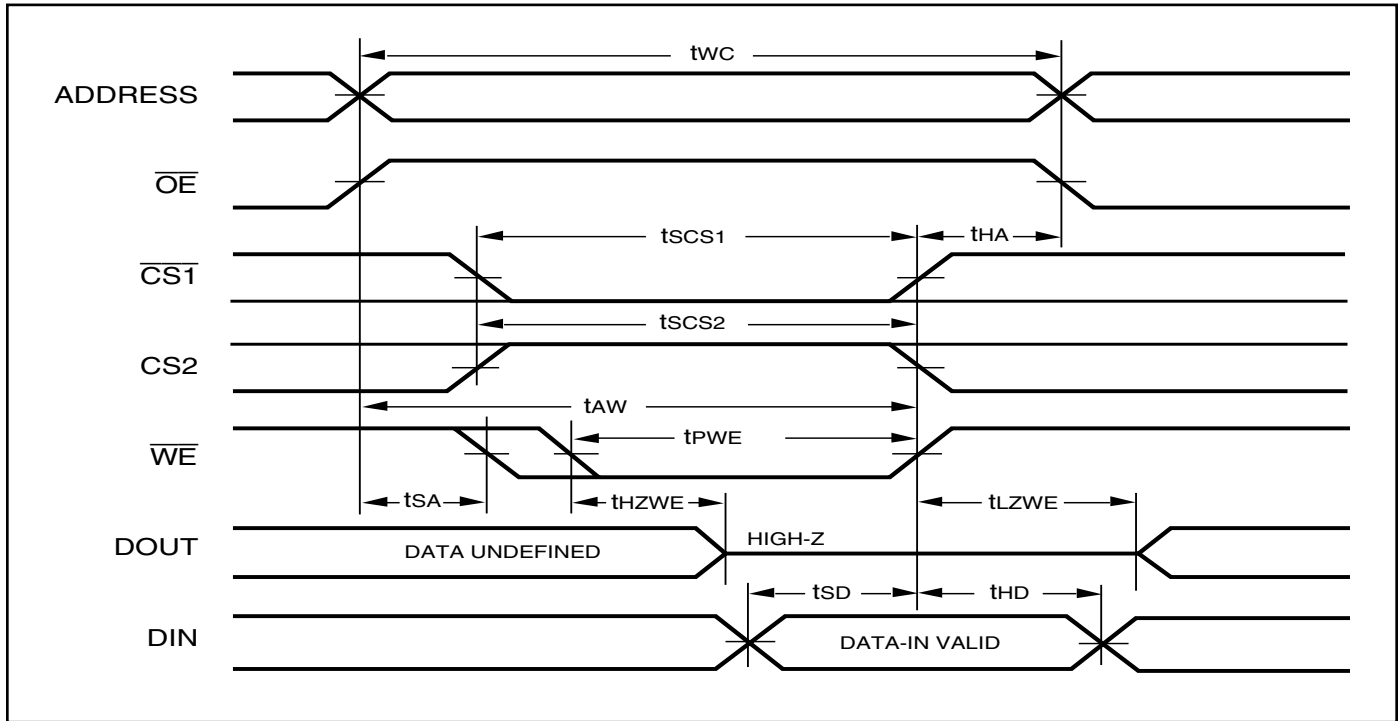
**AC WAVEFORMS**

**WRITE CYCLE NO. 1** ( $\overline{CS1}/\overline{CS2}$  Controlled,  $\overline{OE}$  = HIGH or LOW)

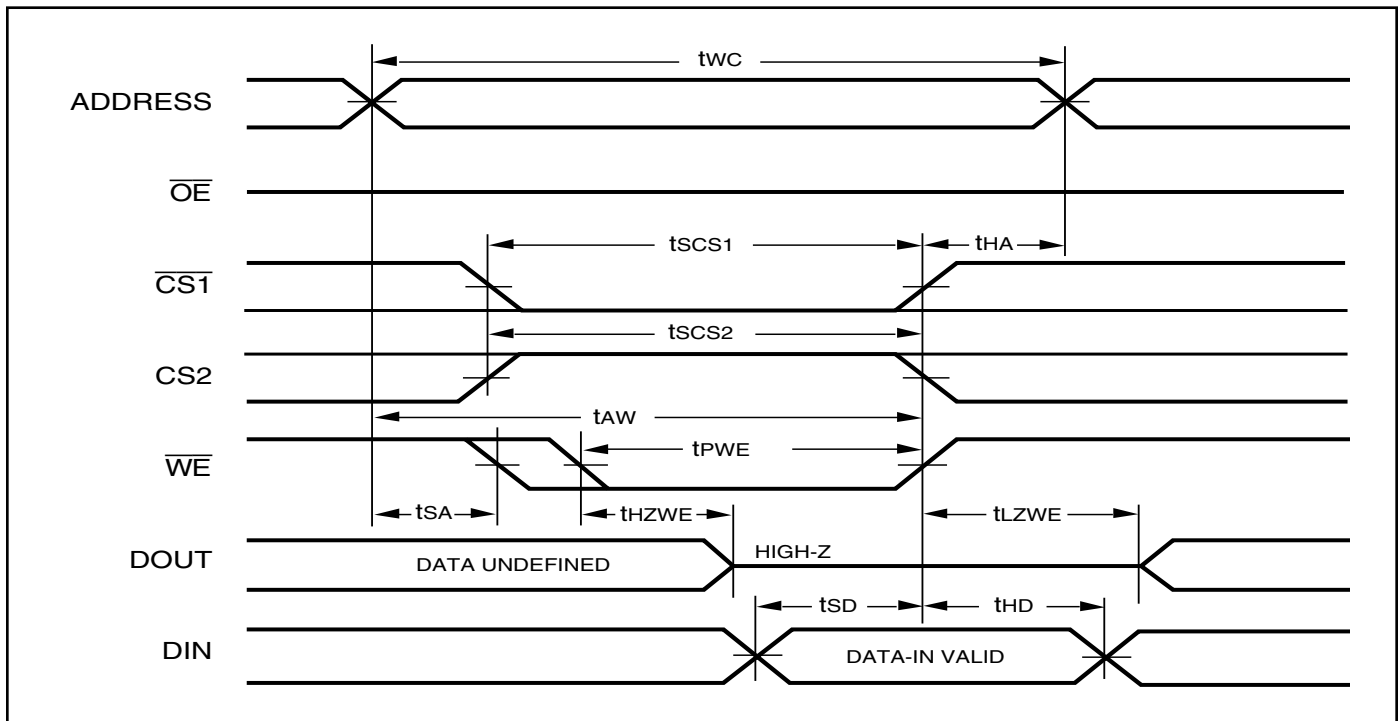


**AC WAVEFORMS**

**WRITE CYCLE NO. 2** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is HIGH During Write Cycle)



**WRITE CYCLE NO. 3** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is LOW During Write Cycle)

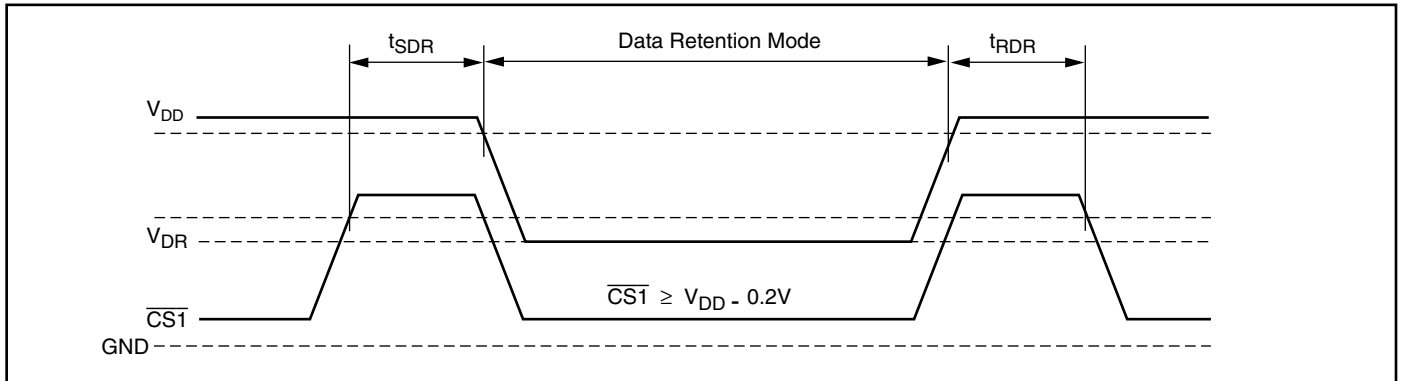


**DATA RETENTION SWITCHING CHARACTERISTICS**

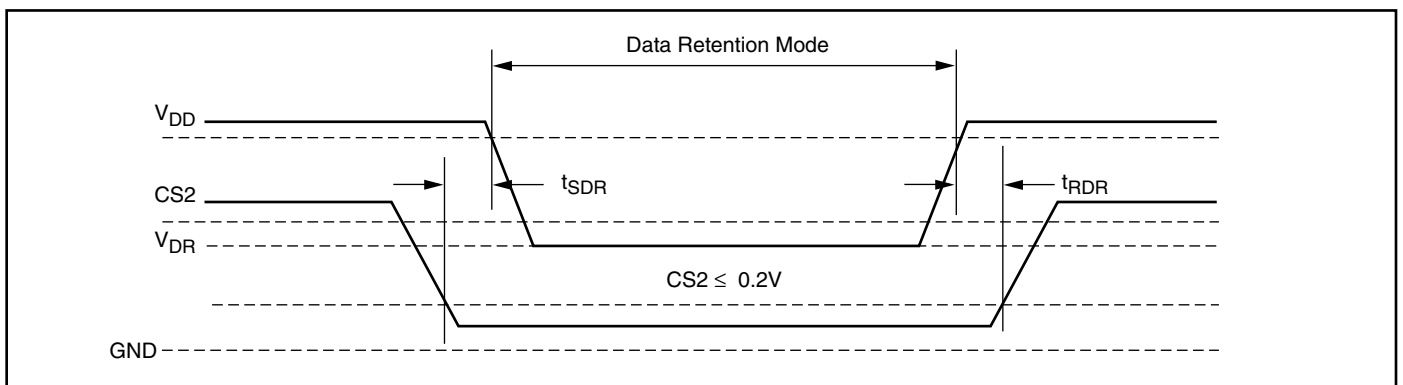
Symbol	Parameter	Test Condition		Min.	typ. <sup>(1)</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>DD</sub> for Data Retention	See Data Retention Waveform		1.2		3.6	V
I <sub>DR</sub>	Data Retention Current	V <sub>DD</sub> = 1.2V, CS1 ≥ V <sub>DD</sub> - 0.2V	Com. Ind. Auto.	—	0.5	2 4 18	μA
t <sub>SDR</sub>	Data Retention Setup Time	See Data Retention Waveform		0		—	ns
t <sub>RDR</sub>	Recovery Time	See Data Retention Waveform		t <sub>RC</sub>		—	ns

Note: 1. Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

**DATA RETENTION WAVEFORM (CS1 Controlled)**



**DATA RETENTION WAVEFORM (CS2 Controlled)**



## ORDERING INFORMATION

### IS62WV1288DALL (1.65V - 2.2V)

Industrial Range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Speed (ns)	Order Part No.	Package
55	IS62WV1288DALL-55TLI	TSOP-I, Lead-free (8mmx20mm)
	IS62WV1288DALL-55HLI	sTSOP-I, Lead-free (8mmx13.4mm)
	IS62WV1288DALL-55BI	mini BGA (6mm x 8mm)
	IS62WV1288DALL-55BLI	mini BGA (6mm x 8mm), Lead-free

## ORDERING INFORMATION

### IS62WV1288DBLL (2.3V - 3.6V)

Industrial Range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}^1$

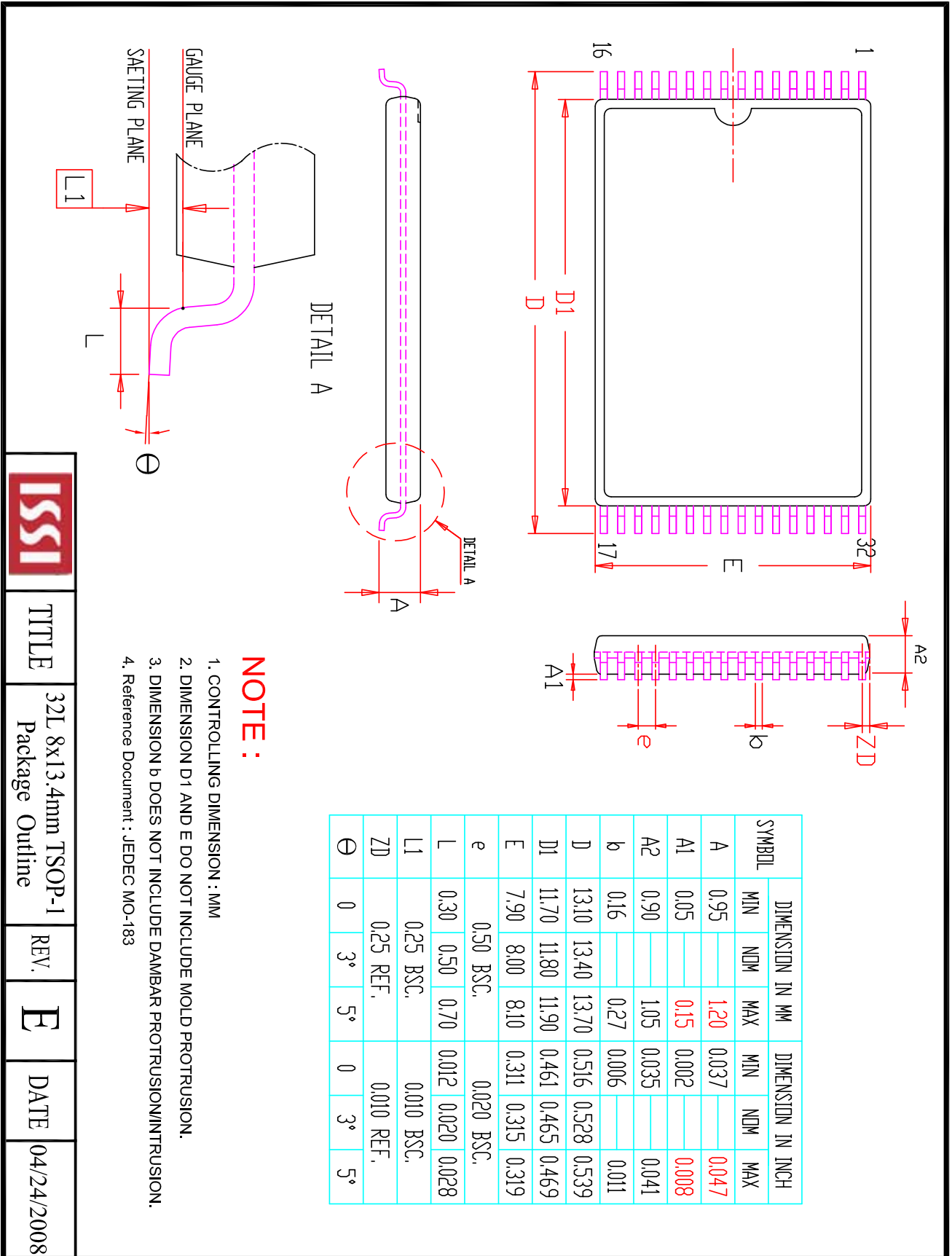
Speed (ns)	Order Part No.	Package
45	IS62WV1288DBLL-45TLI	TSOP-I, Lead-free (8mmx20mm)
	IS62WV1288DBLL-45HLI	sTSOP-I, Lead-free (8mmx13.4mm)
	IS62WV1288DBLL-45QLI	SOP, Lead-free
	IS62WV1288DBLL-45BI	mini BGA (6mm x 8mm)
	IS62WV1288DBLL-45BLI	mini BGA (6mm x 8mm), Lead-free

### Automotive Range: $-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$

Speed (ns)	Order Part No.	Package
45	IS65WV1288DBLL-45TLA3	TSOP-I, Lead-free (8mmx20mm)
	IS65WV1288DBLL-45HLA3	sTSOP-I, Lead-free (8mmx13.4mm)
	IS65WV1288DBLL-45QLA3	SOP, Lead-free

**Notes:**

1. Speed = 35ns for temperature range of  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  or for  $V_{DD} = 3.3\text{V} \pm 5\%$ .



TITLE

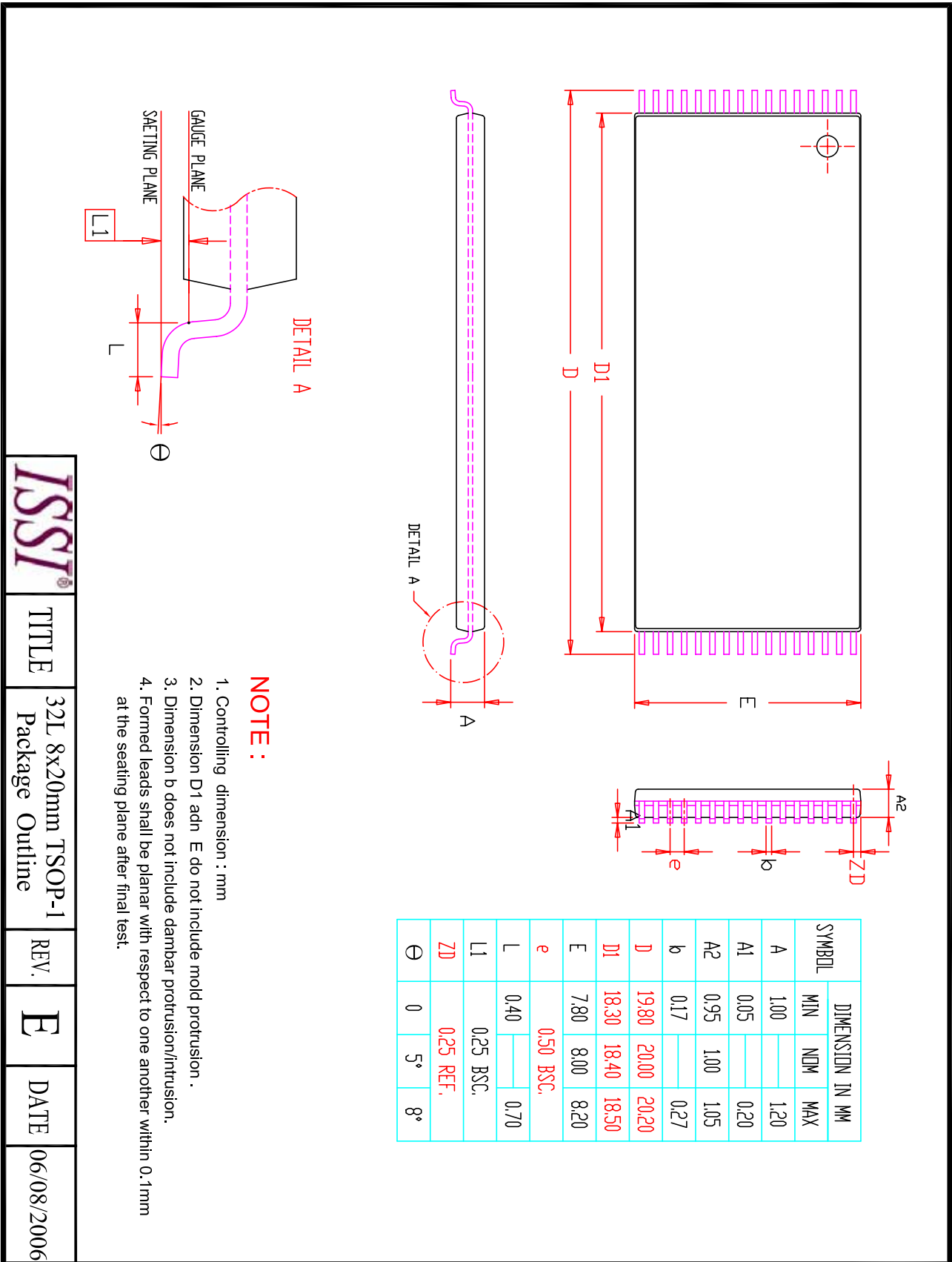
32L 8x13.4mm TSOP-1  
Package Outline

REV.

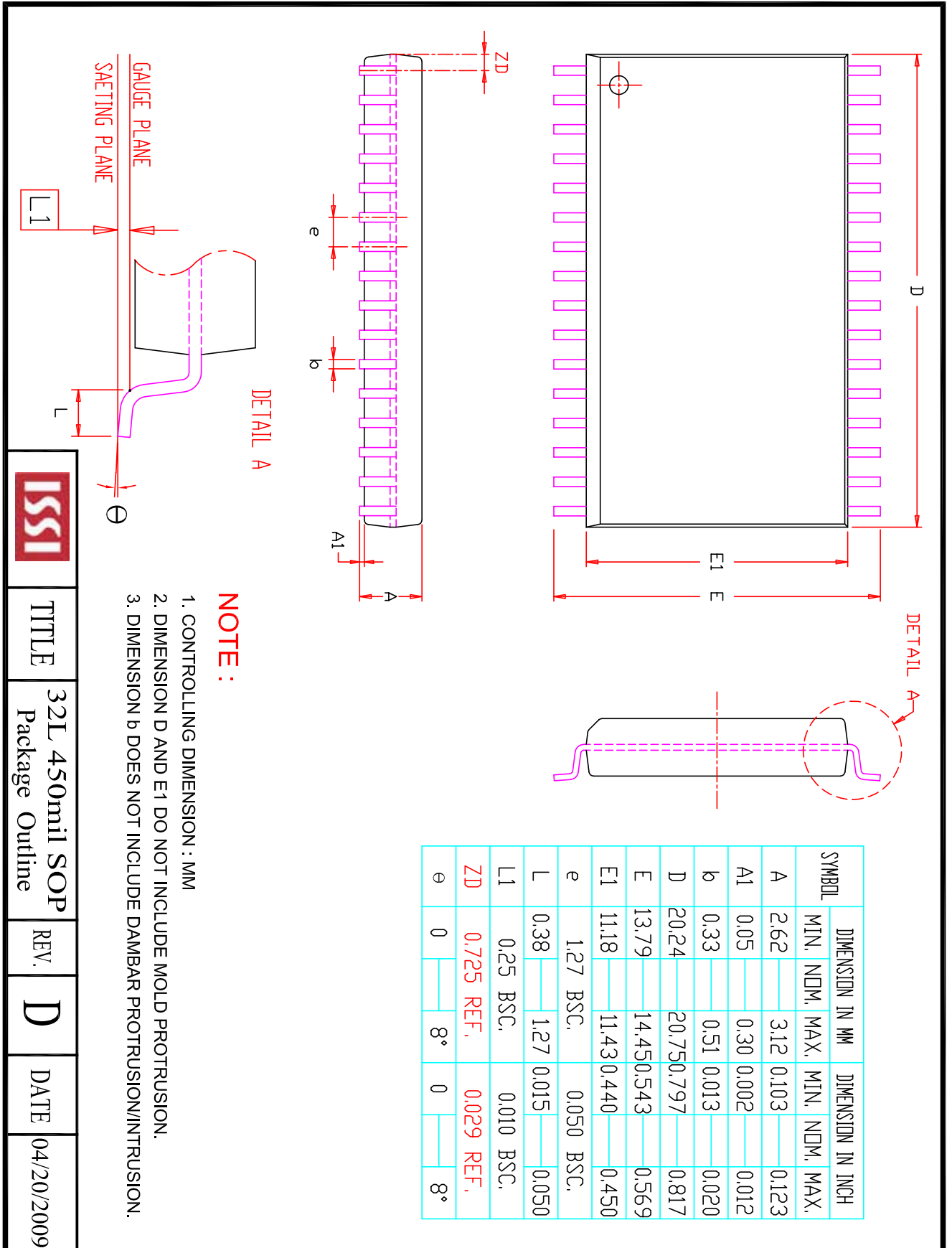
E

DATE

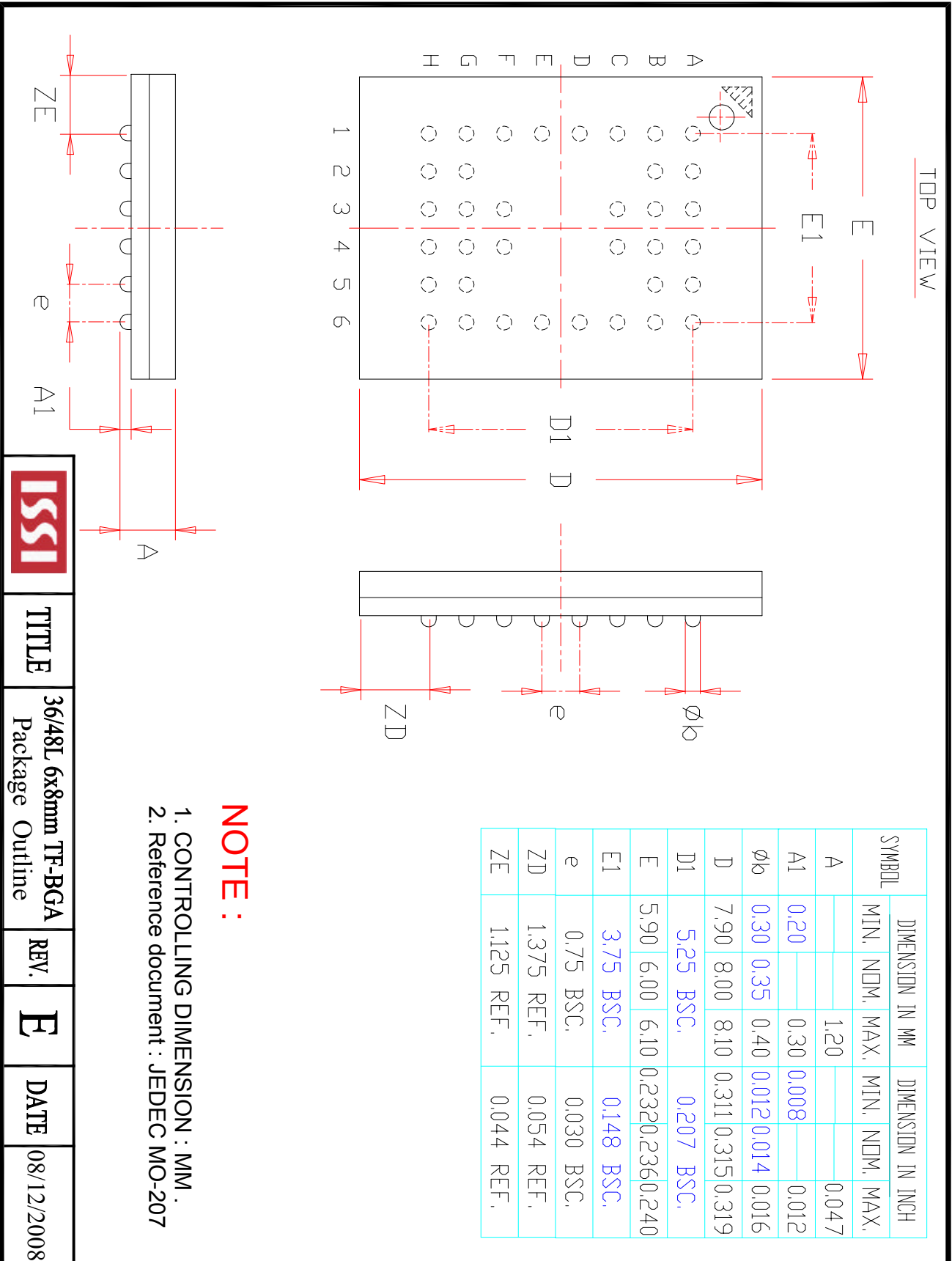
04/24/2008



<b>ISSI</b> ®	TITLE	32L 8x20mm TSOP-1 Package Outline	REV.	<b>E</b>	DATE	06/08/2006
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<b>ISSI</b>	TITLE	32L 450mil SOP Package Outline	REV.	D	DATE	04/20/2009
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<b>ISSI</b>	<b>TITLE</b>	36/48L 6x8mm TF-BGA Package Outline	<b>REV.</b>	<b>E</b>	<b>DATE</b>	08/12/2008
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