

## 2M x 8 HIGH-SPEED LOW POWER CMOS STATIC RAM

August 2016

### FEATURES

- High-speed access times:  
25, 35 ns
- High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single power supply
  - V<sub>DD</sub> 1.65V to 2.2V (IS62WV20488ALL)  
speed = 35ns for V<sub>cc</sub> = 1.65V to 2.2V
  - V<sub>DD</sub> 2.4V to 3.6V (IS62WV20488BLL)  
speed = 25ns for V<sub>cc</sub> = 2.4V to 3.6V
- Packages available:
  - 48-ball miniBGA (9mm x 11mm)
  - 44-pin TSOP (Type II)
- Industrial Temperature Support
- Lead-free available

### DESCRIPTION

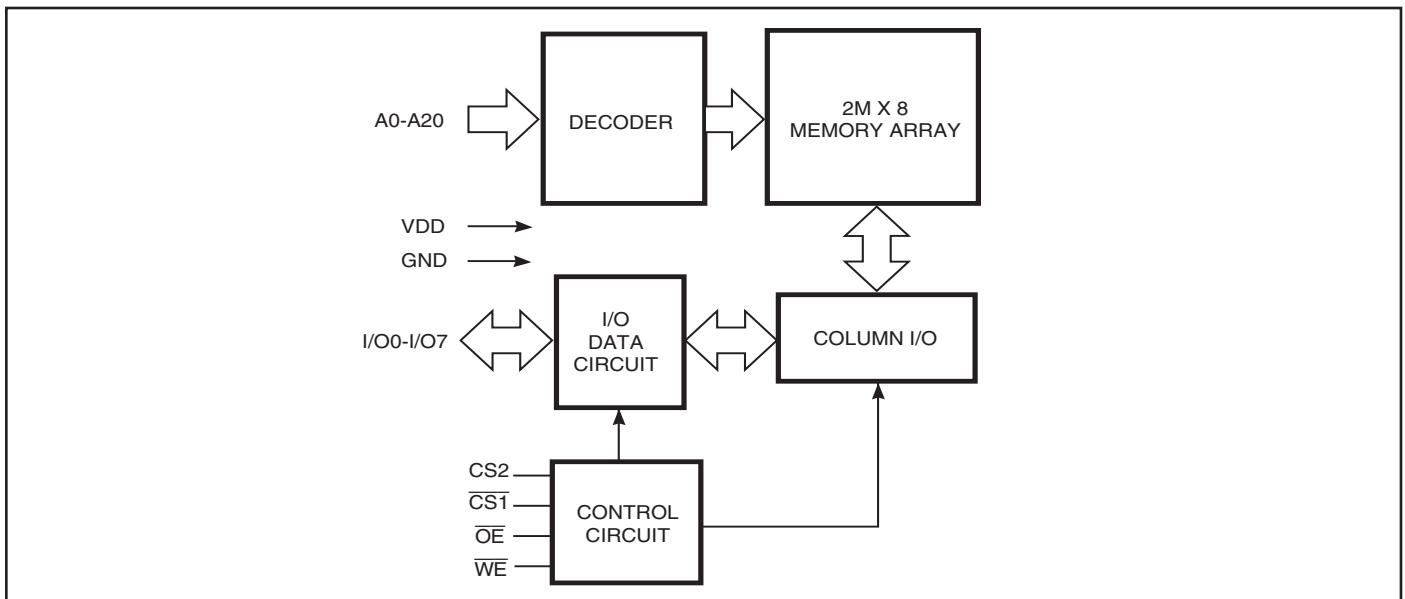
The *ISSI* IS62WV20488ALL/BLL is a high-speed, low power, 2M-word by 8-bit CMOS static RAM. The IS62WV20488ALL/BLL is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When  $\overline{CS1}$  is HIGH (deselected) or when CS2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

The IS62WV20488ALL/BLL operates from a single power supply and all inputs are TTL-compatible.

The IS62WV20488ALL/BLL is available in 48 ball mini BGA and 44-pin TSOP (Type II) packages.

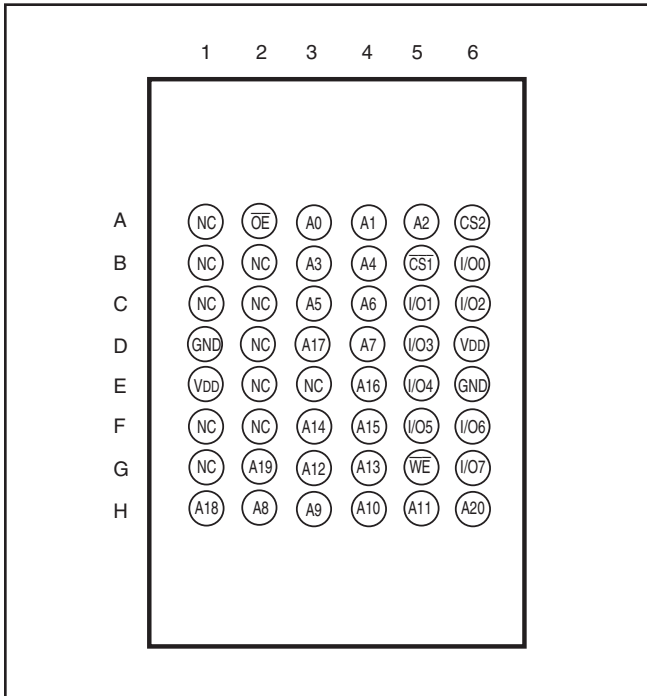
### FUNCTIONAL BLOCK DIAGRAM



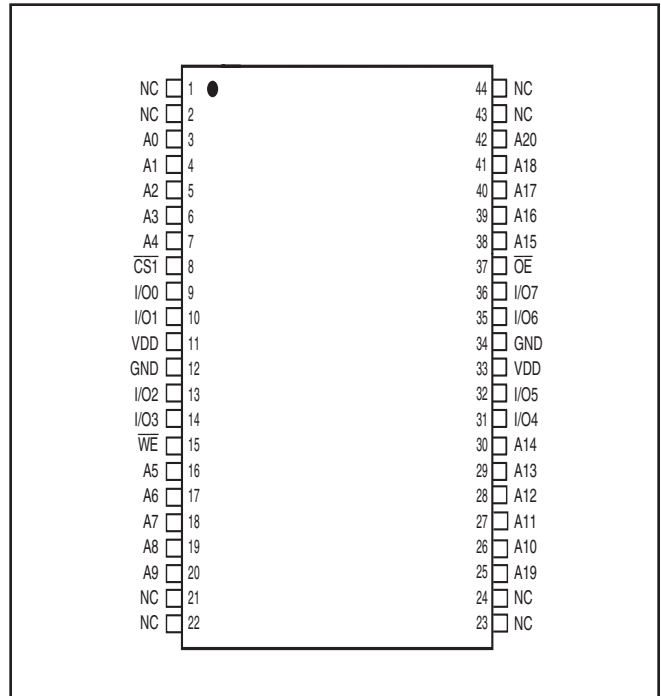
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**PIN CONFIGURATION**

**48-pin Mini BGA (M ) (9mm x 11mm)**



**44-pin TSOP (Type II )**



**PIN DESCRIPTIONS**

A0-A20	Address Inputs
CS1, CS2	Chip Enable Input
OE	Output Enable Input
WE	Write Enable Input
I/O0-I/O7	Data Input / Output
VDD	Power
GND	Ground
NC	No Connection

**TRUTH TABLE**

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	I/O Operation	V <sub>DD</sub> Current
Not Selected (Power-down)	X	H	X	X	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
Output Disabled	H	L	H	H	High-Z	I <sub>CC</sub>
Read	H	L	H	L	D <sub>OUT</sub>	I <sub>CC</sub>
Write	L	L	H	X	D <sub>IN</sub>	I <sub>CC</sub>

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to V <sub>DD</sub> + 0.5	V
V <sub>DD</sub>	V <sub>DD</sub> Relates to GND	-0.3 to 4.0	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W

**Notes:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**CAPACITANCE<sup>(1,2)</sup>**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>OUT</sub> = 0V	8	pF

**Notes:**

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>DD</sub> = 3.3V.

**OPERATING RANGE (V<sub>DD</sub>) (IS62WV20488ALL)**

Range	Ambient Temperature	V <sub>DD</sub> (35 ns)
Commercial	0°C to +70°C	1.65V-2.2V
Industrial	-40°C to +85°C	1.65V-2.2V

**OPERATING RANGE (V<sub>DD</sub>) (IS62WV20488BLL)<sup>(1)</sup>**

Range	Ambient Temperature	V <sub>DD</sub> (25 ns)
Commercial	0°C to +70°C	2.4V-3.6V
Industrial	-40°C to +85°C	2.4V-3.6V

**Note:**

1. When operated in the range of 2.4V-3.6V, the device meets 25ns. When operated in the range of 3.3V ± 5%, the device meets 15ns.

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

**$V_{DD} = 2.4V-3.6V$**

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$V_{DD} = \text{Min.}, I_{OH} = -1.0 \text{ mA}$	1.8	—	V
$V_{OL}$	Output LOW Voltage	$V_{DD} = \text{Min.}, I_{OL} = 1.0 \text{ mA}$	—	0.4	V
$V_{IH}$	Input HIGH Voltage		2.0	$V_{DD} + 0.3$	V
$V_{IL}$	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V
$I_{LI}$	Input Leakage	$GND \leq V_{IN} \leq V_{DD}$	-1	1	$\mu\text{A}$
$I_{LO}$	Output Leakage	$GND \leq V_{OUT} \leq V_{DD}$ , Outputs Disabled	-1	1	$\mu\text{A}$

**Note:**

- $V_{IL}$  (min.) = -0.3V DC;  $V_{IL}$  (min.) = -2.0V AC (pulse width 2.0 ns). Not 100% tested.  
 $V_{IH}$  (max.) =  $V_{DD} + 0.3V$  DC;  $V_{IH}$  (max.) =  $V_{DD} + 2.0V$  AC (pulse width 2.0 ns). Not 100% tested.

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

**$V_{DD} = 1.65V-2.2V$**

Symbol	Parameter	Test Conditions	$V_{DD}$	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -0.1 \text{ mA}$	1.65-2.2V	1.4	—	V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 0.1 \text{ mA}$	1.65-2.2V	—	0.2	V
$V_{IH}$	Input HIGH Voltage		1.65-2.2V	1.4	$V_{DD} + 0.2$	V
$V_{IL}^{(1)}$	Input LOW Voltage		1.65-2.2V	-0.2	0.4	V
$I_{LI}$	Input Leakage	$GND \leq V_{IN} \leq V_{DD}$		-1	1	$\mu\text{A}$
$I_{LO}$	Output Leakage	$GND \leq V_{OUT} \leq V_{DD}$ , Outputs Disabled		-1	1	$\mu\text{A}$

**Note:**

- $V_{IL}$  (min.) = -0.3V DC;  $V_{IL}$  (min.) = -2.0V AC (pulse width 2.0 ns). Not 100% tested.  
 $V_{IH}$  (max.) =  $V_{DD} + 0.3V$  DC;  $V_{IH}$  (max.) =  $V_{DD} + 2.0V$  AC (pulse width 2.0 ns). Not 100% tested.

**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Symbol	Parameter	Test Conditions		-25		-35		Unit
				Min.	Max.	Min.	Max.	
I <sub>CC</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com.	—	25	—	20	mA
			Ind. typ. <sup>(2)</sup>	—	30 20	—	25 17	
I <sub>CC1</sub>	Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = 0	Com.	—	10	—	10	mA
			Ind.	—	15	—	15	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> CS1 ≥ V <sub>IH</sub> , f = 0, CS2 = V <sub>IL</sub>	Com.	—	5	—	5	mA
			Ind.	—	6	—	6	
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max., CS1 ≥ V <sub>DD</sub> - 0.2V, CS2 ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Com.	—	1.5	—	1.5	mA
			Ind. typ. <sup>(2)</sup>	—	1.5 0.8	—	1.5 0.5	

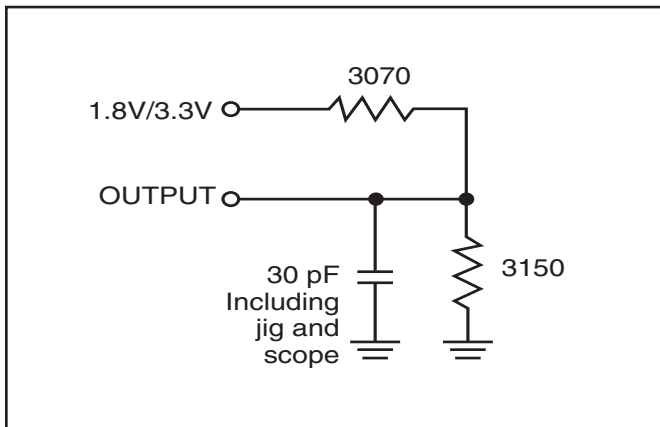
**Note:**

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

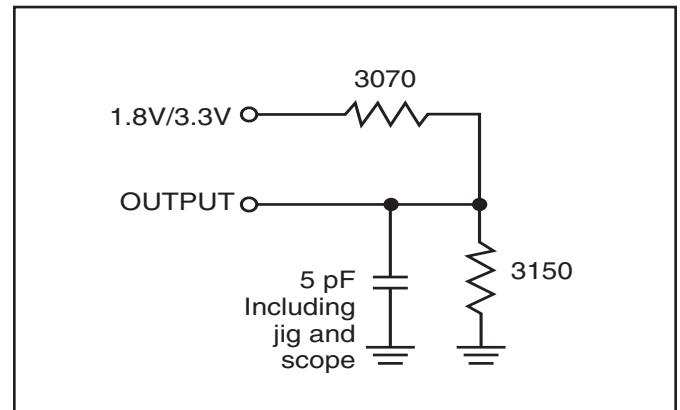
**AC TEST CONDITIONS (LOW POWER)**

Parameter	Unit (2.4V-3.6V)	Unit (1.65V-2.2V)
Input Pulse Level	0.4V to $V_{DD}-0.3V$	0.4V to $V_{DD}-0.2V$
Input Rise and Fall Times	1.5ns	1.5ns
Input and Output Timing and Reference Level ( $V_{Ref}$ )	$V_{DD}/2$	$V_{DD}/2$
Output Load	See Figures 1 and 2	See Figures 1 and 2

**AC TEST LOADS**



**Figure 1**



**Figure 2**

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

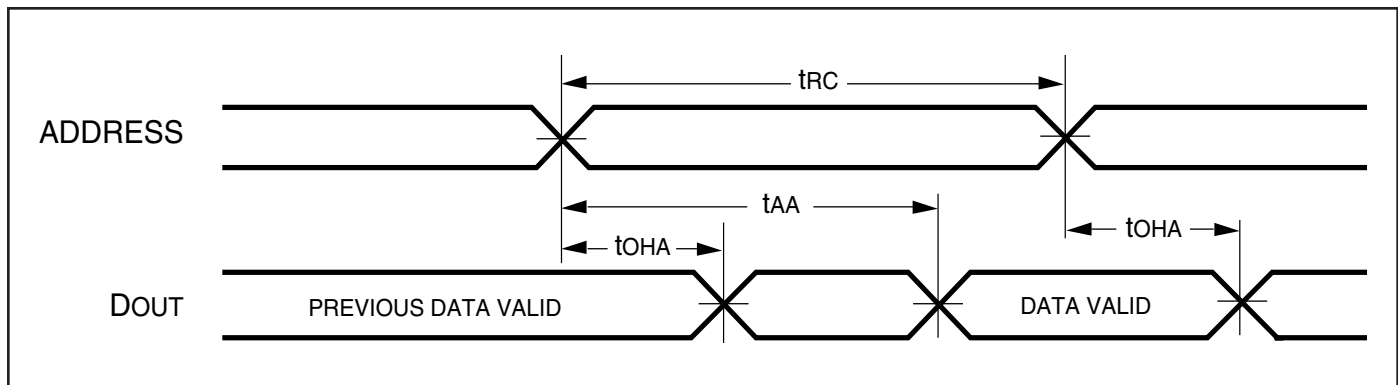
Symbol	Parameter	25ns		35ns		Unit
		Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	25	—	35	—	ns
t <sub>AA</sub>	Address Access Time	—	25	—	35	ns
t <sub>OHA</sub>	Output Hold Time	4	—	4	—	ns
t <sub>ACS1</sub> /t <sub>ACS2</sub>	CS1/CS2 Access Time	—	25	—	35	ns
t <sub>DOE</sub>	OE Access Time	—	12	—	15	ns
t <sub>HZOE<sup>(2)</sup></sub>	OE to High-Z Output	—	8	—	10	ns
t <sub>LZOE<sup>(2)</sup></sub>	OE to Low-Z Output	5	—	5	—	ns
t <sub>HZCS1</sub> /t <sub>HZCS2<sup>(2)</sup></sub>	CS1/CS2 to High-Z Output	0	8	0	10	ns
t <sub>LZCS1</sub> /t <sub>LZCS2<sup>(2)</sup></sub>	CS1/CS2 to Low-Z Output	10	—	10	—	ns

**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V<sub>DD</sub>-0.2V/0.4V to V<sub>DD</sub>-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

**AC WAVEFORMS**

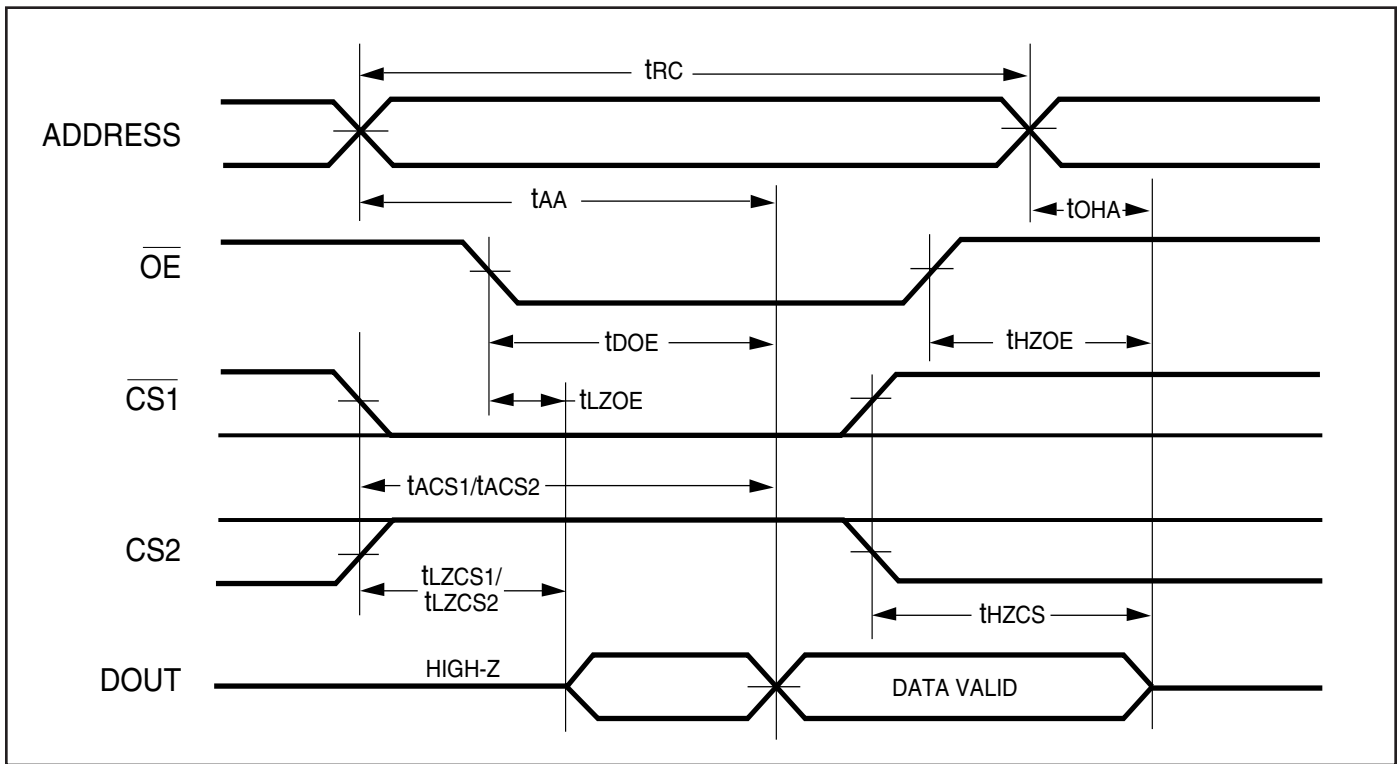
**READ CYCLE NO. 1<sup>(1,2)</sup>** (Address Controlled) ( $\overline{CS1} = \overline{OE} = V_{IL}$ ,  $CS2 = \overline{WE} = V_{IH}$ )





**AC WAVEFORMS**

**READ CYCLE NO. 2<sup>(1,3)</sup> ( $\overline{CS1}$ ,  $CS2$ ,  $\overline{OE}$  Controlled)**



**Notes:**

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CS1} = V_{IL}$ .  $CS2 = \overline{WE} = V_{IH}$ .
3. Address is valid prior to or coincident with  $\overline{CS1}$  LOW and  $CS2$  HIGH transition.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup>** (Over Operating Range)

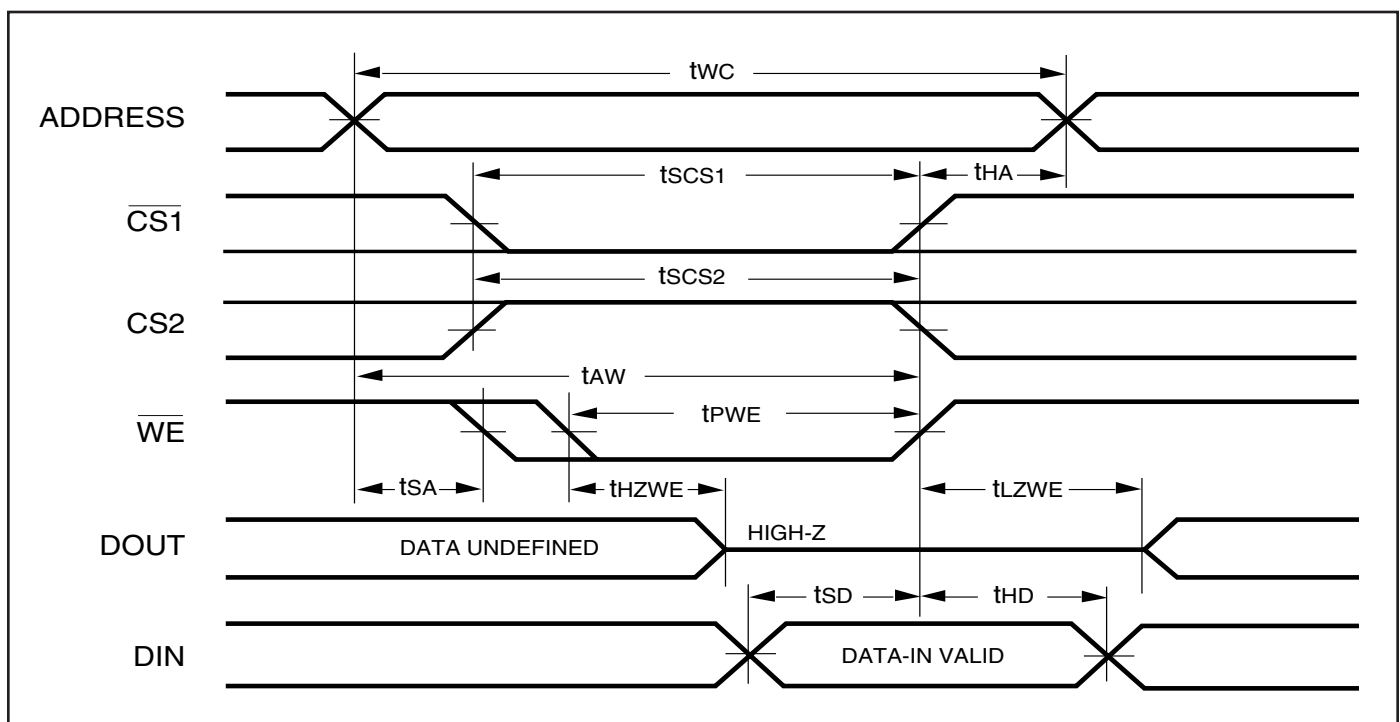
Symbol	Parameter	25 ns		35 ns		Unit
		Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	25	—	35	—	ns
t <sub>SCS1</sub> /t <sub>SCS2</sub>	CS1/CS2 to Write End	18	—	25	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	15	—	25	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	ns
t <sub>PWE</sub> <sup>(4)</sup>	WE Pulse Width	18	—	30	—	ns
t <sub>SD</sub>	Data Setup to Write End	12	—	15	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	ns
t <sub>HZWE</sub> <sup>(3)</sup>	WE LOW to High-Z Output	—	12	—	20	ns
t <sub>LZWE</sub> <sup>(3)</sup>	WE HIGH to Low-Z Output	5	—	5	—	ns

**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V<sub>DD</sub>-0.2V/0.4V to V<sub>DD</sub>-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of CS1 LOW, CS2 HIGH and  $\overline{UB}$  or  $\overline{LB}$ , and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
4. t<sub>PWE</sub> > t<sub>HZWE</sub> + t<sub>SD</sub> when  $\overline{OE}$  is LOW.

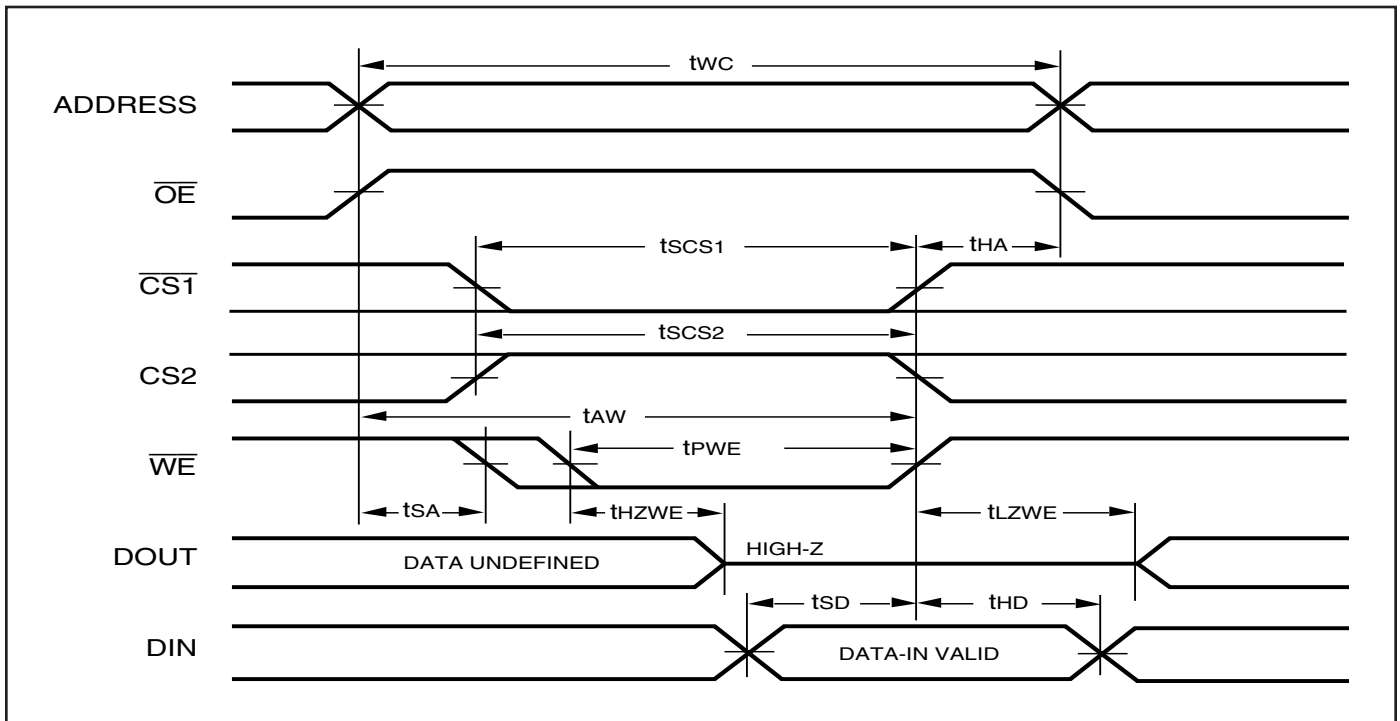
**AC WAVEFORMS**

**WRITE CYCLE NO. 1** ( $\overline{CS1}$ /CS2 Controlled,  $\overline{OE}$  = HIGH or LOW)

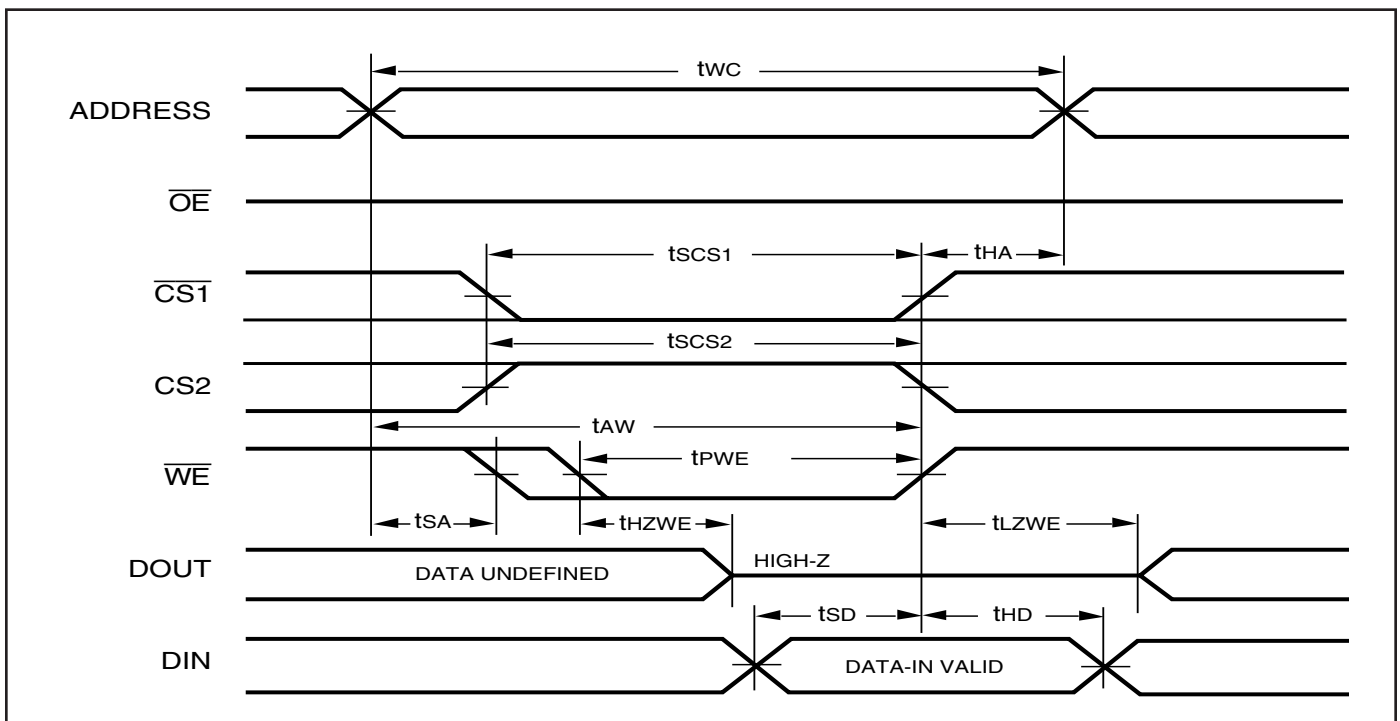


**AC WAVEFORMS**

**WRITE CYCLE NO. 2** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is HIGH During Write Cycle)



**WRITE CYCLE NO. 3** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is LOW During Write Cycle)



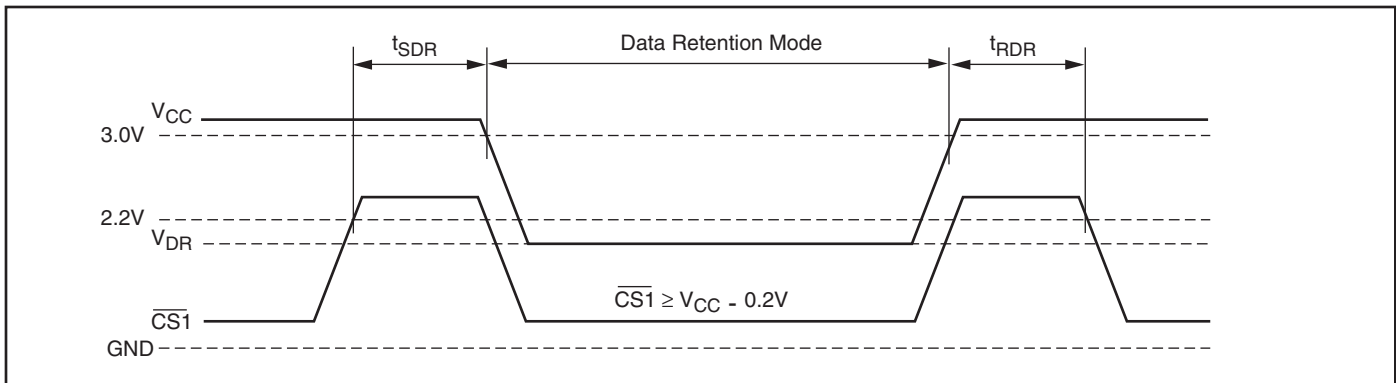
## DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	See Data Retention Waveform	1.2		3.6	V
I <sub>DR</sub>	Data Retention Current	V <sub>CC</sub> = 1.2V, CS1/CS2 ≥ V <sub>CC</sub> - 0.2V	—	0.5	1.5	mA
t <sub>SDR</sub>	Data Retention Setup Time	See Data Retention Waveform	0		—	ns
t <sub>RDR</sub>	Recovery Time	See Data Retention Waveform	t <sub>rc</sub>		—	ns

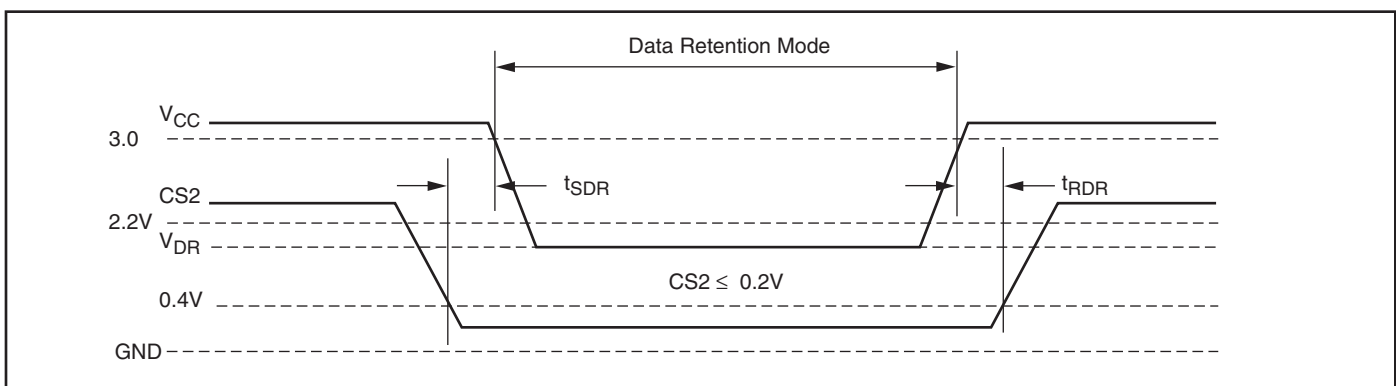
Note:

1. Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

### DATA RETENTION WAVEFORM ( $\overline{CS1}$ Controlled)



### DATA RETENTION WAVEFORM (CS2 Controlled)



**ORDERING INFORMATION**

**Industrial Range: -40°C to +85°C**

**Voltage Range: 2.4V to 3.6V**

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<b>Speed (ns)</b>	<b>Order Part No.</b>	<b>Package</b>
25	IS62WV20488BLL-25MI	48 mini BGA (9mm x 11mm)
	IS62WV20488BLL-25MLI	48 mini BGA (9mm x 11mm), Lead-free
	IS62WV20488BLL-25TI	TSOP (Type II)
	IS62WV20488BLL-25TLI	TSOP (Type II), Lead-free

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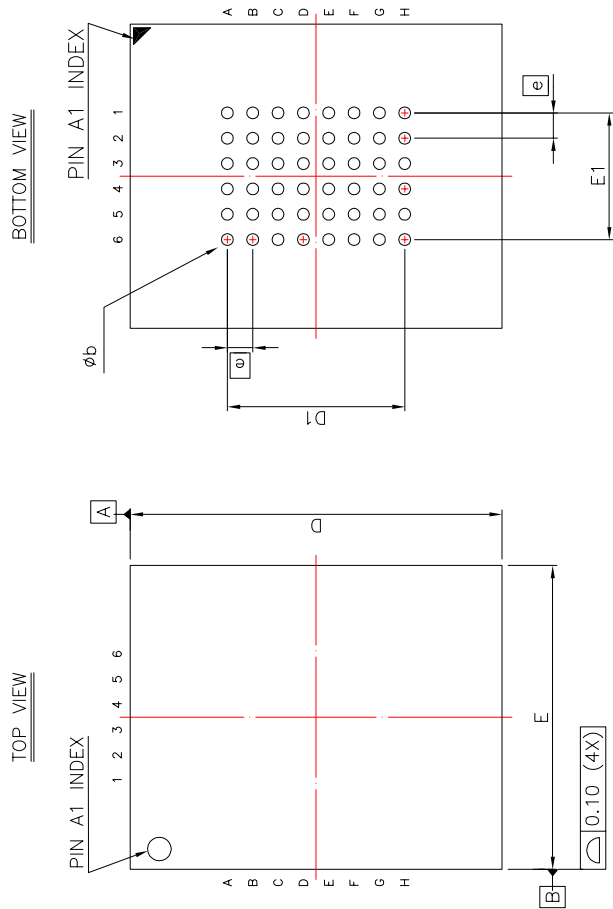
**Industrial Range: -40°C to +85°C**

**Voltage Range: 1.65V to 2.2V**

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<b>Speed (ns)</b>	<b>Order Part No.</b>	<b>Package</b>
35	IS62WV20488ALL-35MI	48 mini BGA (9mm x 11mm)
	IS62WV20488ALL-35MLI	48 mini BGA (9mm x 11mm), Lead-free
	IS62WV20488ALL-35TI	TSOP (Type II)
	IS62WV20488ALL-35TLI	TSOP (Type II), Lead-free

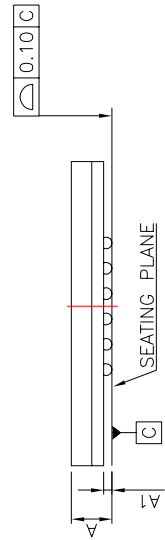
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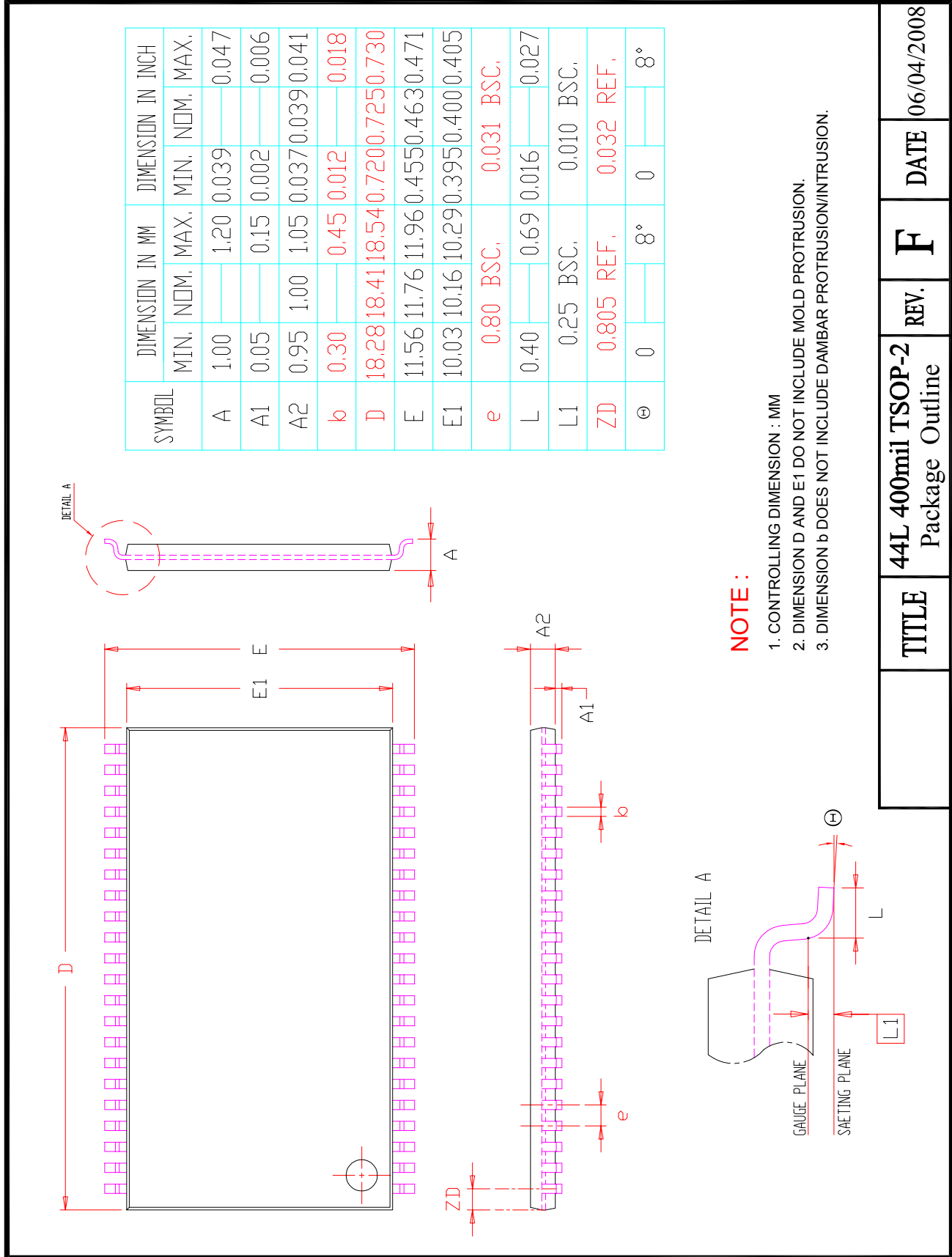
SYM.	DIMENSION (mm)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.20	—	0.30	0.008	—	0.012
b	0.30	0.35	0.40	0.012	0.014	0.016
D	10.90	11.00	11.10	0.429	0.433	0.437
D1	5.25 BSC			0.207 BSC		
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	3.75 BSC			0.148 BSC		
Ⓜ	0.75 BSC			0.030 BSC		

**NOTE :**

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207



	TITLE	48L 9x11mm TF-BGA Package Outline	REV.	B	DATE	08/21/2008
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<b>TITLE</b>	<b>REV.</b>	<b>DATE</b>
44L 400mil TSOP-2 Package Outline	<b>F</b>	06/04/2008

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