

## 512K x 8 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

NOVEMBER 2016

### FEATURES

- High-speed access time: 55ns, 70ns
- CMOS low power operation
  - 36 mW (typical) operating
  - 9  $\mu$ W (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
  - 1.65V – 2.2V  $V_{DD}$  (IS62WV5128ALL)
  - 2.5V – 3.6V  $V_{DD}$  (IS62WV5128BLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial temperature available
- Lead-free available

### DESCRIPTION

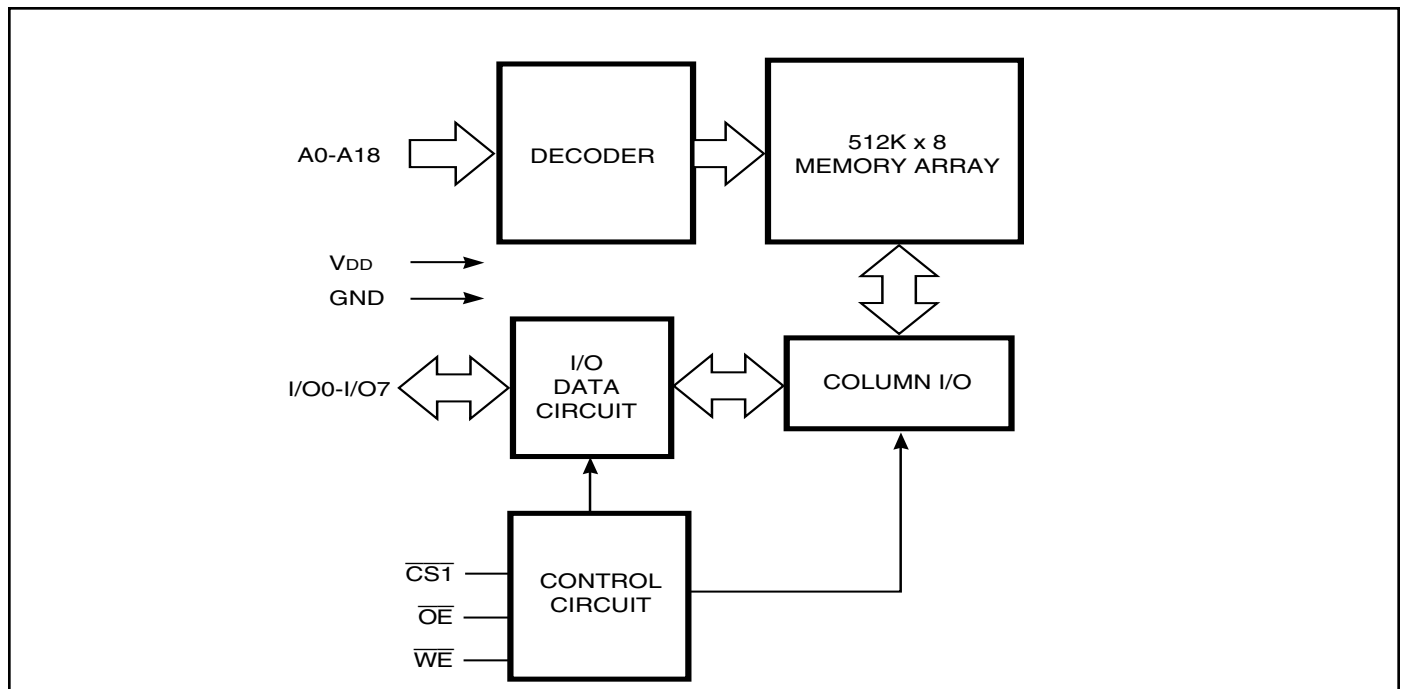
The ISSI IS62WV5128ALL / IS62WV5128BLL are high-speed, 4M bit static RAMs organized as 512K words by 8 bits. It is fabricated using ISSI's high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When CS1 is HIGH (deselected) the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (WE) controls both writing and reading of the memory.

The IS62WV5128ALL and IS62WV5128BLL are packaged in the JEDEC standard 32-pin TSOP (TYPE I), 32-pin sTSOP (TYPE I), 32-pin TSOP (Type II), 32-pin SOP and 36-pin mini BGA.

### FUNCTIONAL BLOCK DIAGRAM



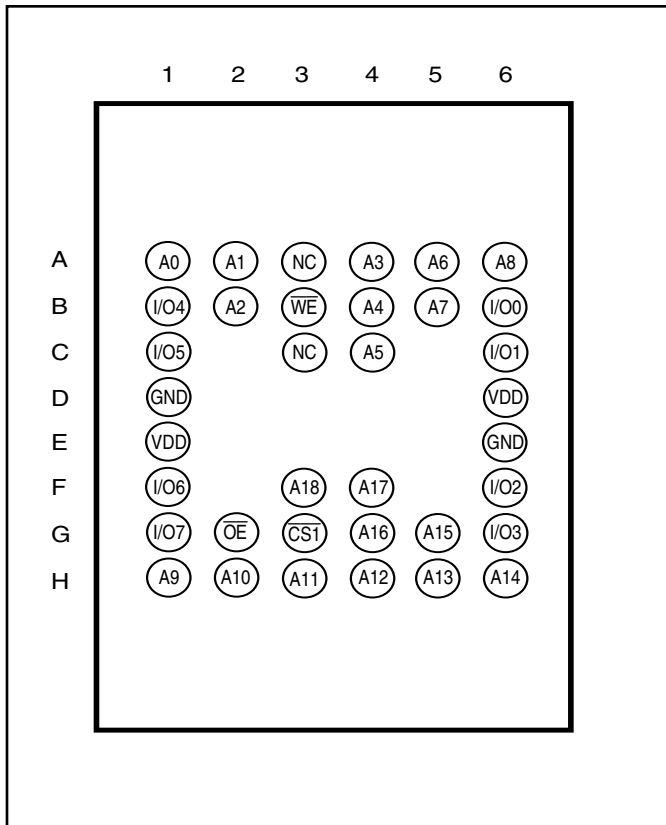
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**IS62WV5128ALL, IS62WV5128BLL**

**PIN DESCRIPTIONS**

A0-A18	Address Inputs
CS1	Chip Enable 1 Input
OE	Output Enable Input
WE	Write Enable Input
I/O0-I/O7	Input/Output
NC	No Connection
V <sub>DD</sub>	Power
GND	Ground

**36-pin mini BGA (B) (6mm x 8mm)  
(Package Code B)**



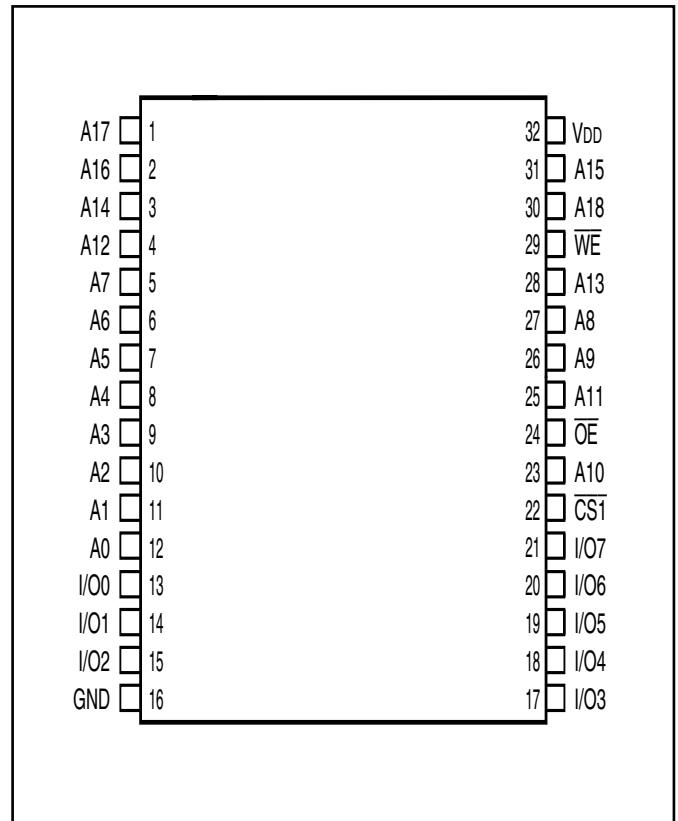
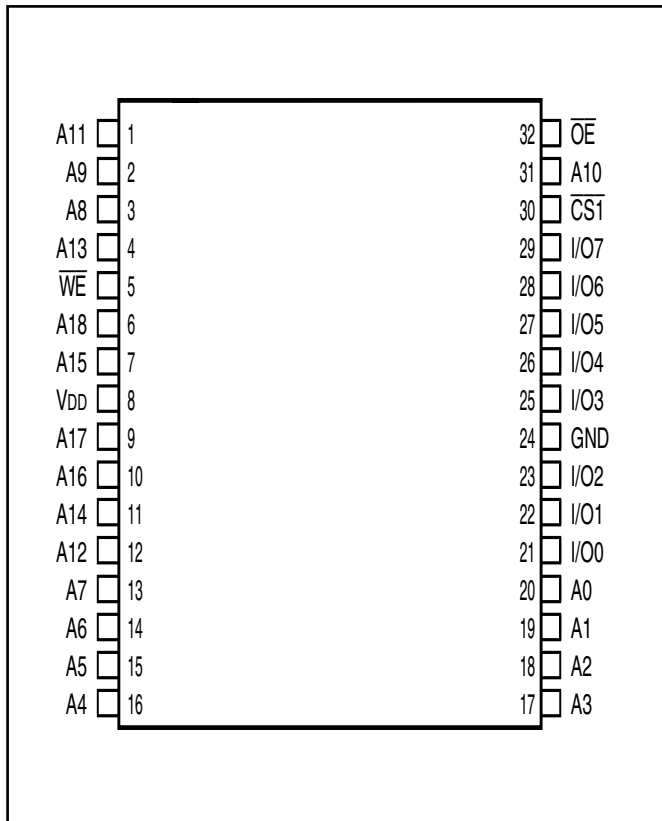
**PIN DESCRIPTIONS**

A0-A18	Address Inputs
CS1	Chip Enable 1 Input
OE	Output Enable Input
WE	Write Enable Input
I/O0-I/O7	Input/Output
VDD	Power
GND	Ground

**PIN CONFIGURATION**

32-pin TSOP (TYPE I), (Package Code T)  
32-pin sTSOP (TYPE I) (Package Code H)

32-pin SOP (Package Code Q)  
32-pin TSOP (TYPE II) (Package Code T2)





## IS62WV5128ALL, IS62WV5128BLL

### OPERATING RANGE (V<sub>DD</sub>)

Range	Ambient Temperature	IS62WV5128ALL	IS62WV5128BLL
Commercial	0°C to +70°C	1.65V - 2.2V	2.5V - 3.6V
Industrial	-40°C to +85°C	1.65V - 2.2V	2.5V - 3.6V

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.2 to V <sub>DD</sub> +0.3	V
V <sub>DD</sub>	V <sub>DD</sub> Related to GND	-0.2 to V <sub>DD</sub> +0.3	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	V <sub>DD</sub>	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	1.65-2.2V	1.4	—	V
		I <sub>OH</sub> = -1 mA	2.5-3.6V	2.2	—	V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA	1.65-2.2V	—	0.2	V
		I <sub>OL</sub> = 2.1 mA	2.5-3.6V	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		1.65-2.2V	1.4	V <sub>DD</sub> + 0.2	V
			2.5-3.6V	2.2	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub> <sup>(1)</sup>	Input LOW Voltage		1.65-2.2V	-0.2	0.4	V
			2.5-3.6V	-0.2	0.6	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>		-1	1	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled		-1	1	μA

Notes:

1. V<sub>IL</sub> (min.) = -1.0V for pulse width less than 10 ns.

**CAPACITANCE<sup>(1)</sup>**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	8	pF
C <sub>OUT</sub>	Input/Output Capacitance	V <sub>OUT</sub> = 0V	10	pF

Note:

1. Tested initially and after any design or process changes that may affect these parameters.

**AC TEST CONDITIONS**

Parameter	IS62WV5128ALL (Unit)	IS62WV5128BLL (Unit)
Input Pulse Level	0.4V to V <sub>DD</sub> -0.2V	0.4V to V <sub>DD</sub> -0.3V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V <sub>REF</sub>	V <sub>REF</sub>
Output Load	See Figures 1 and 2	See Figures 1 and 2

	IS62WV5128ALL 1.65 - 2.2V	IS62WV5128BLL 2.5V - 3.6V
R1(Ω)	3070	3070
R2(Ω)	3150	3150
V <sub>REF</sub>	0.9V	1.5V
V <sub>TM</sub>	1.8V	2.8V

**AC TEST LOADS**

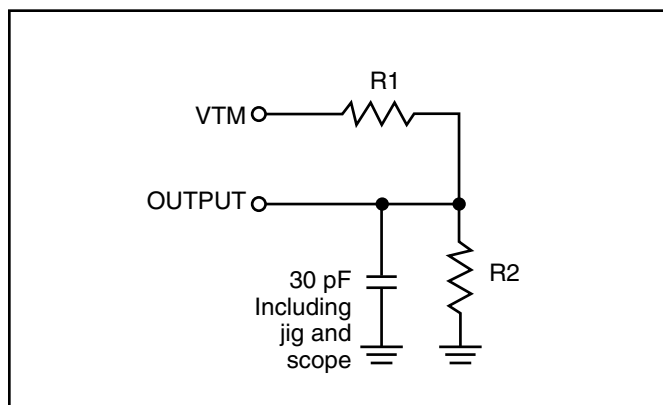


Figure 1

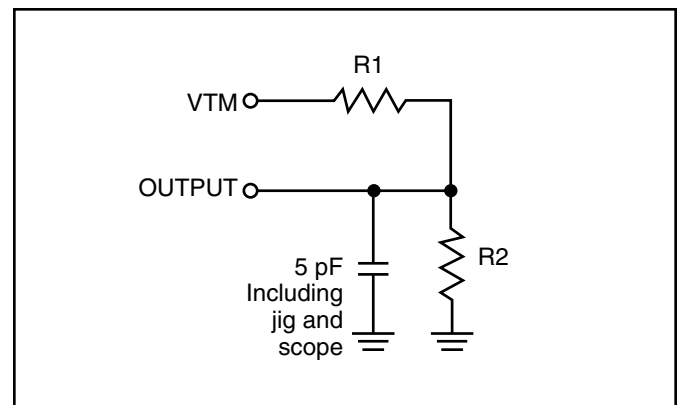


Figure 2



## IS62WV5128ALL, IS62WV5128BLL

### POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

#### 62WV5128ALL (1.65V - 2.2V)

Symbol	Parameter	Test Conditions	Max.	Unit	
			70 ns		
I <sub>CC</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com. Ind.	25 30	mA
I <sub>CC1</sub>	Operating Supply Current	V <sub>DD</sub> = Max., CS1 = 0.2V WE = V <sub>DD</sub> -0.2V f=1MHZ	Com. Ind.	10 10	mA
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> CS1 = V <sub>IH</sub> , f = 1 MHz	Com. Ind.	0.35 0.35	mA
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max., CS1 ≥ V <sub>DD</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Com. Ind.	15 15	μA

Note:

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

### POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

#### 62WV5128BLL (2.5V - 3.6V)

Symbol	Parameter	Test Conditions	Max.	Unit	
			55 ns		
I <sub>CC</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com. Ind.	40 45	mA
I <sub>CC1</sub>	Operating Supply Current	V <sub>DD</sub> = Max., CS1 = 0.2V WE = V <sub>DD</sub> -0.2V f=1MHZ	Com. Ind.	15 15	mA
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> CS1 = V <sub>IH</sub> , f = 1 MHz	Com. Ind.	0.35 0.35	mA
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max., CS1 ≥ V <sub>DD</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Com. Ind.	15 15	μA

Note:

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)**

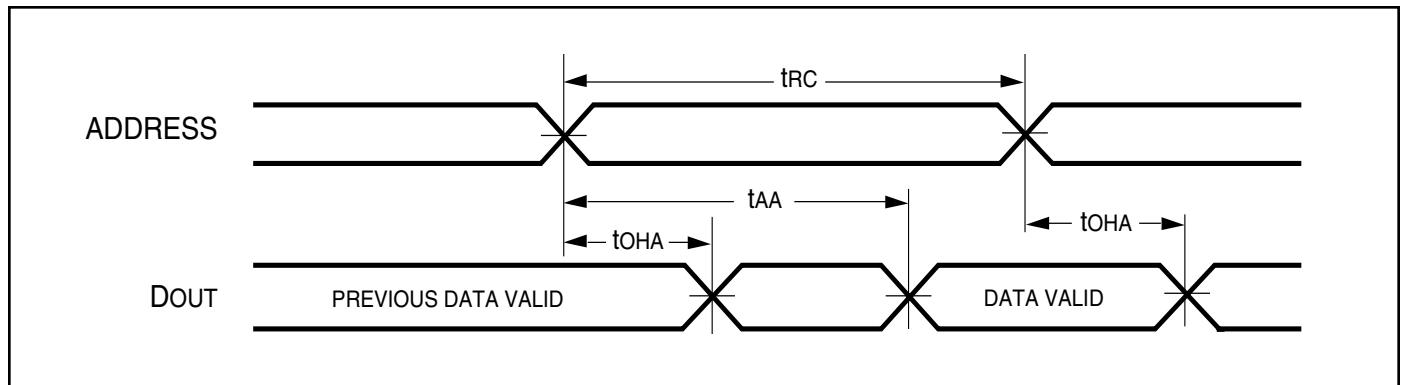
Symbol	Parameter	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	55	—	70	—	ns
t <sub>AA</sub>	Address Access Time	—	55	—	70	ns
t <sub>OHA</sub>	Output Hold Time	10	—	10	—	ns
t <sub>ACS1</sub>	CS1 Access Time	—	55	—	70	ns
t <sub>DOE</sub>	OE Access Time	—	25	—	35	ns
t <sub>HZOE<sup>(2)</sup></sub>	OE to High-Z Output	—	20	—	25	ns
t <sub>LZOE<sup>(2)</sup></sub>	OE to Low-Z Output	5	—	5	—	ns
t <sub>HZCS1</sub>	CS1 to High-Z Output	0	20	0	25	ns
t <sub>LZCS1</sub>	CS1 to Low-Z Output	10	—	10	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V<sub>DD</sub>-0.2V/V<sub>DD</sub>-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

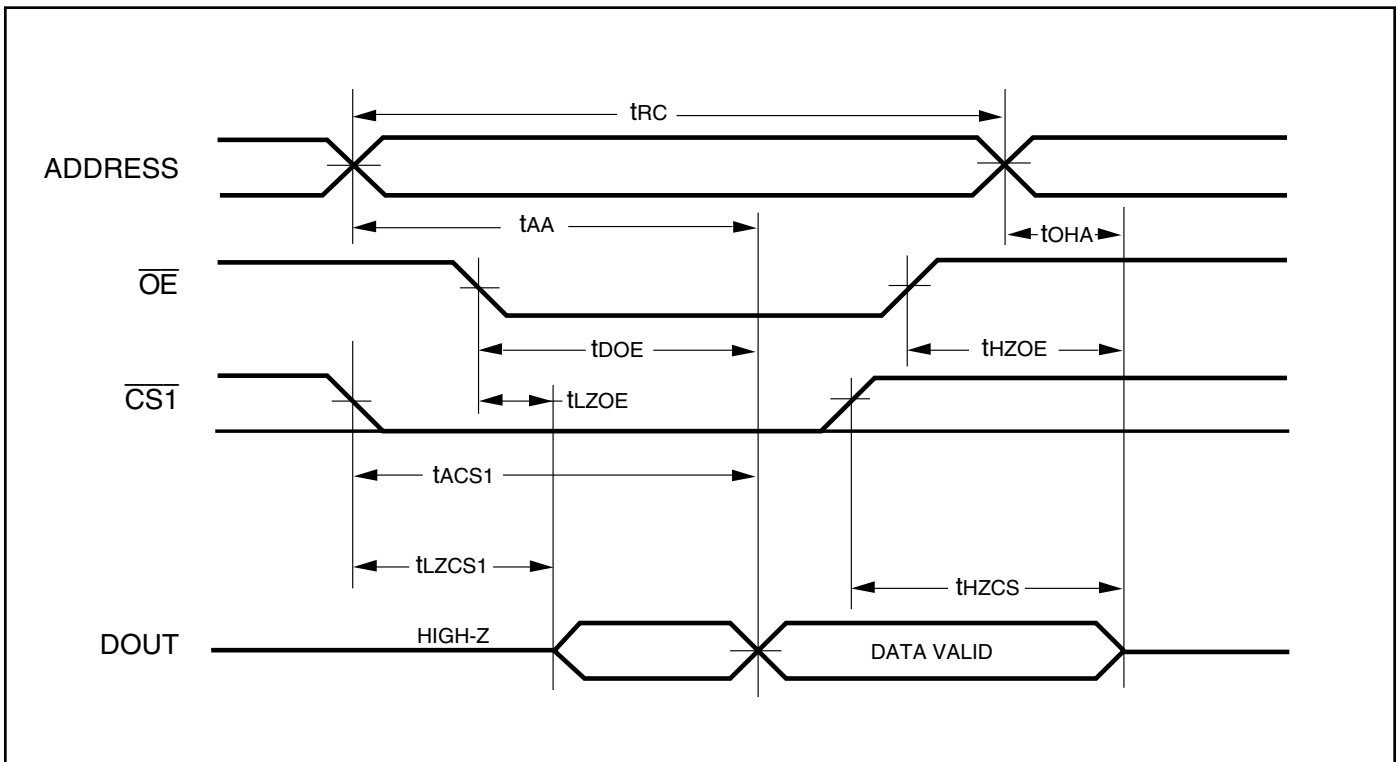
**AC WAVEFORMS**

**READ CYCLE NO. 1<sup>(1,2)</sup> (Address Controlled) (CS1 = OE = V<sub>IL</sub>, WE = V<sub>IH</sub>)**



**AC WAVEFORMS**

**READ CYCLE NO. 2<sup>(1,3)</sup> (CS1, OE Controlled)**



Notes:

1. WE is HIGH for a Read Cycle.
2. The device is continuously selected. OE, CS1= V<sub>IL</sub>. WE=V<sub>IH</sub>.
3. Address is valid prior to or coincident with CS1 LOW transition.



**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup> (Over Operating Range)**

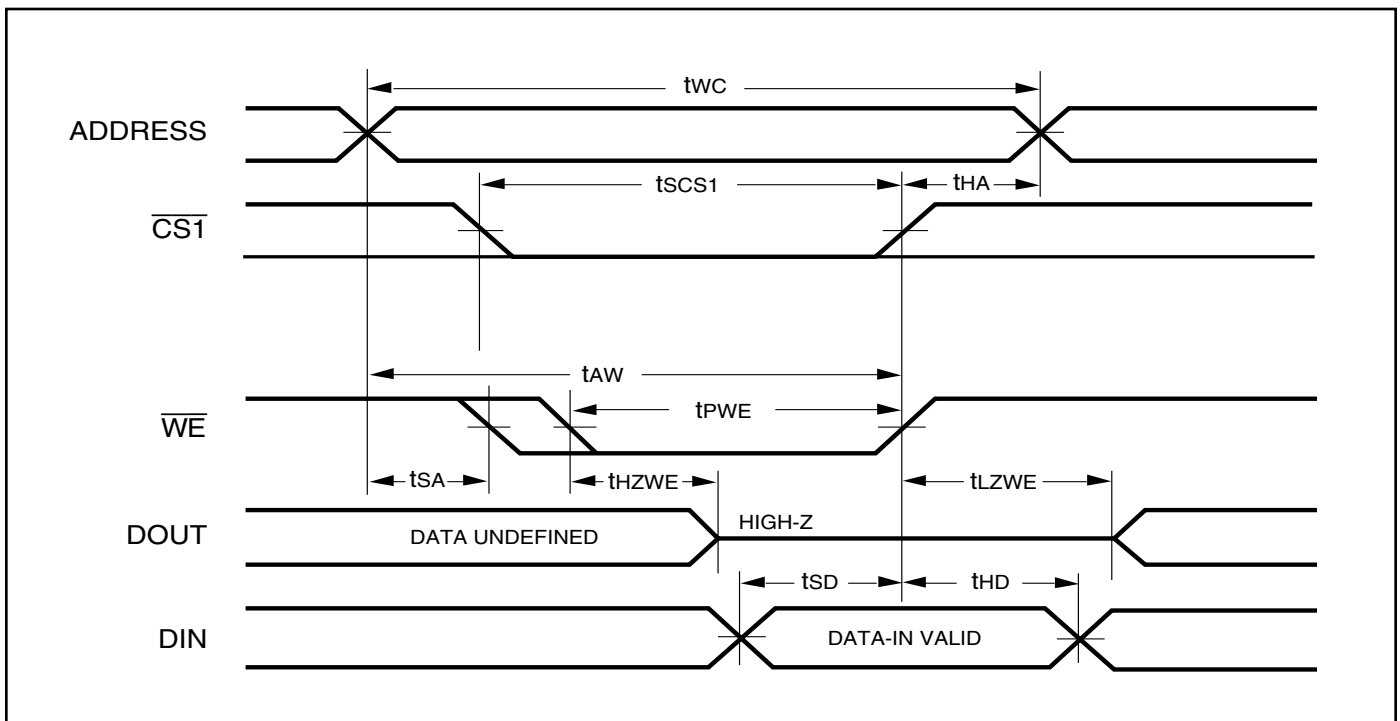
Symbol	Parameter	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
t <sub>wc</sub>	Write Cycle Time	55	—	70	—	ns
t <sub>sCS1</sub>	CS1 to Write End	45	—	60	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	45	—	60	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	ns
t <sub>PWE</sub>	WE Pulse Width	40	—	50	—	ns
t <sub>SD</sub>	Data Setup to Write End	25	—	30	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	ns
t <sub>HZWE</sub> <sup>(3)</sup>	WE LOW to High-Z Output	—	20	—	20	ns
t <sub>LZWE</sub> <sup>(3)</sup>	WE HIGH to Low-Z Output	5	—	5	—	ns

Notes:

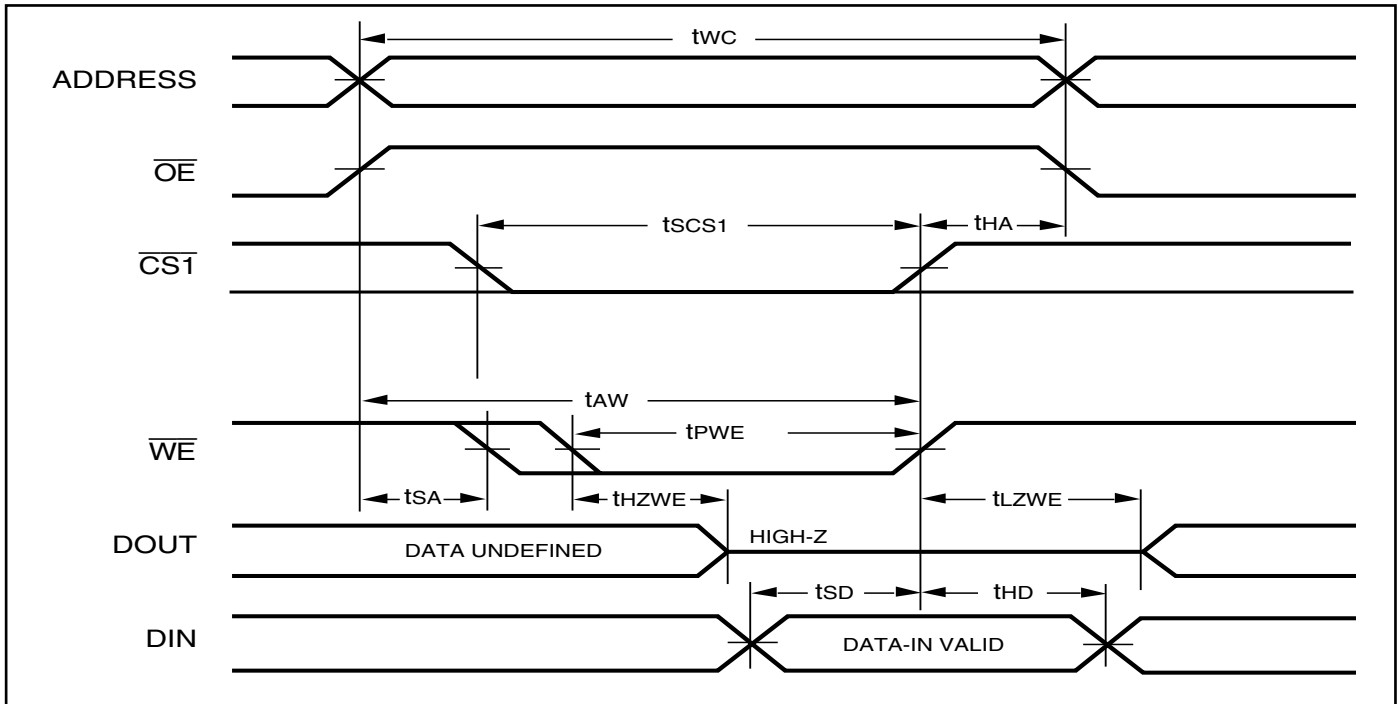
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4V to V<sub>DD</sub>-0.2V/V<sub>DD</sub>-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of CS1 LOW and WE LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

**AC WAVEFORMS**

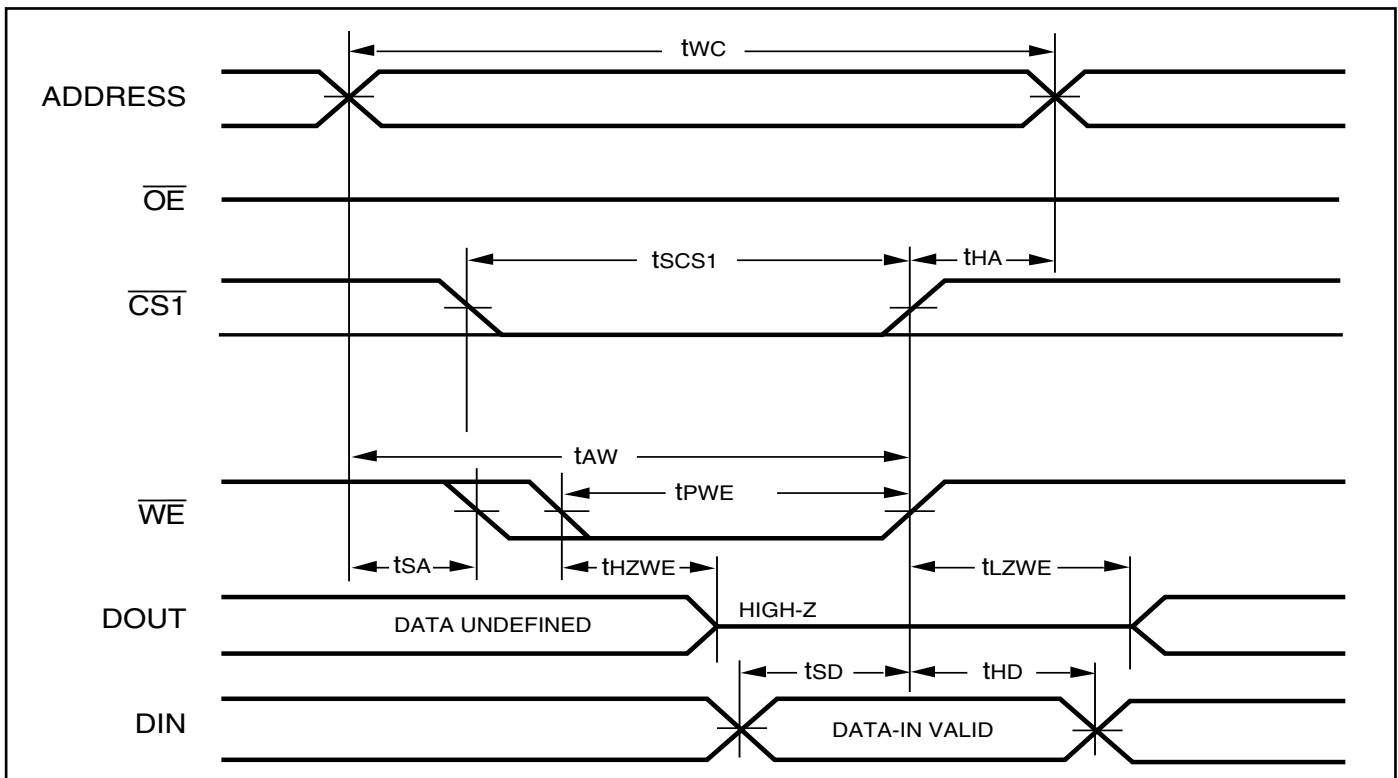
**WRITE CYCLE NO. 1 (CS1 Controlled, OE = HIGH or LOW)**



**WRITE CYCLE NO. 2 (WE Controlled: OE is HIGH During Write Cycle)**



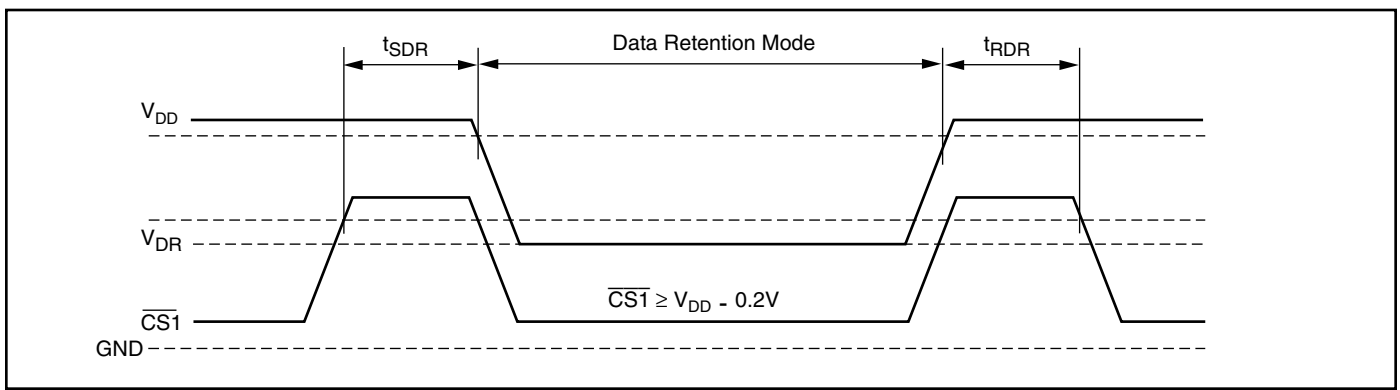
**WRITE CYCLE NO. 3 (WE Controlled: OE is LOW During Write Cycle)**



**DATA RETENTION SWITCHING CHARACTERISTICS**

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V <sub>DR</sub>	V <sub>DD</sub> for Data Retention	See Data Retention Waveform	1.2	3.6	V
I <sub>DR</sub>	Data Retention Current	V <sub>DD</sub> = 1.2V, CS1 ≥ V <sub>DD</sub> - 0.2V	—	15	μA
t <sub>SDR</sub>	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t <sub>RDR</sub>	Recovery Time	See Data Retention Waveform	t <sub>rc</sub>	—	ns

**DATA RETENTION WAVEFORM (CS1 Controlled)**





## IS62WV5128ALL, IS62WV5128BLL

### ORDERING INFORMATION

IS62WV5128ALL (1.65V-2.2V)

Industrial Range: -40°C to +85°C

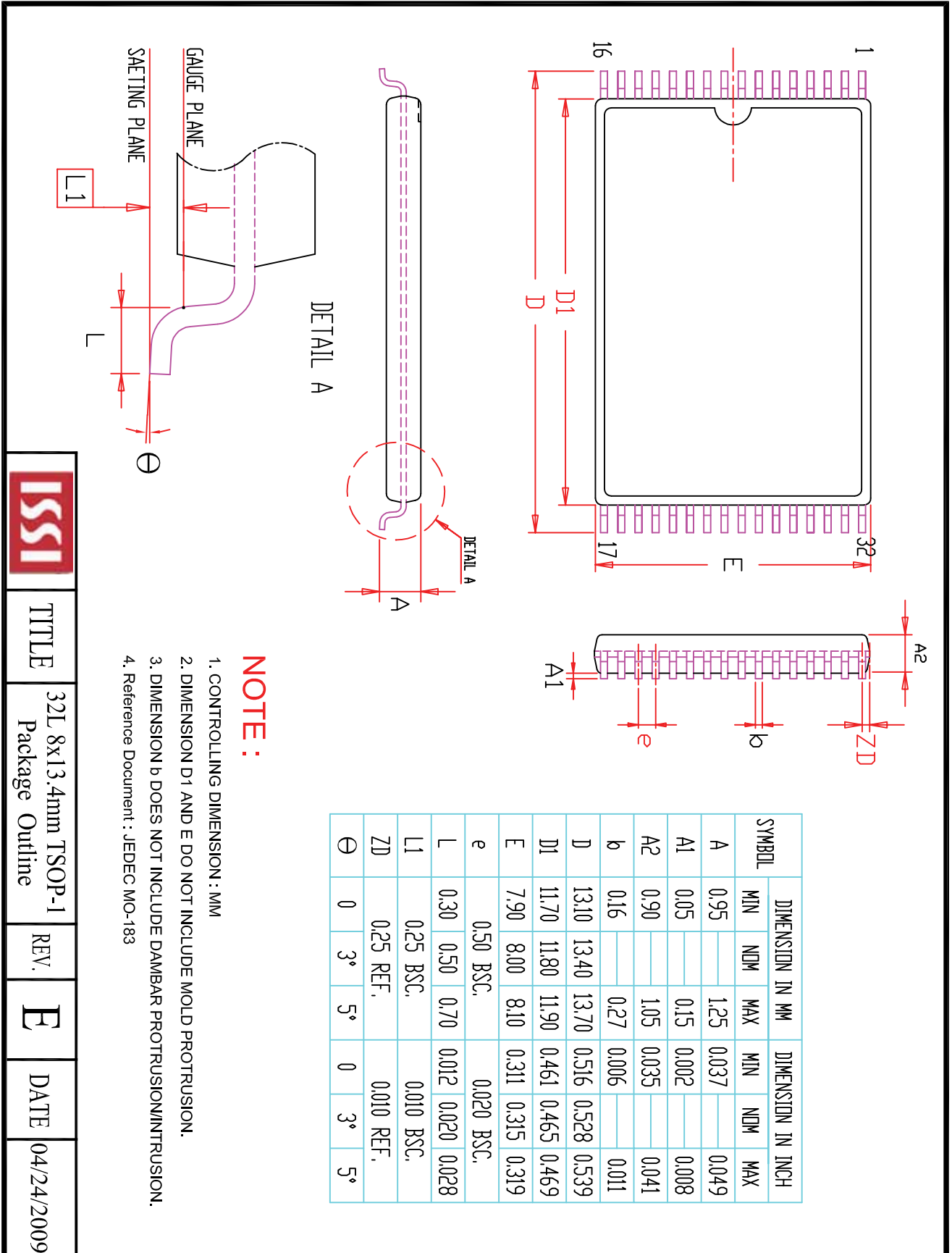
Speed (ns)	Order Part No.	Package
70	IS62WV5128ALL-70BI	mini BGA (6mmx8mm)

### ORDERING INFORMATION

IS62WV5128BLL (2.5V - 3.6V)

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS62WV5128BLL-55TLI	TSOP, TYPE I, Lead-free
55	IS62WV5128BLL-55QLI	SOP, Lead-free
55	IS62WV5128BLL-55T2LI	TSOP, TYPE II, Lead-free
55	IS62WV5128BLL-55HLI	sTSOP, TYPE I, Lead-free
55	IS62WV5128BLL-55BI	mini BGA (6mmx8mm)
55	IS62WV5128BLL-55BLI	mini BGA (6mmx8mm), Lead-free



TITLE

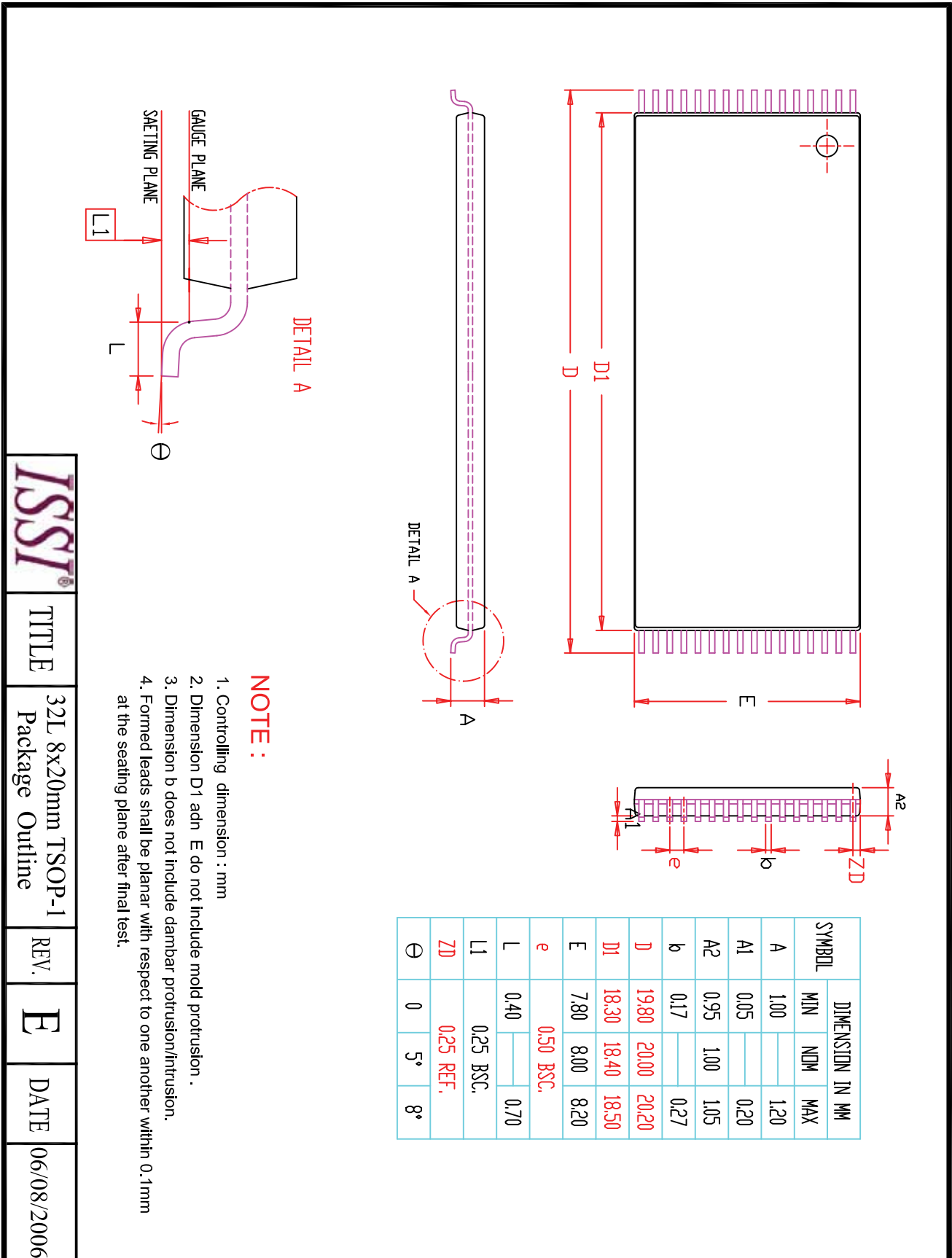
32L 8x13.4mm TSOP-1  
Package Outline

REV.

E

DATE

04/24/2009



ISSI

TITLE

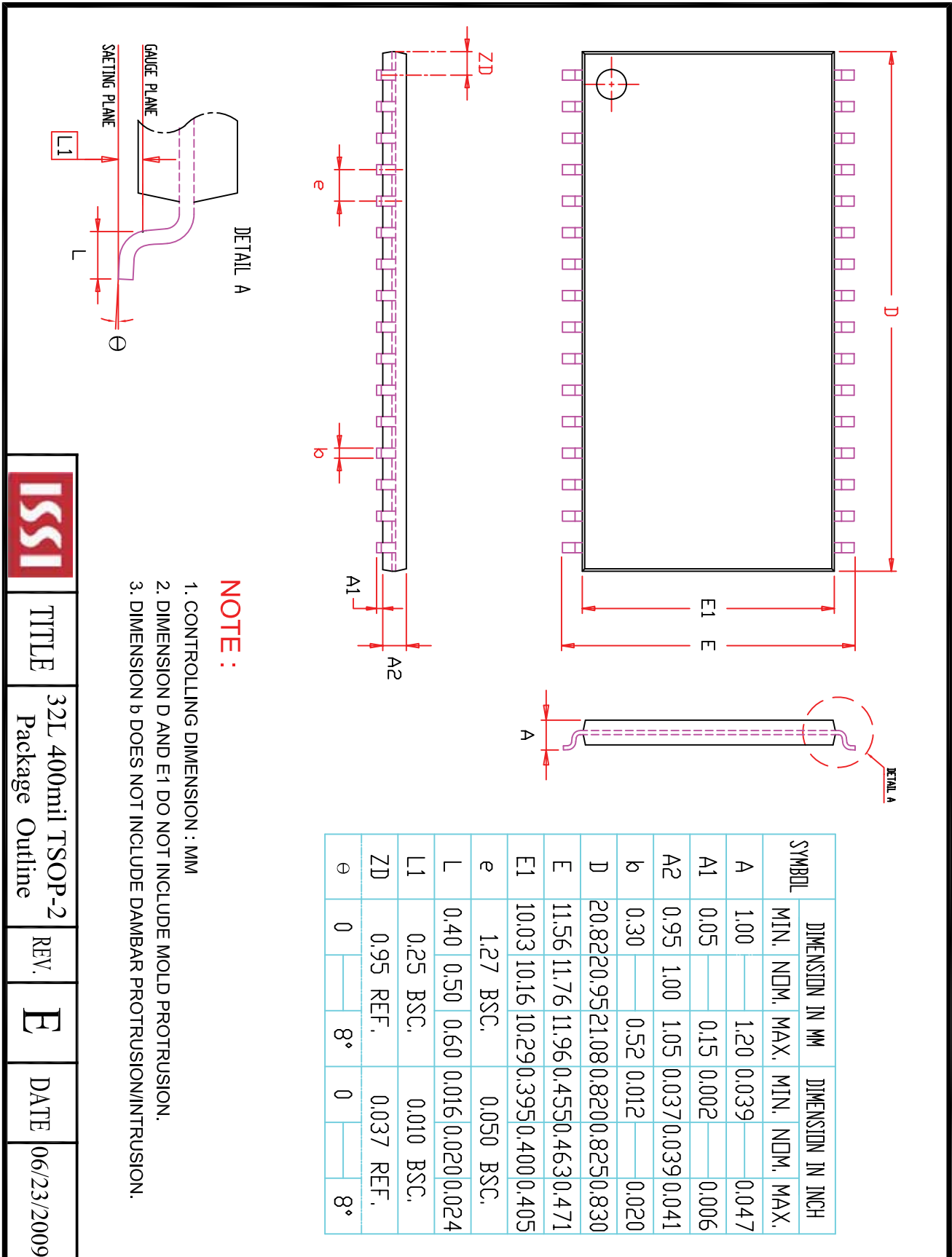
32L 8x20mm TSOP-1  
Package Outline

REV.

E

DATE

06/08/2006



**NOTE :**

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00		1.20	0.039		0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.52	0.012		0.020
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	1.27	BSC.		0.050	BSC.	
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.25	BSC.		0.010	BSC.	
ZD	0.95	REF.		0.037	REF.	
θ	0		8°	0		8°



TITLE

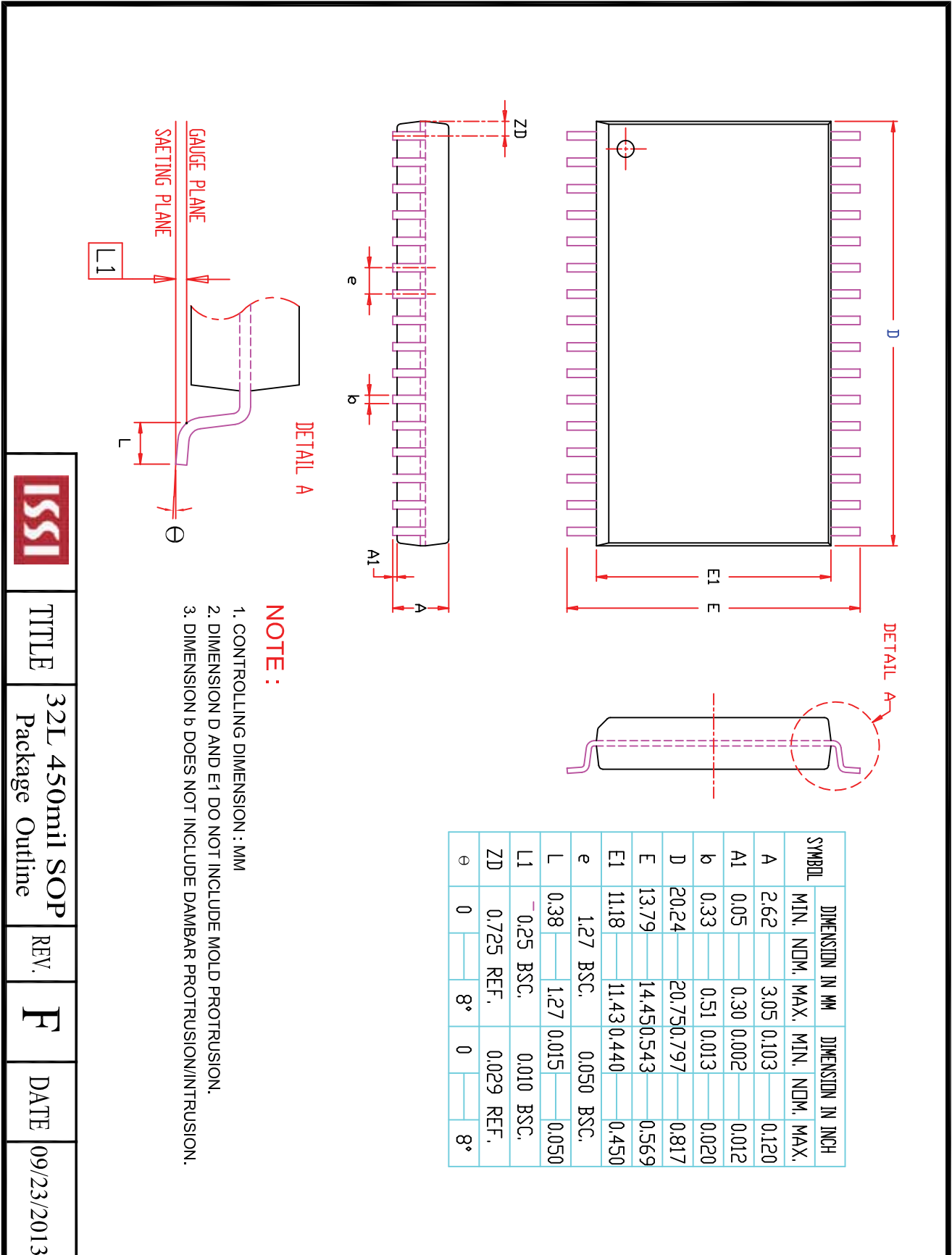
32L 400mil TSOP-2  
Package Outline

REV.

E

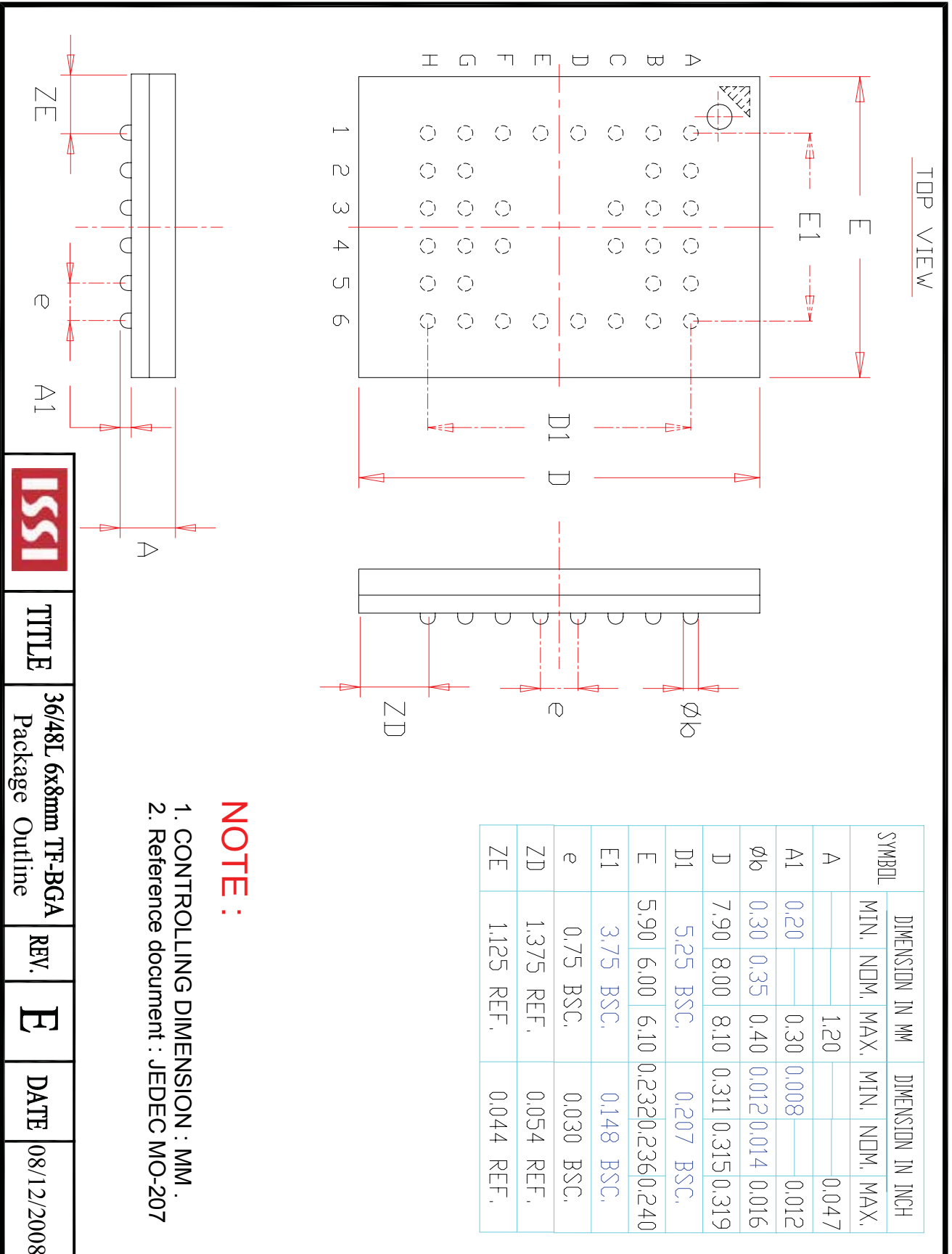
DATE

06/23/2009



	TITLE	32L 450mil SOP Package Outline	REV.	F	DATE	09/23/2013
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TITLE

36/48L 6x8mm TF-BGA  
Package Outline

REV.

E

DATE

08/12/2008

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[IDT70V5388S166BG](#) [IS64WV3216BLL-15CTLA3](#) [IS66WVE4M16ECLL-70BLI](#) [PCF8570P](#) [K6F2008V2E-LF70000](#) [K6T4008C1B-GB70](#)  
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