

# IS66WV1M16DALL IS66WV1M16DBLL



PRELIMINARY INFORMATION  
MARCH 2011

## 16Mb LOW VOLTAGE, ULTRA LOW POWER PSEUDO CMOS STATIC RAM

### FEATURES

- High-speed access time:
  - 70ns (IS66WV1M16DALL/DBLL)
  - 55ns (IS66WV1M16DBLL)
- CMOS low power operation
- Single power supply
  - $V_{DD} = 1.7V - 1.95V$  (IS66WV1M16DALL)
  - $V_{DD} = 2.5V - 3.6V$  (IS66WV1M16DBLL)
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- Lead-free available

### DESCRIPTION

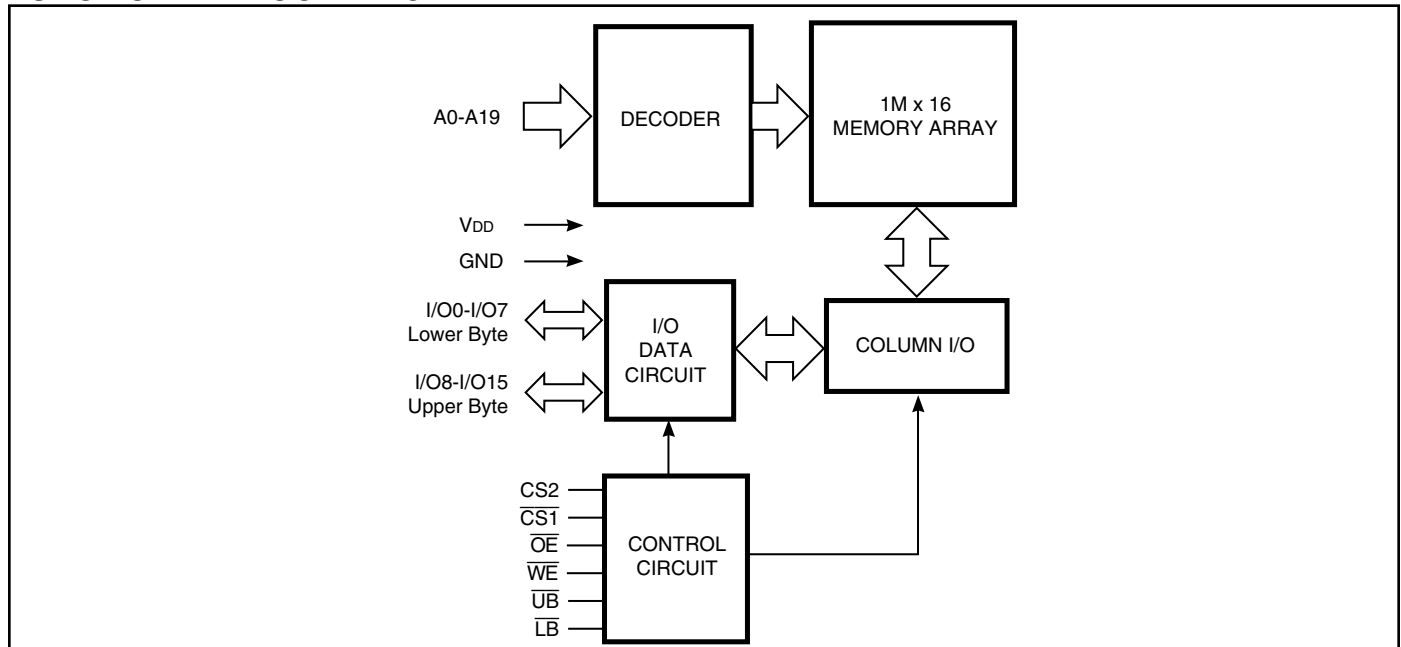
The *ISSI* IS66WV1M16DALL/DBLL is a high-speed, 16M bit static RAMs organized as 1Mb words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When  $\overline{CS1}$  is HIGH (deselected) or when CS2 is LOW (deselected) or when  $\overline{CS1}$  is LOW, CS2 is HIGH and both  $\overline{LB}$  and  $\overline{UB}$  are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory. A data byte allows Upper Byte ( $\overline{UB}$ ) and Lower Byte ( $\overline{LB}$ ) access.

The IS66WV1M16DALL/DBLL is packaged in the JEDEC standard 48-ball mini BGA (6mm x 8mm). The device is also available for die sales.

### FUNCTIONAL BLOCK DIAGRAM



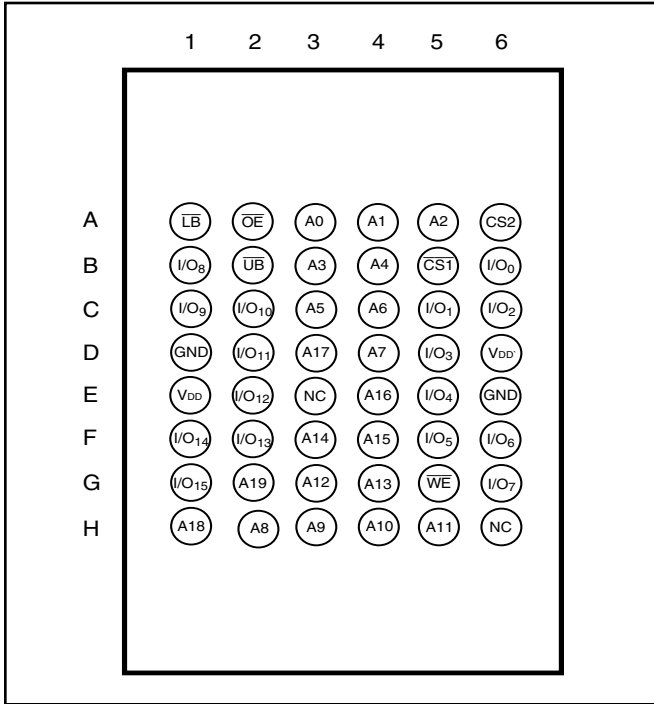
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- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

**PIN CONFIGURATIONS:**

**48-Ball mini BGA (6mm x 8mm)**



**Note:**  
TSOP package option is under evaluation.

**PIN DESCRIPTIONS**

A0-A19	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CS1}$ , CS2	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V <sub>DD</sub>	Power
GND	Ground

**TRUTH TABLE**

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN		V <sub>DD</sub> Current
							I/O0-I/O7	I/O8-I/O15	
Not Selected	X	H	X	X	X	X	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
	X	X	L	X	X	X	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
	X	X	X	X	H	H	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
Output Disabled	H	L	H	H	L	X	High-Z	High-Z	I <sub>CC</sub>
	H	L	H	H	X	L	High-Z	High-Z	I <sub>CC</sub>
Read	H	L	H	L	L	H	DOUT	High-Z	I <sub>CC</sub>
	H	L	H	L	H	L	High-Z	DOUT	
	H	L	H	L	L	L	DOUT	DOUT	
Write	L	L	H	X	L	H	D <sub>IN</sub>	High-Z	I <sub>CC</sub>
	L	L	H	X	H	L	High-Z	D <sub>IN</sub>	
	L	L	H	X	L	L	D <sub>IN</sub>	D <sub>IN</sub>	

**OPERATING RANGE (V<sub>DD</sub>)**

Range	Ambient Temperature	(70ns)	(55ns)
Commercial	0°C to +70°C	1.7V - 1.95V, 2.5V - 3.6V	2.5V - 3.6V
Industrial	-40°C to +85°C	1.7V - 1.95V, 2.5V - 3.6V	2.5V - 3.6V
Automotive	-40°C to +105°C	2.5V-3.6V	

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.2 to V <sub>DD</sub> +0.3	V
T <sub>BIAS</sub>	Temperature Under Bias	-40 to +85	°C
V <sub>DD</sub>	V <sub>DD</sub> Related to GND	-0.2 to +3.8	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W

**Note:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC ELECTRICAL CHARACTERISTICS (Over Operating Range)**

**V<sub>DD</sub> = 2.5V-3.6V**

Symbol	Parameter	Test Conditions	V <sub>DD</sub>	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1 mA	2.5-3.6V	2.2	—	V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA	2.5-3.6V	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.5-3.6V	2.2	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage		2.5-3.6V	-0.2	0.6	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>		-1	1	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled		-1	1	μA

**Notes:**

- V<sub>IL</sub> (min.) = -2.0V AC (pulse width < 10ns). Not 100% tested.  
V<sub>IH</sub> (max.) = V<sub>DD</sub> + 2.0V AC (pulse width < 10ns). Not 100% tested.

**DC ELECTRICAL CHARACTERISTICS (Over Operating Range)**

**V<sub>DD</sub> = 1.7V-1.95V**

Symbol	Parameter	Test Conditions	V <sub>DD</sub>	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	1.7-1.95V	1.4	—	V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA	1.7-1.95V	—	0.2	V
V <sub>IH</sub>	Input HIGH Voltage		1.7-1.95V	1.4	V <sub>DD</sub> + 0.2	V
V <sub>IL</sub>	Input LOW Voltage		1.7-1.95V	-0.2	0.4	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>		-1	1	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled		-1	1	μA

**Notes:**

- V<sub>IL</sub> (min.) = -1.0V AC (pulse width < 10ns). Not 100% tested.  
V<sub>IH</sub> (max.) = V<sub>DD</sub> + 1.0V AC (pulse width < 10ns). Not 100% tested.

### CAPACITANCE<sup>(1)</sup>

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	8	pF
C <sub>OUT</sub>	Input/Output Capacitance	V <sub>OUT</sub> = 0V	10	pF

**Note:**

1. Tested initially and after any design or process changes that may affect these parameters.

### AC TEST CONDITIONS

Parameter	1.7V-1.95V (Unit)	2.5V-3.6V (Unit)
Input Pulse Level	0.4V to V <sub>DD</sub> -0.2	0.4V to V <sub>DD</sub> -0.3V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V <sub>REF</sub>	V <sub>REF</sub>
Output Load	See Figures 1 and 2	See Figures 1 and 2

	1.7V - 1.95V	2.5V - 3.6V
R1(Ω)	3070	1029
R2(Ω)	3150	1728
V <sub>REF</sub>	0.9V	1.4V
V <sub>TM</sub>	1.8V	2.8V

### AC TEST LOADS

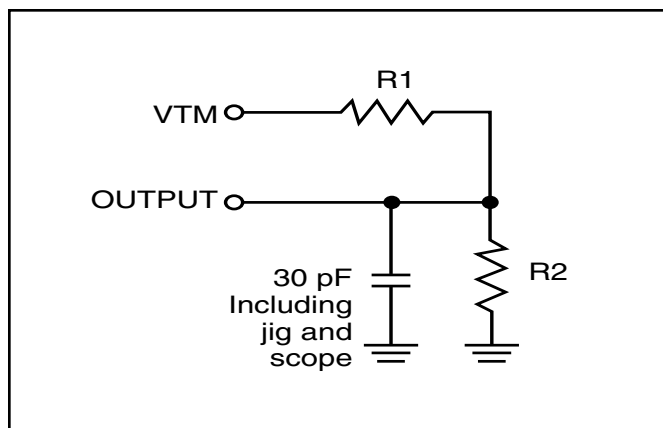


Figure 1

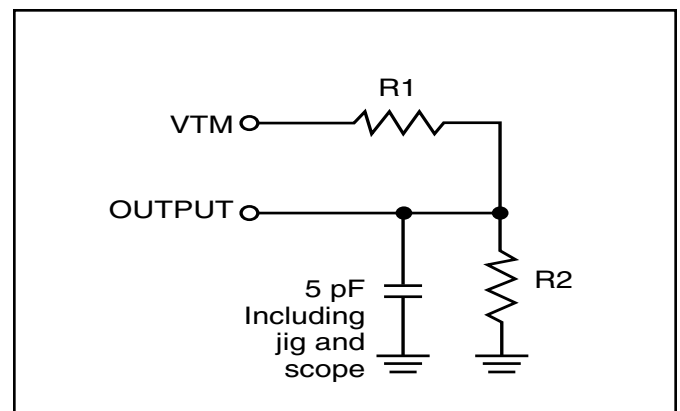


Figure 2

**1.7V-1.95V POWER SUPPLY CHARACTERISTICS** (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 70ns	Unit
I <sub>CC</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max.,	Com.	20	mA
		I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Ind.	25	
		All Inputs 0.4V or V <sub>DD</sub> - 0.2V	Auto.	30	
I <sub>CC1</sub>	Operating Supply Current	V <sub>DD</sub> = Max., $\overline{CS1} = 0.2V$	Com.	4	mA
		$\overline{WE} = V_{DD} - 0.2V$	Ind.	4	
		CS2 = V <sub>DD</sub> - 0.2V, f = 1MHz	Auto.	10	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max.,	Com.	0.6	mA
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	Ind.	0.6	
		$\overline{CS1} = V_{IH}$ , CS2 = V <sub>IL</sub> , f = 1 MHz	AUTO.	1	
	<b>OR</b>				
	ULB Control	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IL}$ , f = 0, $\overline{UB} = V_{IH}$ , $\overline{LB} = V_{IH}$			
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max.,	Com.	100	μA
		$\overline{CS1} \geq V_{DD} - 0.2V$ ,	Ind.	120	
		CS2 ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Auto.	150	
	<b>OR</b>				
	ULB Control	V <sub>DD</sub> = Max., $\overline{CS1} = V_{IL}$ , CS2=V <sub>IH</sub> V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0; $\overline{UB} / \overline{LB} = V_{DD} - 0.2V$			

**Note:**

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

**2.5V-3.6V POWER SUPPLY CHARACTERISTICS** (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 55ns	Unit
I <sub>CC</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max.,	Com.	25	mA
		I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Ind.	28	
		All Inputs 0.4V	Auto.	35	
		or V <sub>DD</sub> - 0.3V	typ. <sup>(2)</sup>	15	
I <sub>CC1</sub>	Operating Supply Current	V <sub>DD</sub> = Max., $\overline{CS1} = 0.2V$	Com.	5	mA
		$\overline{WE} = V_{DD} - 0.2V$	Ind.	5	
		CS2 = V <sub>DD</sub> - 0.2V, f = 1MHz	AUTO.	10	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max.,	Com.	0.6	mA
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	Ind.	0.6	
		$\overline{CS1} = V_{IH}$ , CS2 = V <sub>IL</sub> ,	AUTO.	1	
		f = 1 MHz			
	<b>OR</b>				
	ULB Control	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IL}$ , f = 0, $\overline{UB} = V_{IH}$ , $\overline{LB} = V_{IH}$			
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max.,	Com.	100	μA
		$\overline{CS1} \geq V_{DD} - 0.2V$ ,	Ind.	130	
		CS2 ≤ 0.2V,	Auto.	150	
		V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	typ. <sup>(2)</sup>	75	
	<b>OR</b>				
	ULB Control	V <sub>DD</sub> = Max., $\overline{CS1} = V_{IL}$ , CS2 = V <sub>IH</sub> V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0; $\overline{UB} / \overline{LB} = V_{DD} - 0.2V$			

**Note:**

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

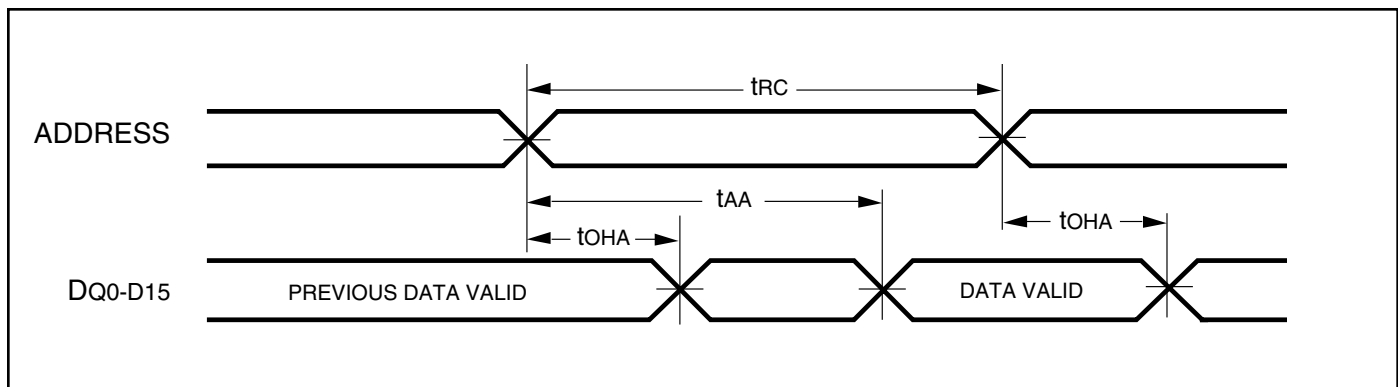
Symbol	Parameter	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	55	—	70	—	ns
t <sub>AA</sub>	Address Access Time	—	55	—	70	ns
t <sub>OHA</sub>	Output Hold Time	10	—	10	—	ns
t <sub>ACS1</sub> /t <sub>ACS2</sub>	$\overline{CS1}/CS2$ Access Time	—	55	—	70	ns
t <sub>DOE</sub>	$\overline{OE}$ Access Time	—	25	—	35	ns
t <sub>HZOE<sup>(2)</sup></sub>	$\overline{OE}$ to High-Z Output	—	20	—	25	ns
t <sub>LZOE<sup>(2)</sup></sub>	$\overline{OE}$ to Low-Z Output	5	—	5	—	ns
t <sub>HZCS1</sub> /t <sub>HZCS2<sup>(2)</sup></sub>	$\overline{CS1}/CS2$ to High-Z Output	0	20	0	25	ns
t <sub>LZCS1</sub> /t <sub>LZCS2<sup>(2)</sup></sub>	$\overline{CS1}/CS2$ to Low-Z Output	10	—	10	—	ns
t <sub>BA</sub>	$\overline{LB}, \overline{UB}$ Access Time	—	55	—	70	ns
t <sub>HZB</sub>	$\overline{LB}, \overline{UB}$ to High-Z Output	0	20	0	25	ns
t <sub>LZB</sub>	$\overline{LB}, \overline{UB}$ to Low-Z Output	0	—	0	—	ns

**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V<sub>DD</sub>-0.2V/0.4V to V<sub>DD</sub>-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±100 mV from steady-state voltage. Not 100% tested.

**AC WAVEFORMS**

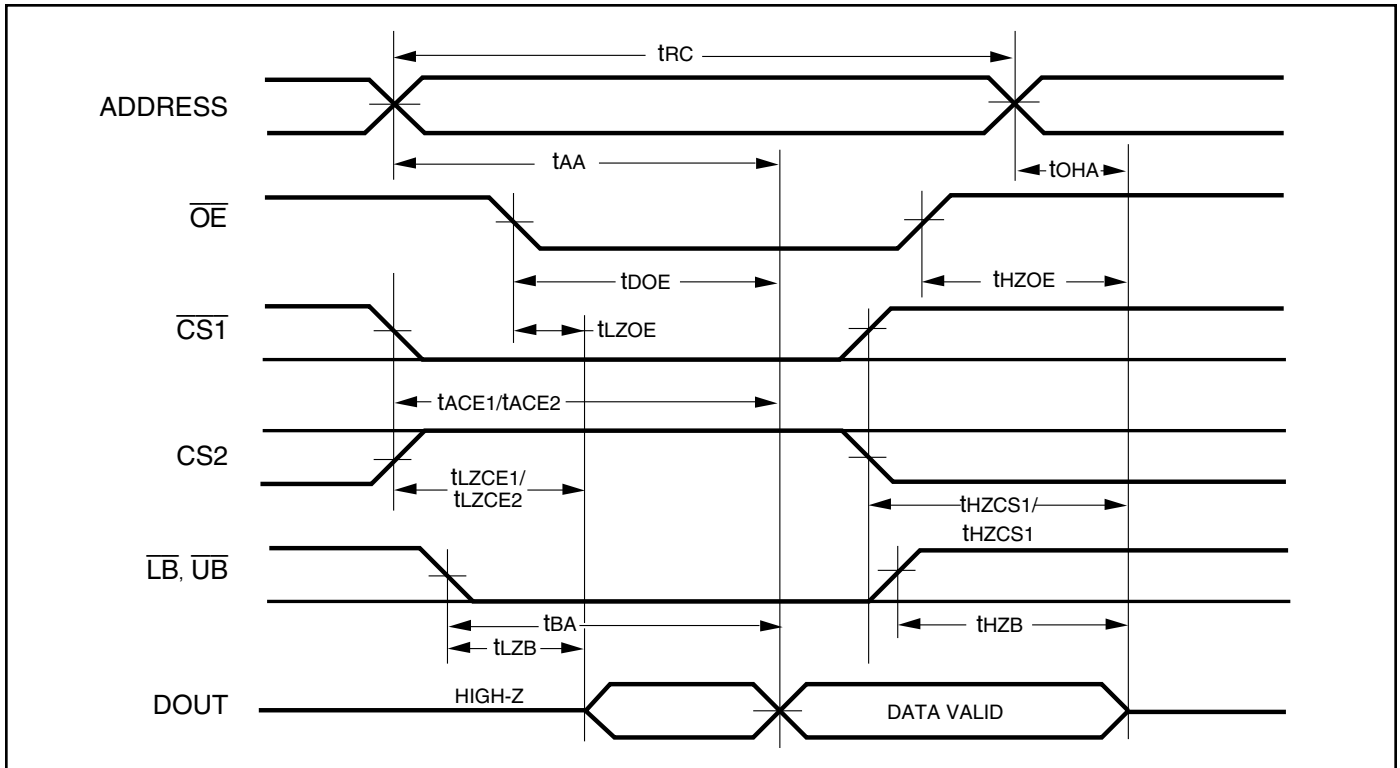
**READ CYCLE NO. 1<sup>(1,2)</sup>** (Address Controlled) ( $\overline{CS1} = \overline{OE} = V_{IL}$ ,  $CS2 = \overline{WE} = V_{IH}$ ,  $\overline{UB}$  or  $\overline{LB} = V_{IL}$ )





AC WAVEFORMS

READ CYCLE NO. 2<sup>(1,3)</sup> ( $\overline{CS1}$ ,  $CS2$ ,  $\overline{OE}$ , AND  $\overline{UB}/\overline{LB}$  Controlled)



Notes:

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CS1}$ ,  $\overline{UB}$ , or  $\overline{LB} = V_{IL}$ .  $CS2 = \overline{WE} = V_{IH}$ .
3. Address is valid prior to or coincident with  $\overline{CS1}$  LOW transition.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup> (Over Operating Range)**

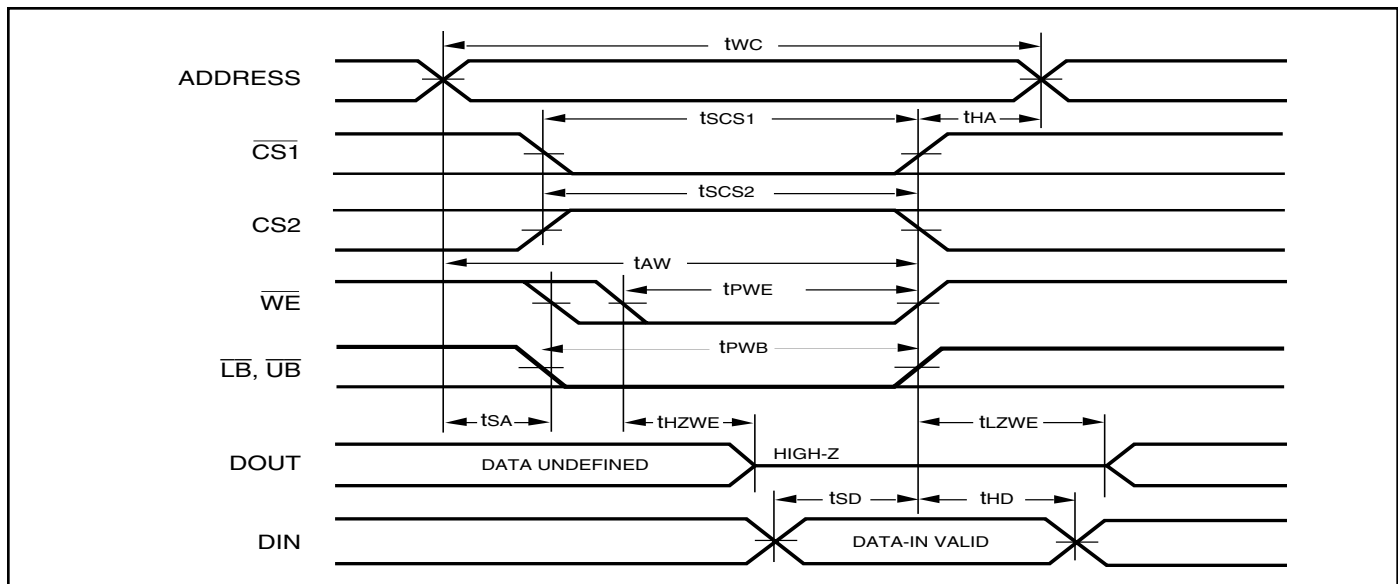
Symbol	Parameter	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
t <sub>wc</sub>	Write Cycle Time	55	—	70	—	ns
t <sub>sCS1/tSCS2</sub>	$\overline{CS1}/CS2$ to Write End	45	—	60	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	45	—	60	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	ns
t <sub>PWB</sub>	$\overline{LB}$ , $\overline{UB}$ Valid to End of Write	45	—	60	—	ns
t <sub>PWE<sup>(4)</sup></sub>	$\overline{WE}$ Pulse Width	45	15,000	60	15,000	ns
t <sub>SD</sub>	Data Setup to Write End	25	—	30	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	ns
t <sub>HZWE<sup>(3)</sup></sub>	$\overline{WE}$ LOW to High-Z Output	—	20	—	30	ns
t <sub>LZWE<sup>(3)</sup></sub>	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	ns

**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V<sub>DD</sub>-0.2V/0.4V to V<sub>DD</sub>-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of  $\overline{CS1}$  LOW, CS2 HIGH and  $\overline{UB}$  or  $\overline{LB}$ , and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured  $\pm 100$  mV from steady-state voltage. Not 100% tested.
4. t<sub>PWE</sub> > t<sub>HZWE</sub> + t<sub>SD</sub> when  $\overline{OE}$  is LOW.

**AC WAVEFORMS**

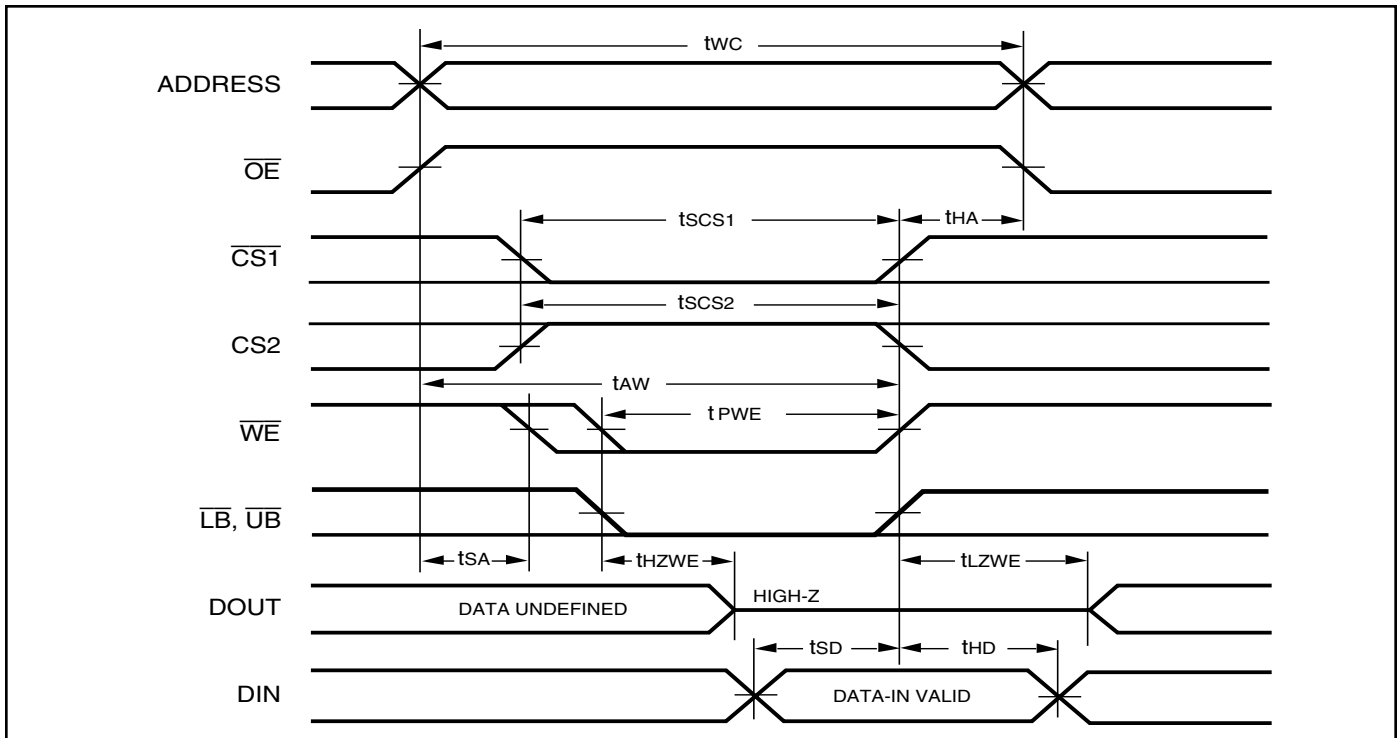
**WRITE CYCLE NO. 1<sup>(1,2)</sup> ( $\overline{CS1}$  Controlled,  $\overline{OE}$  = HIGH or LOW)**



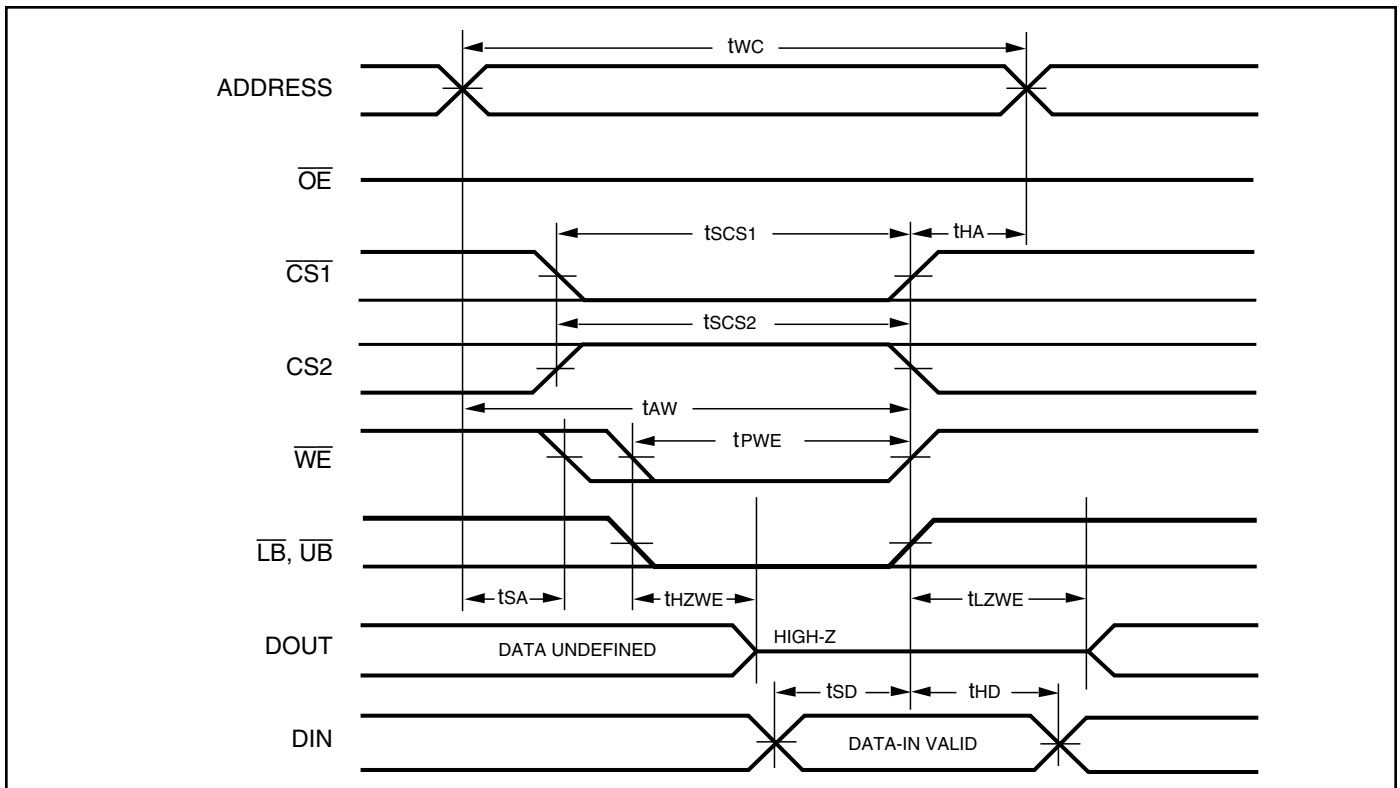
**Notes:**

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the  $\overline{CS1}$ , CS2 and  $\overline{WE}$  inputs and at least one of the  $\overline{LB}$  and  $\overline{UB}$  inputs being in the LOW state.
2. WRITE = ( $\overline{CS1}$ ) [ ( $\overline{LB}$ ) = ( $\overline{UB}$ ) ] ( $\overline{WE}$ ).

**WRITE CYCLE NO. 2** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is HIGH During Write Cycle)



**WRITE CYCLE NO. 3** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is LOW During Write Cycle)



WRITE CYCLE NO. 4 ( $\overline{UB}/\overline{LB}$  Controlled)

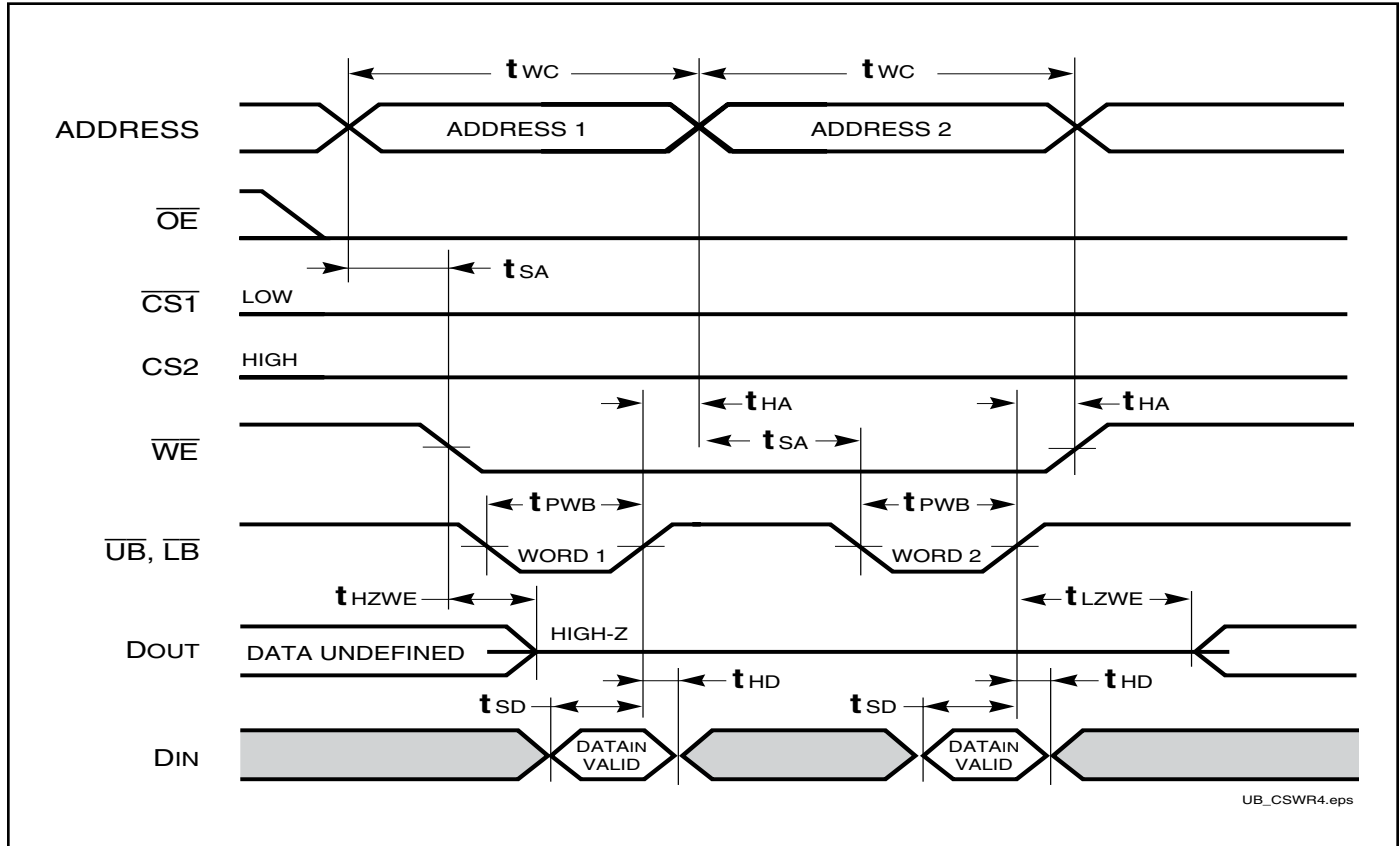


Figure 1: Avoidable Timing

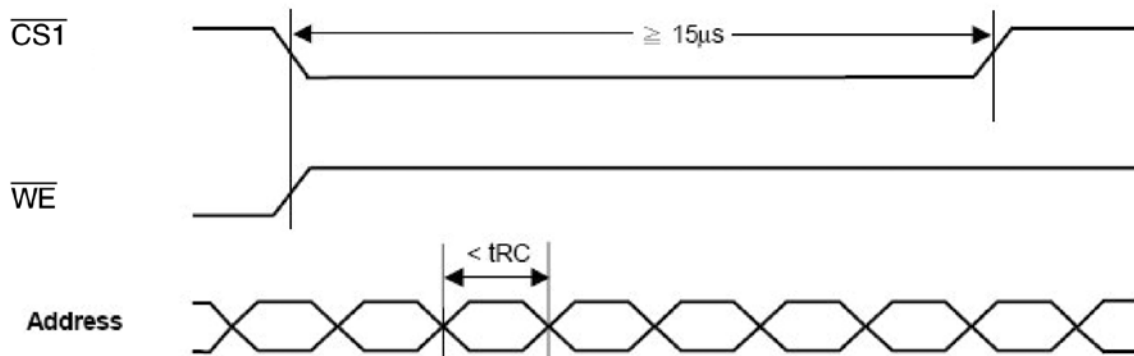


Figure 2:

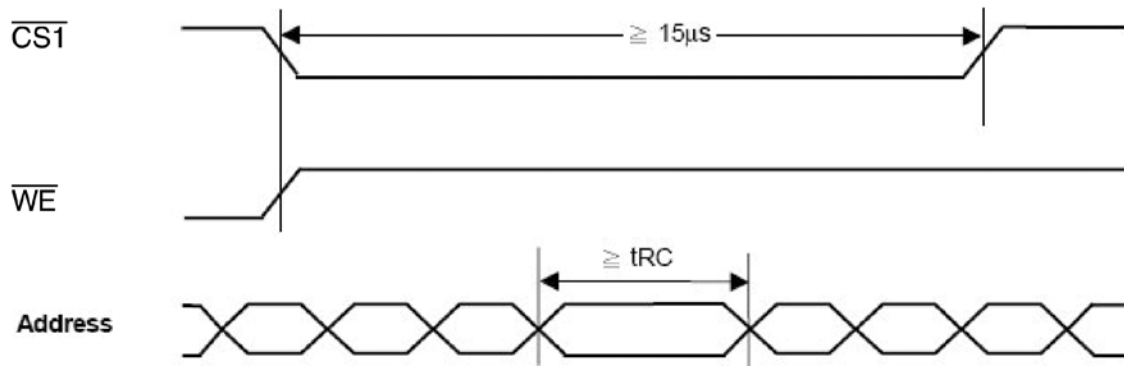
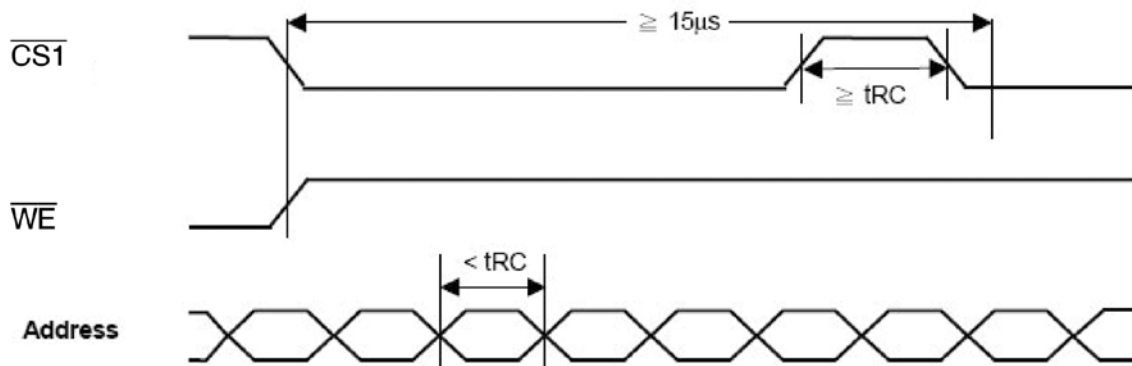


Figure 3:



Please avoid address change for less than  $t_{RC}$  during the cycle time longer than  $15\mu s$  (Figure 1). Figure 2 & 3 provide work around solution for this issue.

**IS66WV1M16DALL**  
**IS66WV1M16DBLL**



**IS66WV1M16DALL**

**Industrial Range: -40°C to +85°C**

**Voltage Range: 1.7V to 1.95V**

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<b>Speed (ns)</b>	<b>Order Part No.</b>	<b>Package</b>
70	IS66WV1M16DALL-70BLI	mini BGA (6mm x 8mm), Lead-free

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**IS66WV1M16DBLL**

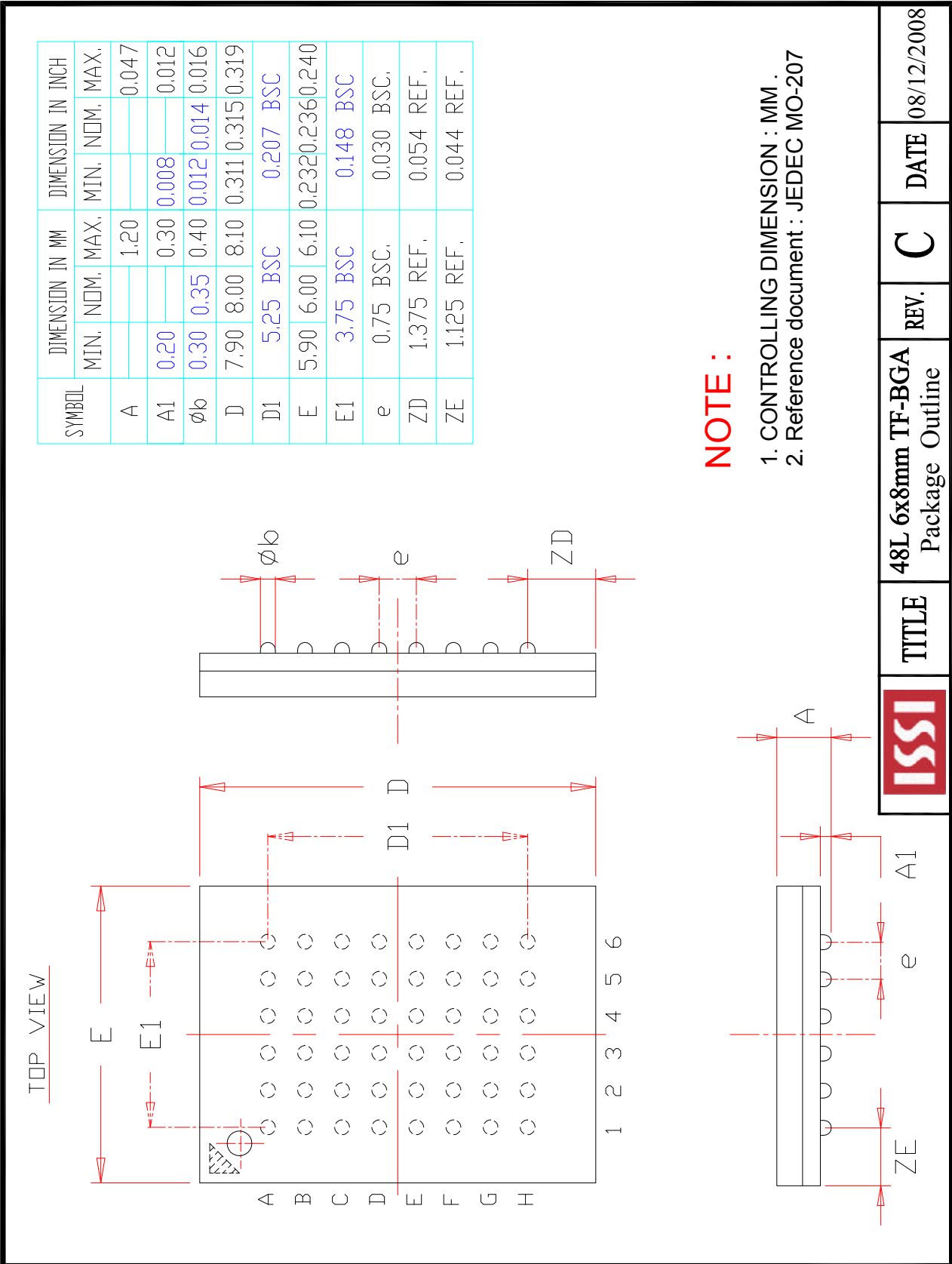
**Industrial Range: -40°C to +85°C**

**Voltage Range: 2.5V to 3.6V**

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<b>Speed (ns)</b>	<b>Order Part No.</b>	<b>Package</b>
55	IS66WV1M16DBLL-55BLI	mini BGA (6mm x 8mm), Lead-free
70	IS66WV1M16DBLL-70BLI	mini BGA (6mm x 8mm), Lead-free

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[IDT70V5388S166BG](#) [IS64WV3216BLL-15CTLA3](#) [IS66WVE4M16ECLL-70BLI](#) [PCF8570P](#) [K6F2008V2E-LF70000](#) [K6T4008C1B-GB70](#)  
[CY7C1353S-100AXC](#) [AS6C8016-55BIN](#) [AS7C164A-15PCN](#) [515712X](#) [IDT71V67603S133BG](#) [IS62WV51216EBLL-45BLI](#)  
[IS63WV1288DBLL-10HLI](#) [IS66WVE2M16ECLL-70BLI](#) [IS66WVE4M16EALL-70BLI](#) [IS62WV6416DBLL-45BLI](#) [IS61WV102416DBLL-](#)  
[10TLI](#) [CY7C1381KV33-100AXC](#) [CY7C1381KVE33-133AXI](#) [8602501XA](#) [5962-3829425MUA](#) [5962-3829430MUA](#) [5962-8855206YA](#)  
[5962-8866201YA](#) [5962-8866204TA](#) [5962-8866206MA](#) [5962-8866208UA](#) [5962-8872502XA](#) [5962-9062007MXA](#) [5962-9161705MXA](#)  
[GS882Z18CD-150I](#) [M38510/28902BVA](#) [8413202RA](#) [5962-9161708MYA](#) [5962-8971203XA](#) [5962-8971202ZA](#) [5962-8872501LA](#) [5962-](#)  
[8866208YA](#) [5962-8866205YA](#) [5962-8866205UA](#) [5962-8866203YA](#) [5962-8855202YA](#) [5962-8751309VA](#) [5962-8687519XA](#)