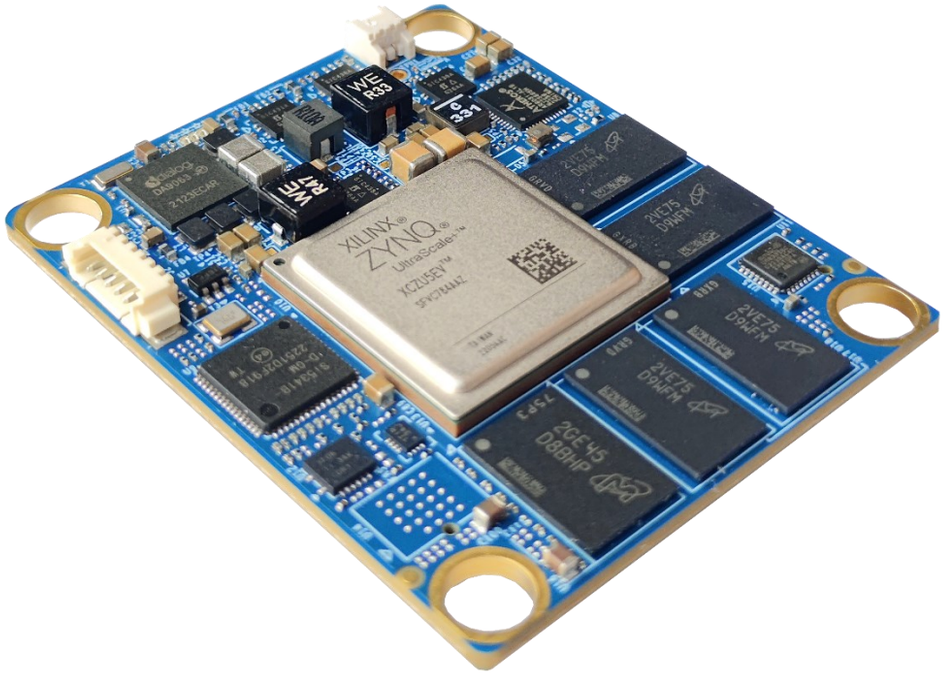
iW-RainboW-G36M
Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM Datasheet



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0.3	21st Feb 2024	Updated with SOM & DevKit Images
0.4	22nd July 2024	Updated "Reset Out, HS PCIe Reset, 1PPS_IN, Dedicated_INT" signal description and SOM Power consumption details
0.5	07th Aug 2024	Updated B2B Connector Pinout

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Table of Contents

List of Figures

List of Tables

1. INTRODUCTION

1.1 Purpose

This document is the datasheet for the Zynq UltraScale+ MPSoC System on Module based on the Xilinx Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1). This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the Zynq UltraScale+ MPSoC System on Module from a Hardware Systems perspective.

1.2 SOM Overview

The Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM is an extension of Zynq UltraScale+ MPSoC. Zynq UltraScale+ MPSoC SOM has a form factor of 50mm x 60mm and provides the functional requirements for an embedded application. Two High-Speed High-Density connectors provide the carrier board interface to carry all the I/O signals to and from the Zynq UltraScale+ MPSoC SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ADC	Analog to Digital Converter
ARM	Advanced RISC Machine
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
DDR4 SDRAM	Double Data Rate fourth-generation Synchronous Dynamic Random Access Memory
FPGA	Field Programmable Gate Array
eMMC	Embedded Multimedia Card
GB	Giga Byte
Gbps	Gigabits per sec
GEM	Gigabit Ethernet Controller
GHz	Giga Hertz
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second
LVDS	Low Voltage Differential Signalling
MAC	Media Access Controller
MB	Mega Byte
Mbps	Megabits per sec
MHz	Mega Hertz
NPTH	Non-Plated Through hole

Acronyms	Abbreviations
PCB	Printed Circuit Board
PMIC	Power Management Integrated Circuit
PTH	Plated Through hole
PL	Programmable Logic
PS	Processing System
RGMII	Reduced Gigabit Media Independent Interface
RTC	Real Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output
SGMII	Serial Gigabit Media Independent Interface
SoC	System On Chip
SOM	System On Module
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus
USB OTG	USB On the Go
UTMI	USB2.0 Transceiver Macrocell Interface

1.4 Terminlogy Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB	Universal Serial Bus differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SOM.

1.5 References

- Zynq UltraScale+ MPSoC Technical Reference Manual
- Zynq UltraScale+ MPSoC Device Overview

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM features and Hardware architecture with high level block diagram. Also, this section provides detailed information about Board-to-Board connectors pin assignment and usage.

2.1 Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM Block Diagram

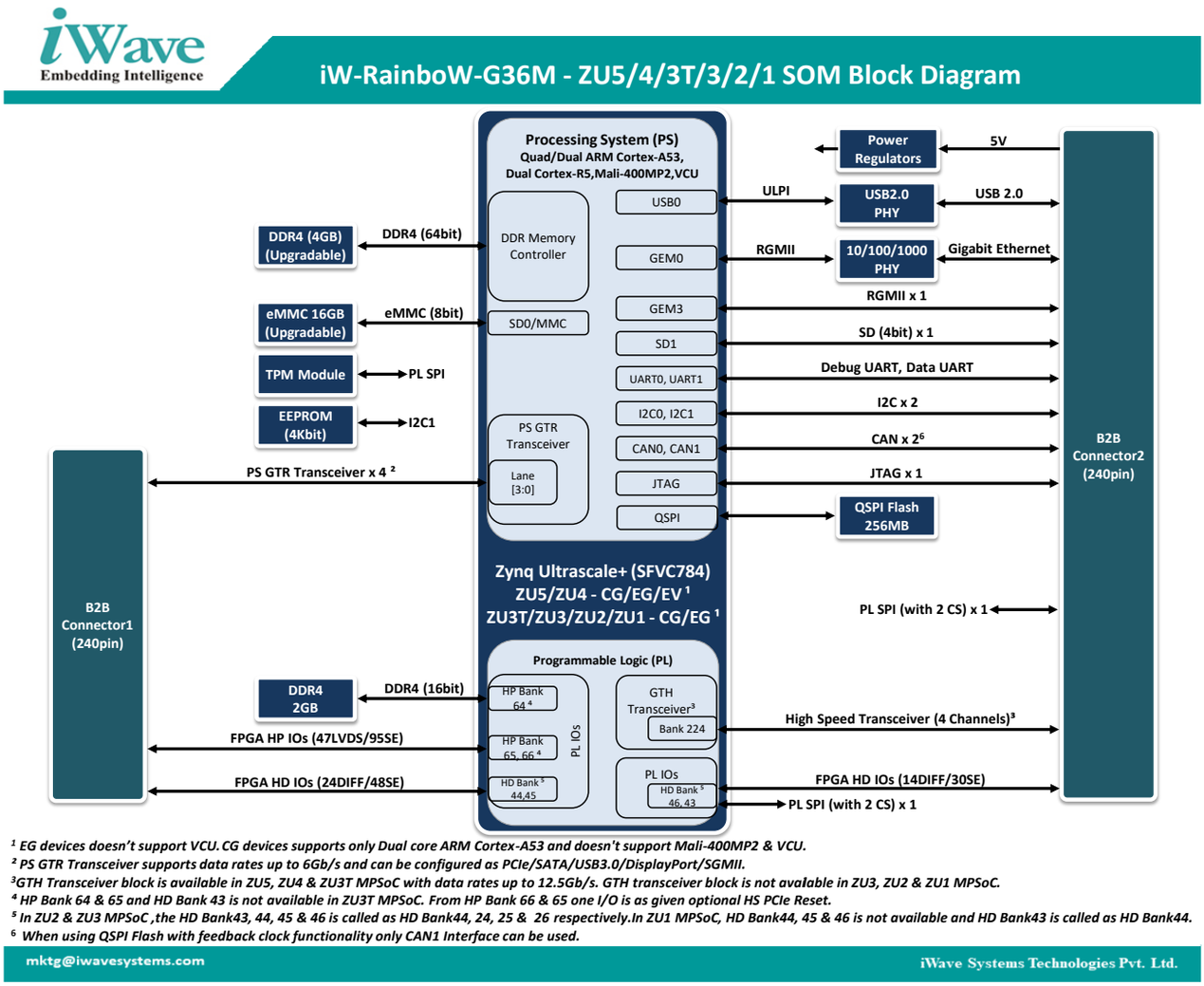

Figure 1: Zynq UltraScale+ MPSoC SOM Block Diagram

2.2 Zynq UltraScale+ MPSoC SOM Features

The Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1-EV, EG, CG) SOM supports the following features.

SoC

- Xilinx Zynq UltraScale+ MPSoC
  - Compatible Zynq Ultrascale+ MPSoC Family (SFVC784) – ZU5EV/EG/CG, ZU4EV/EG/CG, ZU3TEG/CG, ZU3EG/CG, ZU2EG/CG, ZU1EG/CG
  - Programming Logic with up to 256.2K Logic cells and Processing System with integrated Quad-core ARM Cortex-A53 MPCore Application processor (up to 1.5GHz), Dual-core ARM Cortex-R5 MPCore Real Time Processor (up to 600MHz) and Mali™-400 MP2 Graphics Processor.

PMIC

- Renesas/Dialog's DA9063 PMIC with RTC

Memory

- 4GB DDR4 (64bit) for PS (Upgradable upto 8GB)
- 2GB DDR4 (16bit) for PL
- 16GB eMMC Flash (Upgradable upto 128GB)
- 2Kbit EEPROM
- 256MB QSPI Flash

Other On-SOM Features

- Gigabit Ethernet PHY Transceiver
- USB2.0 Transceiver
- TPM 2.0 Module
- Fan Header

Board-to-Board Connector 1 Interfaces (240pin)

From PS Block

- PS-GTR High Speed Transceivers[2] (Upto 6Gbps) x 4

From PL Block

- PL IOs - HP Bank66
  - Upto 24 Differential IOs/48 Single ended IOs
- PL IOs - HP Bank65[4]
  - Upto 24 Differential IOs/48 Single ended IOs

- PL IOs - HD Bank44
  - Upto 12 Differential/24 Single ended IOs
- PL IOs - HD Bank45[5]
  - Upto 12 Differential/24 Single ended IOs

Board-to-Board Connector 2 Interfaces (240pin)

From PS Block

- Gigabit Ethernet x 1 Port (through On-SOM Gigabit Ethernet PHY transceiver)
- RGMII x1 Port
- USB2.0 OTG x 1 Port (through On-SOM USB2.0 transceiver)
- SD (4bit) x 1 Port
- CAN Interface x 2[3]
- Debug UART x 1 Port
- Data UART x 1 Port
- I2C x 2 Ports
- JTAG

From PL Block

- PL-GTH High Speed Transceivers[4] (Upto 12.5Gbps) x 4
- PL IOs - HD Bank43[5]
  - Upto 8 Differential/ 17 Single ended (SE) IOs
- PL IOs - HD Bank46[6]
  - Upto 7 Differential/ 15 Single ended (SE) IOs
- SPI x 1 (with 2 CS) Port

General Specification

- Power Supply : 5V (from Board-to-Board Connector 2)
- Form Factor : 60mm x 50mm (REN Form Factor)

[1] EG devices doesn't support VCU. CG devices support only Dual core ARM Cortex-A53 and doesn't support Mali-400MP2 & VCU.

[2] PS GTR Transceiver supports data rates up to 6Gb/s and can be configured as PCIe/SATA/USB3.0/DisplayPort/SGMII.

[3] When using QSPI Flash with feedback clock functionality of CAN1 Interface can be used.

[4] GTH Transceiver block is available in ZU5, ZU4 & ZU3T MPSoC with data rates up to 12.5Gb/s. GTH transceiver block is not available in ZU3, ZU2 & ZU1 MPSoC.

[5] *HP Bank 64 & 65 and HD Bank 43 is not available in ZU3T MPSoC.*

[6] *In ZU2 & ZU3 MPSoC, the HD Bank43, 44, 45 & 46 is called as HD Bank44, 24, 25 & 26 respectively. In ZU1 MPSoC, HD Bank44, 45 & 46 is not available and HD Bank43 is called as HD Bank44.*

2.3 Zynq UltraScale+ MPSoC

Xilinx's SoC portfolio integrates the software programmability of a processor with the hardware programmability of an FPGA, providing unrivalled levels of system performance, flexibility, and scalability. Unlike traditional SoC processing solutions, the flexible programmable logic provides optimization and differentiation, allowing to add the peripherals and accelerators for a broad base of applications.

The Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM is based on Xilinx Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) with SFVC784 package. Zynq UltraScale+ MPSoC family integrates Processing system (PS) and Xilinx programmable logic (PL) in a single device. MPSoC's Processing system includes feature-rich Quad-core ARM Cortex-A53 MPCore up to 1.5 GHz of Application processor, Dual-core ARM Cortex-R5 MPCore up to 600MHz and Mali™-400 MP2 of Graphics Processor. The Block Diagram of Zynq UltraScale+ MPSoC from Xilinx website is shown below for reference.

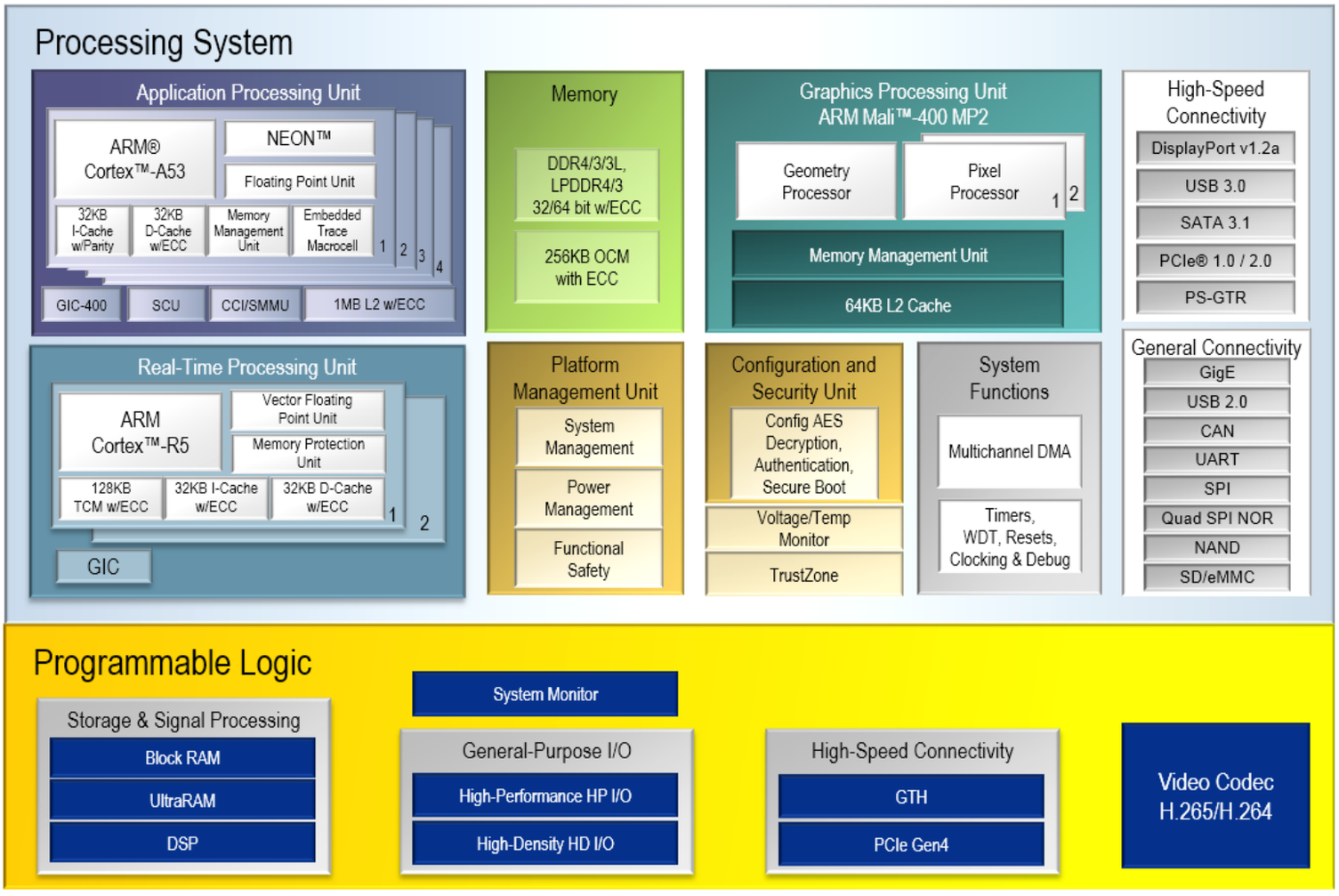

Figure 2: Zynq UltraScale+ MPSoC CPU Simplified Block Diagram

Note: Please refer the latest Zynq UltraScale+ MPSoC Datasheet & Technical Reference Manual for more details which may be revised from time to time.

The Zynq UltraScale+ MPSoC SOM is compatible to ZU5/4/3T/3/2/1 – EV/EG/CG MPSoC devices and feature comparison between these devices are shown below.

	ZU5EV	ZU5EG	ZU5CG	ZU4EV	ZU4EG	ZU4CG	ZU3TEG	ZU3TCG	ZU3EG	ZU3CG	ZU2EG	ZU2CG	ZU1EG	ZU1CG
Application Processing Unit	Quad-core Arm Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache													
Real-Time Processing Unit	Dual-core Arm Cortex-R5F with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM													
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; Emmc													
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters													
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII													
Graphics Processing Unit	Yes		No	Yes		No	Yes	No	Yes	No	Yes	No	Yes	No
Video Codec	1	0	0	1	0	0	0	0	0	0	0	0	0	0
System Logic Cells	2,56,200			1,92,150			1,57,500		1,54,350		1,03,320		81,900	
CLB Flip-Flops	2,34,240			1,75,680			1,44,000		1,41,120		94,464		74,880	
CLB LUTs	1,17,120			87,840			72,000		70,560		47,232		37,440	
Distributed RAM (Mb)	3.5			2.6			2		2		1		1	
Block RAM Blocks	144			128			144		216		150		108	
Block RAM (Mb)	5.1			4.5			5		8		5		4	
UltraRAM Blocks	64			48			48		0		0		0	
UltraRAM (Mb)	18			13.5			14		0		0		0	
DSP Slices	1,248			728			576		360		240		216	
CMTs	4			4			1		3		3		3	
Max. HP I/Os	156			156			52		156		156		156	
Max. HD I/Os	96			96			72		96		96		24	
System Monitor	2			2			2		2		2		1	
GTH Transceivers (12.5Gb/s)	8			8			8		0		0		0	
Transceiver Fractional PLLs	4			4			4		0		0		0	
PCIe Express	1			1			1		0		0		0	

Figure 3: Zynq UltraScale+ MPSoC Devices Comparison

The Zynq UltraScale+ MPSoC's PS has 78 dedicated I/O pins referred as MIO (Multiplexed I/O) for the PS peripheral interfaces. These 78 MIO pins are divided into three banks (PS BANK500, 501 & 502) and each bank includes 26 device pins. Since 78 MIO pins are not enough to support simultaneous use of all the peripherals supported by PS, there is option in MPSoC to route most of the IO peripheral interfaces to PL Bank I/O pins referred as EMIO (Extended MIO). Zynq UltraScale+ MPSoC's PS Peripheral Pin mapping options between MIO & EMIO is shown below.

Peripheral Interface	MIO	EMIO
Quad-SPI NAND	Yes	No
USB2.0: 0,1	Yes: External PHY	No
SDIO 0,1	Yes	Yes
SPI: 0,1	Yes	Yes
I2C: 0,1	Yes	Yes
CAN: 0,1	CAN: External PHY	CAN: External PHY
GPIO	GPIO: Up to 78 bits	GPIO: Up to 96 bits
GigE: 0,1,2,3	RGMII v2.0: External PHY	Supports GMII, RGMII v2.0 (HSTL), RGMII v1.3, MII, SGMII, and 1000BASE-X in Programmable Logic
UART: 0,1	Simple UART: Only two pins (TX and RX)	Full UART (TX, RX, DTR, DCD, DSR, RI, RTS, and CTS) requires either: • Two Processing System (PS) pins (RX and TX) through MIO and six

Peripheral Interface	MIO	EMIO
		additional Programmable Logic (PL) pins, or • Eight Programmable Logic (PL) pins
Debug Trace Ports	Yes: Up to 16 trace bits	Yes: Up to 32 trace bits
Processor JTAG	Yes	Yes

The Zynq UltraScale+ MPSoC's PL Banks are classified as high-performance (HP) banks or high-density (HD) banks. The HP Bank I/Os are optimized for highest performance operation organized in banks of 52pins. The HD Bank I/Os are reduced-features I/Os organized in banks of 24pins.

In Zynq UltraScale+ MPSoC PL, each bank supports four global clock (GC or HDGC) input pin pairs. GC pins have direct access to the global clock buffers, MMCMs and PLLs of the same Bank. HDGC pins are from HD I/O banks and have direct access only to the global clock buffers.

Also, Zynq UltraScale+ MPSoC supports two types of high-speed transceivers namely GTH and PS-GTR. These transceivers are arranged in groups of four known as a transceiver Quad GTH transceivers are from PL and PS-GTR transceivers are from PS.

2.3.1 MPSoC Power

The Zynq UltraScale+ MPSoC SOM uses discrete power regulators and the DA9063 PMIC from Dialog Semiconductor (Renesas) to manage MPSoC power. In the SOM, the PS low-power domain, PS full-power domain, and PL power domain supply voltage (VCC_PSINTLP, VCC_PSINTFP, VCCINT) are fixed at either 0.85V/0.72V or 0.9V, depending on the speed grade of the MPSoC. Additionally, all PS Bank I/O voltages (VCCO_PSIO) are fixed at 1.8V.

The I/O voltage of PL HP Bank 65 is generated from LDO6, while PL HP Bank 66 is generated from LDO9. PL HD Bank 44 and 45 supply voltages are generated from PMIC LDOs LDO3 and LDO4, respectively. PL HD Bank 43 and 46 supply voltages are combined and generated from PMIC LDO7. By default, HP Banks voltages are set to 1.0V, and HD Banks voltages are set to 1.2V, but they can be configured through software during bootup.

2.3.2 MPSoC Reset

The Zynq UltraScale+ MPSoC SOM uses the PMIC's Reset output (nRESET) for the PS Power On Reset, which is connected to the PS_POR_B pin of the MPSoC. Additionally, it supports a warm reset input from Board-to-Board Connector-2 pin B11, which is connected to the PS_SRST_B pin of the MPSoC.

2.3.3 MPSoC Reference Clock

The Zynq UltraScale+ MPSoC SOM supports a on board clock synthesizer and oscillators for reference clock to different blocks of Zynq UltraScale+ MPSoC. These reference clock details are mentioned in the below table.

Table 3: Zynq UltraScale+ MPSoC SOM Reference Clock.

Sl. No	On-SOM Synthesizer	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
1	33.3333MHz	PS_REF_CLK	PS - 503	R16	1.8V, LVCMOS	33.33MHz single ended reference clock for PS from OUT0 of Clock Synthesizer.
2	100MHz	IO_L5P_HDGC_AD7P_43	PL – HD43	AE12	1.8V[1], LVCMOS	100MHz single ended reference clock for PL from OUT1 of Clock Synthesizer. This is connected to PL Bank43 HDGC Global clock pin for ZU5/4/3/2/1 MPSoC Devices
		IO_L5P_HDGC_AD7P_46	PL – HD46	D15		100MHz single ended reference clock for PL from OUT1 of Clock Synthesizer. This is connected to PL Bank46 HDGC Global clock pin for ZU3T MPSoC Device.
3	300MHz	IO_L13N_T2L_N1_GC_QBC_64	PL – HP64	AD4	1.8V, LVDS	LVDS reference clock for PL DDR4 SDRAM. This is connected to PL Bank64 Global clock pins from OUT7 of Clock Synthesizer.
		IO_L13P_T2L_N0_GC_QBC_64		AD5		
4	27MHz	PS_MGTREFCLK3P_505	PS - 505	A21	1.8V, LVDS	LVDS reference clock for PS GTR Lane 3. This is generated from OUT3 of Clock Synthesizer.
		PS_MGTREFCLK3N_505		A22		
5	125MHz	PS_MGTREFCLK2P_505	PS - 505	C21	1.8V, LVDS	LVDS Reference clock for PS GTR Lane 2. This is generated from OUT5 of Clock synthesizer.
		PS_MGTREFCLK2N_505		C22		
6	100MHz	PS_MGTREFCLK1P_505	PS - 505	E21	1.8V, LVDS	LVDS Reference clock for PS GTR Lane 1. This is generated from OUT6 of Clock Synthesizer.
		PS_MGTREFCLK1N_505		E22		
7	156.25MHz	MGTREFCLK1P_224	PL GTH 224	V6	1.8V, LVDS	LVDS Secondary reference clock for PL GTH Bank 224. This is generated from OUT4 of Clock synthesizer.
		MGTREFCLK1N_224		V5		

[1] I/O voltage of PL Bank43 and Bank46 is software configurable. Since this clock synthesizer supports 1.8V to 3.3V VDDO only, this reference clock can be used only if the I/O voltage of PL Bank43 or 46 is set between 1.8V to 3.3V.

2.3.4 MPSoC Configuration & Status

The Zynq UltraScale+ MPSoC uses a multi-stage boot process that supports both non-secure and secure boot modes. The PS is responsible for managing the boot and configuration process. After resetting, the device executes code from on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the on-chip RAM. The FSBL initiates the boot of the PS, which can then load and configure the PL. Alternatively, configuration of the PL can be deferred to a later stage.

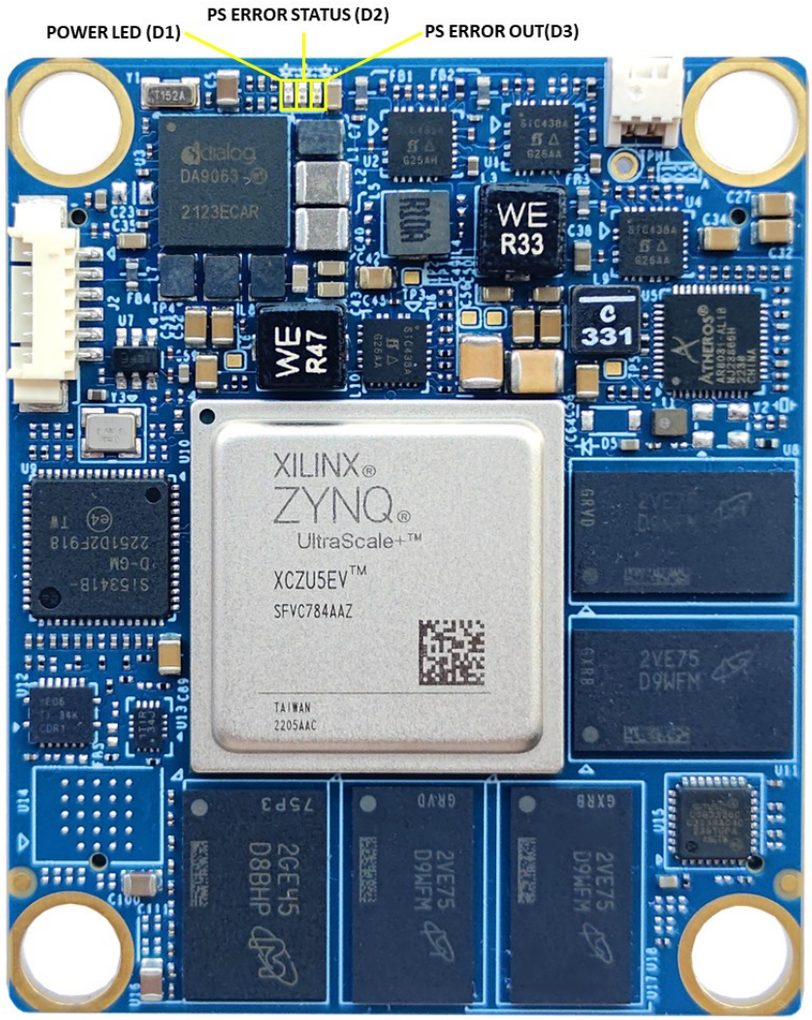

Figure 4: Error Status Indication LEDs

The Zynq UltraScale+ MPSoC SOM supports three LEDs for the MPSoC error status indication namely PS_ERROR_OUT, PS_ERROR_STATUS and Power LED. LED D3 is for PS_ERROR_OUT and it is asserted for accidental loss of power, a hardware error or an exception in the PMU. LED D2 is for PS_ERROR_STATUS and it indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status. LED D1 is for power indication which is connected to the last voltage rail of SOM power sequence

The Zynq UltraScale+ MPSoC SOM supports three dedicated input and output configuration pins - PUDC_B, POR_OVERRIDE & PS-Done. By default, Weak pre -reconfiguration I/O pull-up resistors disabled for PUDC_B pin, Standard PL power-on delay time for POR_OVERRIDE pin and PS_DONE pin is connected to VCC_1V8 through 4.7K.

2.3.5 MPSoC Boot Mode

The Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM always boots from PS first and configures the PL through software. Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM can support eMMC, SD1, USB0, QSPI & JTAG as boot device and configurable through mode pins which are extended to the Board-to-Board Connector 2. Upon device reset, MPSoC mode pins are read to determine the primary boot device. By default, eMMC is supported as boot device in SBC.

Please refer the below table for boot media selection and supported configuration details.

Table 4: Boot Mode Truth Table

BOOTMODE SELECTION				
BOOTMEDIA	**PSMODE3**	**PSMODE2**	**PSMODE1**	**PSMODE0**
eMMC (1.8V)	0	1	1	0
SD1 (2.0)	0	1	0	1
USB0 (2.0)	0	1	1	1
QSPI	0	0	1	0
PS JTAG	0	0	0	0

Note: In Zynq UltraScale+ MPSoC SOM, the boot media setting is fixed through resistors.

Please refer **Power and Control Pins** Section for the details related to Boot Media pin allocation at Board-to-Board Connector 2

2.3.6 MPSoC System Monitor/ADC

The Zynq UltraScale+ MPSoC contain two System Monitor block (SYSMONE4), one in the PL (PL SYSMON) and another in the PS (PS SYSMON). It is used to enhance the overall safety, security and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors.

The PL SYSMON uses 10-bit 200kSPS ADC to digitize the sensor/ADC inputs. It monitors the die temperature in the PL and several internal PL and PS power supply nodes. The PL SYSMON can also monitor up to 17 external analog channels which includes 16 auxiliary analog inputs and one VP_VN dedicated input. The external auxiliary inputs can be routed through any PL Bank. The ADC voltage reference is selectable between an internal reference and the external pins VREFP and VREFN. In Zynq UltraScale+ MPSoC SOM, 1.25V external voltage reference is supported.

The PS SYSMON uses 10-bit 1MSPS ADC to digitize the sensor inputs. It is located in the PS LPD and monitors two temperature points & several internal fixed voltage nodes. The PS has two temperature sensors, one is physically located in the PS SYSMON near the RPU. The second, remote sensor is located in the FPD near the APU. The ADC always uses an internally generated voltage reference.

2.4 PMIC with RTC

The Zynq UltraScale+ MPSoC SOM supports Dialog semiconductor DA9063 PMIC. The I2C1 module of Zynq UltraScale+ MPSoC PS is used for PMIC interface through MIO pins with I2C address 0x5A/0x5B.

PMIC's LDO3 and LDO4 are connected to the I/O voltage of PL HD Bank 44 and HD Bank 45, respectively. They are set to 1.2V by default. The voltage of LDO7 is connected to the combined I/O voltages of PL HD Bank 43 and 46. Furthermore, PMIC's LDO6 and LDO9 output are connected to the I/O voltages of PL HP Bank 65 and 66, respectively, which are set to 1V by default. However, the I/O voltage can be configured through software during bootup.

PMIC supports reset output and connected to Zynq UltraScale+ MPSoC PS (PS_POR_B) for power on reset. Also, PMIC supports IRQ output for events indication and connected optionally to MPSoC's PL I/O of HP Bank 66 (C7).

The PMIC supports Real Time Clock functionality. It uses the Coin cell battery power from Board-to-Board Connector 2 pin no. D9 for RTC backup power. The PMIC can support backup battery charging to charge Lithium-Manganese coin cell batteries and super capacitors if required.

Important Note: Every Power Off and On, The DA9063 PMIC work as initial OTP Setting

2.5 Memory

2.5.1 DDR4 SDRAM for PS

The Zynq UltraScale+ MPSoC SOM supports 64bit, 4GB DDR4 RAM memory for MPSoC's PS. Four 16 bit, 1GB DDR4 SDRAM ICs are used to support a total on board RAM memory of 4GB. These DDR4 devices operates at 2400Mbps data rate. DDR4 memory is connected to the hard memory controller of the MPSoC PS. The RAM size can be expandable up to maximum of 8GB based on the availability of higher density 16bit DDR4 device.

Note: Refer **Error! Reference source not found.** *section for exact RAM size used on the SOM based on the Product Part Number.*

2.5.2 DDR4 SDRAM for PL

The Zynq UltraScale+ MPSoC SOM supports 16bit, 2GB DDR4 RAM memory for MPSoC's PL. One 16 bit, 2GB DDR4 SDRAM IC is used to support RAM memory for PL. These DDR4 devices operates up to 2133Mbps data rate. In Zynq UltraScale+ MPSoC SOM, Bank64 is used for PL DDR4 interface. The RAM size can be expandable up to maximum of 4GB based on the availability of higher density 16bit DDR4 device.

The Zynq UltraScale+ MPSoC SOM supports 300MHz differential clock from on board clock synthesizer for PL DDR4 reference clock and connected to Bank64 AD4 & AD5 dedicated clock input pins through AC Coupling capacitors.

Note: Refer **Error! Reference source not found.** *section for exact RAM size used on the SOM based on the Product Part Number.*

2.5.3 eMMC Flash

The Zynq UltraScale+ MPSoC SOM supports 16GB eMMC Flash memory also for Boot & Storage of Zynq UltraScale+ MPSoC PS. This eMMC Flash memory is directly connected to the SD0 controller of the MPSOC's PS through MIO pins and operates at 1.8V Voltage level. This SD/SDIO controller supports eMMC4.51 standard with up to 8bit HS200 mode. The eMMC Flash size can be expandable up to 128GB for storage.

Note: Refer **Error! Reference source not found.** *section for exact eMMC Flash size used on the SOM based on the Product Part N umber.*

2.5.4 EEPROM

The Zynq UltraScale+ MPSoC supports 2Kb EEPROM for storing SOM configuration. The I2C1 module of Zynq UltraScale+ MPSoC PS is used for EEPROM interface through MIO pins with I2C address 0x50, 0x58. This device operates at 1.8 voltage level.

2.5.5 QSPI Flash

The Zynq Ultrascale+ MPSoC SOM supports one on board 256MB QSPI from QSPI controller of MPSoC's PS through MIO pins at 1.8V Voltage level as primary boot device or storage device. The SOM supports 4-bit QSPI Flash with feedback clock functionality.

Note: While using the feedback clock functionality with QSPI Flash, the CAN0 interface of MPSoC's PS cannot be used.

2.6 On SOM Features

2.6.1 Fan Header

The Zynq UltraScale+ MPSoC SOM supports a Fan Header (J1) to connect cooling Fan if required. The Fan Header (J1) is physically located on topside of the SOM as shown below.

Number of Pins	- 2
Connector Part	- 0530480210 from Molex
Mating Connector	- 51021-0200 from Molex
Mating Connector Crimp	- 50058-8000 from Molex
Compatible Fan (Example)	- AFB0505MB from Delta Electronics

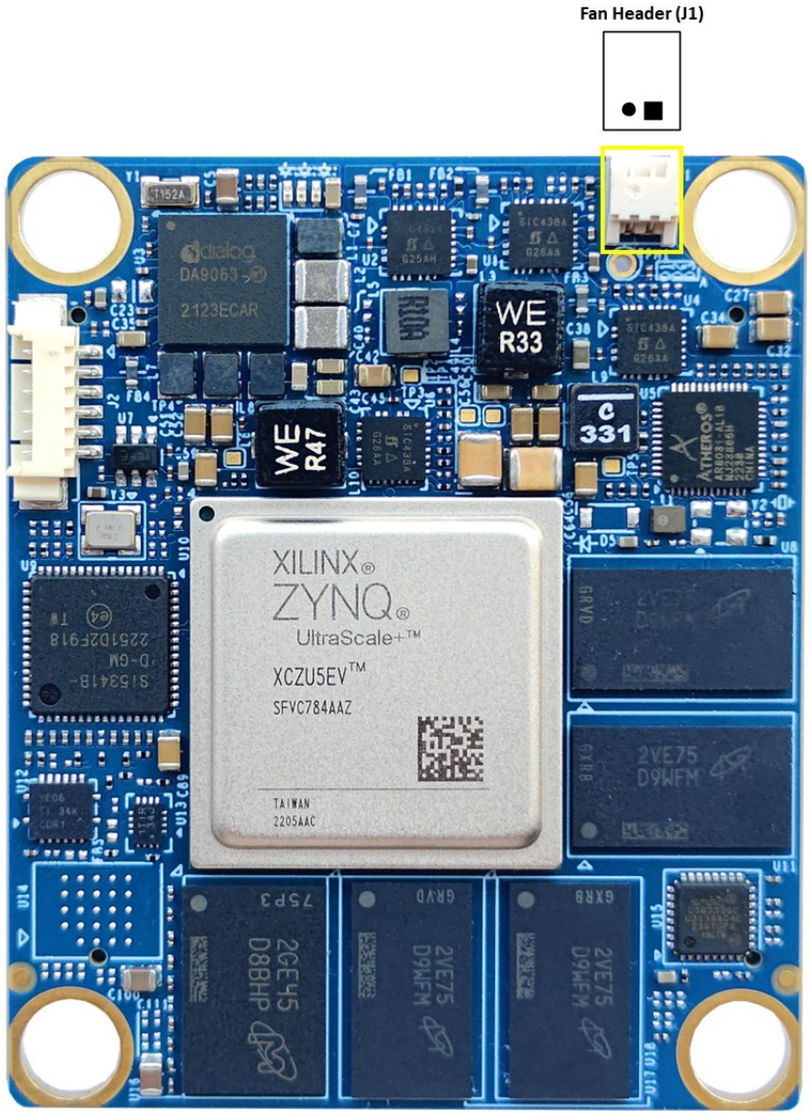

Figure 5: Fan Header

Table 5: Fan Header Pinout

Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
1	VCC_5V	-	-	-	O, 5V Power	Supply Voltage.
2	GND	-	-	-	Power	Ground.

2.6.2 TPM Module

The Zynq UltraScale+ MPSoC SOM supports Trusted Platform Module (TPM) 2.0 Module through SPI Interface of PL. The TPM technology is designed to provide hardware-based, security-related functions. A TPM chip is a secure crypto-processor that is designed to carry out cryptographic operations. This TPM Module operates at 3.3V Voltage level.

2.7 Board-to-Board Connector 1

The Zynq UltraScale+ MPSoC SOM supports two 240-pin high-speed, high-density connectors for interface expansion. The SOM design makes every effort to maximize the interfaces of the Zynq UltraScale+ MPSoC to the carrier board by adding these two board-to-board connectors.

The pinout for Board-to-Board Connector-1 on the Zynq UltraScale+ MPSoC SOM is provided in the table below, and the available interfaces are explained in the following sections. Board-to-Board Connector-1 is located on the bottom side of the SOM, as shown in the diagram below.

Number of Pins	- 240
Connector Part Number	- ADM6-60-01.5-L-4-2-A-TR from Samtech
Mating Connector	- ADF6-60-03.5-L-4-2-A-TR from Samtech
Staking Height	- 5mm

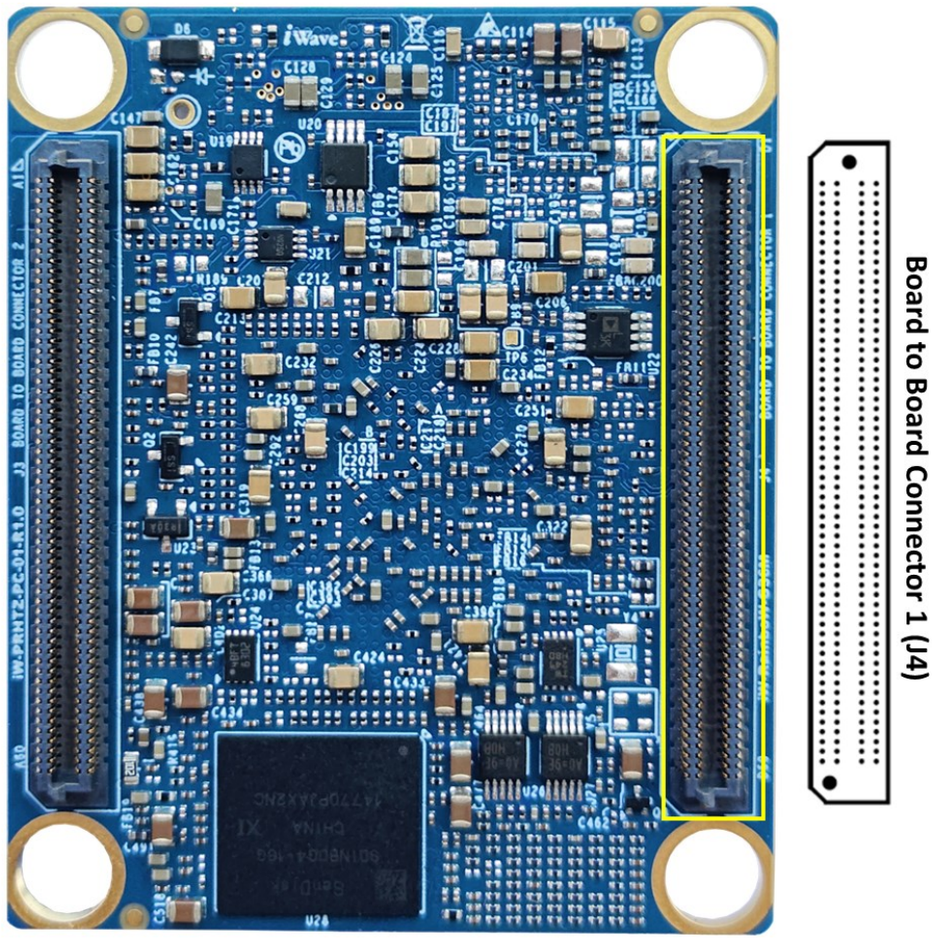

Figure 6: Board-to-Board Connector 1

Table 6: Board-to-Board Connector 1 Pinout

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	NC	**B1**	VCCO_HD44	**C1**	VCCO_HP65	**D1**	VCCO_HP66
A2	PL_B4_LVDS66_L10P_QBC	**B2**	PL_C1_LVDS66_L7P_QBC	**C2**	PL_G3_LVDS66_L4P_DBC	**D2**	PL_G1_LVDS66_L1P_DBC
A3	PL_A4_LVDS66_L10N_QBC	**B3**	PL_B1_LVDS66_L7N_QBC	**C3**	PL_F3_LVDS66_L4N_DBC	**D3**	PL_F1_LVDS66_L1N_DBC
A4	PL_D4_LVDS66_L11P_GC	**B4**	PL_A2_LVDS66_L8P	**C4**	PL_E4_LVDS66_L5P	**D4**	PL_E1_LVDS66_L2P
A5	PL_C4_LVDS66_L11N_GC	**B5**	PL_A1_LVDS66_L8N	**C5**	PL_E3_LVDS66_L5N	**D5**	PL_D1_LVDS66_L2N
A6	PL_C3_LVDS66_L12P_GC	**B6**	PL_B3_LVDS66_L9P	**C6**	PL_G5_LVDS66_L6P	**D6**	PL_F2_LVDS66_L3P
A7	PL_C2_LVDS66_L12N_GC	**B7**	PL_A3_LVDS66_L9N	**C7**	PL_F5_LVDS66_L6N	**D7**	PL_E2_LVDS66_L3N
A8	GND	**B8**	GND	**C8**	GND	**D8**	GND
A9	PL_C8_LVDS66_L22P_DBC	**B9**	PL_B5_LVDS66_L19P_DBC	**C9**	PL_G8_LVDS66_L16P_QBC	**D9**	PL_D7_LVDS66_L13P_GC
A10	PL_B8_LVDS66_L22N_DBC	**B10**	PL_A5_LVDS66_L19N_DBC	**C10**	PL_F7_LVDS66_L16N_QBC	**D10**	PL_D6_LVDS66_L13N_GC
A11	PL_A9_LVDS66_L23P	**B11**	PL_C6_LVDS66_L20P	**C11**	PL_F8_LVDS66_L17P	**D11**	PL_E5_LVDS66_L14P_GC
A12	PL_A8_LVDS66_L23N	**B12**	PL_B6_LVDS66_L20N	**C12**	PL_E8_LVDS66_L17N	**D12**	PL_D5_LVDS66_L14N_GC
A13	PL_C9_LVDS66_L24P	**B13**	PL_A7_LVDS66_L21P	**C13**	PL_E9_LVDS66_L18P	**D13**	PL_G6_LVDS66_L15P
A14	PL_B9_LVDS66_L24N	**B14**	PL_A6_LVDS66_L21N	**C14**	PL_D9_LVDS66_L18N	**D14**	PL_F6_LVDS66_L15N
A15	SYS_SYNC_CLOCKP	**B15**	NC	**C15**	NC	**D15**	NC
A16	SYS_SYNC_CLOCKN	**B16**	NC	**C16**	NC	**D16**	NC
A17	GND	**B17**	GND	**C17**	GND	**D17**	GND
A18	PL_H4_LVDS65_L10P_QBC	**B18**	PL_L1_LVDS65_L7P_QBC	**C18**	PL_R8_LVDS65_L4P_DBC	**D18**	PL_W8_LVDS65_L1P_DBC
A19	PL_H3_LVDS65_L10N_QBC	**B19**	PL_K1_LVDS65_L7N_QBC	**C19**	PL_T8_LVDS65_L4N_DBC	**D19**	PL_Y8_LVDS65_L1N_DBC
A20	PL_K4_LVDS65_L11P_GC	**B20**	PL_J1_LVDS65_L8P	**C20**	PL_R7_LVDS65_L5P	**D20**	PL_U9_LVDS65_L2P
A21	PL_K3_LVDS65_L11N_GC	**B21**	PL_H1_LVDS65_L8N	**C21**	PL_T7_LVDS65_L5N	**D21**	PL_V9_LVDS65_L2N
A22	PL_L3_LVDS65_L12P_GC	**B22**	PL_K2_LVDS65_L9P	**C22**	PL_R6_LVDS65_L6P	**D22**	PL_U8_LVDS65_L3P
A23	PL_L2_LVDS65_L12N_GC	**B23**	PL_J2_LVDS65_L9N	**C23**	PL_T6_LVDS65_L6N	**D23**	PL_V8_LVDS65_L3N
A24	GND	**B24**	GND	**C24**	GND	**D24**	GND
A25	PL_K8_LVDS65_L22P_DBC	**B25**	PL_J5_LVDS65_L19P_DBC	**C25**	PL_P7_LVDS65_L16P_QBC	**D25**	PL_L7_LVDS65_L13P_GC
A26	PL_K7_LVDS65_L22N_DBC	**B26**	PL_J4_LVDS65_L19N_DBC	**C26**	PL_P6_LVDS65_L16N_QBC	**D26**	PL_L6_LVDS65_L13N_GC
A27	PL_K9_LVDS65_L23P_I2C_SCLK	**B27**	PL_J6_LVDS65_L20P	**C27**	PL_N9_LVDS65_L17P	**D27**	PL_M6_LVDS65_L14P_GC
A28	PL_J9_LVDS65_L23N	**B28**	PL_H6_LVDS65_L20N	**C28**	PL_N8_LVDS65_L17N	**D28**	PL_L5_LVDS65_L14N_GC
A29	PL_H9_LVDS65_L24P_PERSTN1_I2C_S	**B29**	PL_J7_LVDS65_L21P	**C29**	PL_M8_LVDS65_L18P	**D29**	PL_N7_LVDS65_L15P
A30	PL_H8_LVDS65_L24N_PERSTN0	**B30**	PL_H7_LVDS65_L21N	**C30**	PL_L8_LVDS65_L18N	**D30**	PL_N6_LVDS65_L15N
A31	SYS_SYNC_CLK_OUTP	**B31**	NC	**C31**	NC	**D31**	NC
A32	SYS_SYNC_CLK_OUTN	**B32**	NC	**C32**	NC	**D32**	NC
A33	GND	**B33**	GND	**C33**	GND	**D33**	GND
A34	PL_Y12_LVDS44_L12P	**B34**	PL_W14_LVDS44_L9P	**C34**	PL_AE13_LVDS44_L4P	**D34**	PL_AE15_LVDS44_L1P
A35	PL_AA12_LVDS44_L12N	**B35**	PL_W13_LVDS44_L9N	**C35**	PL_AF13_LVDS44_L4N	**D35**	PL_AE14_LVDS44_L1N

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A36	PL_AA13_LVDS44_L7P_HDGC	**B36**	PL_Y14_LVDS44_L10P	**C36**	PL_AD15_LVDS44_L5P_HDGC	**D36**	PL_AG14_LVDS44_L2P
A37	PL_AB13_LVDS44_L7N_HDGC	**B37**	PL_Y13_LVDS44_L10N	**C37**	PL_AD14_LVDS44_L5N_HDGC	**D37**	PL_AH14_LVDS44_L2N
A38	PL_AB15_LVDS44_L8P_HDGC	**B38**	PL_W12_LVDS44_L11P	**C38**	PL_AC14_LVDS44_L6P_HDGC	**D38**	PL_AG13_LVDS44_L3P
A39	PL_AB14_LVDS44_L8N_HDGC	**B39**	PL_W11_LVDS44_L11N	**C39**	PL_AC13_LVDS44_L6N_HDGC	**D39**	PL_AH13_LVDS44_L3N
A40	GND	**B40**	GND	**C40**	GND	**D40**	GND
A41	PL_B11_LVDS45_L10P	**B41**	PL_G11_LVDS45_L5P_HDGC	**C41**	PL_K13_LVDS45_L2P	**D41**	PL_E10_LVDS45_L7P_HDGC
A42	PL_A10_LVDS45_L10N	**B42**	PL_F10_LVDS45_L5N_HDGC	**C42**	PL_K12_LVDS45_L2N	**D42**	PL_D10_LVDS45_L7N_HDGC
A43	PL_A12_LVDS45_L11P	**B43**	PL_F12_LVDS45_L6P_HDGC	**C43**	PL_H11_LVDS45_L3P	**D43**	PL_E12_LVDS45_L8P_HDGC
A44	PL_A11_LVDS45_L11N	**B44**	PL_F11_LVDS45_L6N_HDGC	**C44**	PL_G10_LVDS45_L3N	**D44**	PL_D11_LVDS45_L8N_HDGC
A45	PL_D12_LVDS45_L12P	**B45**	PL_C11_LVDS45_L9P	**C45**	PL_J12_LVDS45_L4P	**D45**	PL_J11_LVDS45_L1P
A46	PL_C12_LVDS45_L12N	**B46**	PL_B10_LVDS45_L9N	**C46**	PL_H12_LVDS45_L4N	**D46**	PL_J10_LVDS45_L1N
A47	B2B_1PPS_IN	**B47**	NC	**C47**	NC	**D47**	NC
A48	GND	**B48**	NC	**C48**	NC	**D48**	NC
A49	B2B_PS_MGTREFCLK3P_505	**B49**	GND	**C49**	B2B_PS_MGTREFCLK1P_505	**D49**	GND
A50	B2B_PS_MGTREFCLK3N_505	**B50**	GND	**C50**	B2B_PS_MGTREFCLK1N_505	**D50**	GND
A51	GND	**B51**	B2B_PS_MGTREFCLK2P_505	**C51**	GND	**D51**	B2B_PS_MGTREFCLK0P_505
A52	GND	**B52**	B2B_PS_MGTREFCLK2N_505	**C52**	GND	**D52**	B2B_PS_MGTREFCLK0N_505
A53	PS_MGTRRXP3_505	**B53**	GND	**C53**	PS_MGTRRXP1_505	**D53**	GND
A54	PS_MGTRRXN3_505	**B54**	GND	**C54**	PS_MGTRRXN1_505	**D54**	GND
A55	GND	**B55**	PS_MGTRRXP2_505	**C55**	GND	**D55**	PS_MGTRRXP0_505
A56	GND	**B56**	PS_MGTRRXN2_505	**C56**	GND	**D56**	PS_MGTRRXN0_505
A57	PS_MGTRTXP3_505	**B57**	GND	**C57**	PS_MGTRTXP1_505	**D57**	GND
A58	PS_MGTRTXN3_505	**B58**	GND	**C58**	PS_MGTRTXN1_505	**D58**	GND
A59	GND	**B59**	PS_MGTRTXP2_505	**C59**	GND	**D59**	PS_MGTRTXP0_505
A60	GND	**B60**	PS_MGTRTXN2_505	**C60**	GND	**D60**	PS_MGTRTXN0_505

2.7.1 PS Interfaces

The interfaces which are supported in Board-to-Board Connector 1 from Zynq UltraScale+ MPSoC's PS is explained in the following section.

2.7.1.1 PS-GTR Transceivers

The Zynq UltraScale+ MPSoC supports four Multi-Gigabit PS-GTR transceivers with data rate from 1.25Gbps to 6.0Gbps. This PS-GTR transceiver lanes provide I/O path for MPSoC MAC controllers and their link partner outside. At any given time, these four lanes can be used for any of below mentioned peripheral standards.

- x1, x2, or x4 lane of PCIe at Gen1 (2.5Gb/s) or Gen2 (5.0Gb/s) rates
- 1 or 2 lanes of DisplayPort (TX only) at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s
- 1 or 2 SATA channels at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s
- 1 or 2 USB3.0 channels at 5.0Gb/s
- 1-4 Ethernet SGMII channels at 1.25Gb/s

The available peripheral standard option for each PS-GTR transceiver lane in Zynq UltraScale+ MPSoC is shown below. This is user programmable via the high-speed I/O multiplexer (HS-MIO) of MPSoC.

PS Peripheral Interface	Lane0	Lane1	Lane2	Lane3
PCIe (x1, x2 or x4)	PCIe0	PCIe1	PCIe2	PCIe3
SATA (1 or 2 channels)	SATA0	SATA1	SATA0	SATA1
DisplayPort (TX only)	DP1	DP0	DP1	DP0
USB0	USB0	USB0	USB0	-
USB1	-	-	-	USB1
SGMII0	SGMII0	-	-	-
SGMII1	-	SGMII1	-	-
SGMII2	-	-	SGMII2	-
SGMII3	-	-	-	SGMII3

The Zynq UltraScale+ MPSoC SOM supports four PS GTR transceivers from Board-to-Board Connector 1. Each PS GTR transceiver lane supports one dedicated reference clock input pair with the ability to share reference clocks between lanes from Board-to-Board Connector 1.

In the Zynq UltraScale+ MPSoC SOM, while the on-SOM clock synthesizer provides a reference clock to the three PS-GTR lanes, there is also an option for the end user to source reference clocks to the PS-GTR lanes through Board-to-Board Connector 1. This allows the user to select the required peripheral standards for the PS-GTR lanes.

Note: Please contact iWave for PS GTR Reference clock changes.

For more details on PS-GTR transceiver pinouts on Board-to-Board Connector 1, refer the below table.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
PS GTR Lane0 Pins						
D59	PS_MGTRTXP0_505	PS_MGTRTXP0_505	505	E25	O, DIFF	PS-GTR Lane0 High speed differential transmitter positive.
D60	PS_MGTRTXN0_505	PS_MGTRTXN0_505	505	E26	O, DIFF	PS-GTR Lane0 High speed differential transmitter negative.
D55	PS_MGTRRXP0_505	PS_MGTRRXP0_505	505	F27	I, DIFF	PS-GTR Lane0 High speed differential receiver positive.
D56	PS_MGTRRXN0_505	PS_MGTRRXN0_505	505	F28	I, DIFF	PS-GTR Lane0 High speed differential receiver negative.
D51	PS_MGTREFCLK0P_505	PS_MGTREFCLK0P_505	505	F23	I, DIFF	PS-GTR Lane0 High speed differential reference clock positive.
D52	PS_MGTREFCLK0N_505	PS_MGTREFCLK0N_505	505	F24	I, DIFF	PS-GTR Lane0 High speed differential reference clock negative.
PS GTR Lane1 Pins						
C57	PS_MGTRTXP1_505	PS_MGTRTXP1_505	505	D23	O, DIFF	PS-GTR Lane1 High speed differential transmitter positive.
C58	PS_MGTRTXN1_505	PS_MGTRTXN1_505	505	D24	O, DIFF	PS-GTR Lane1 High speed differential transmitter negative.
C53	PS_MGTRRXP1_505	PS_MGTRRXP1_505	505	D27	I, DIFF	PS-GTR Lane1 High speed differential receiver positive.
C54	PS_MGTRRXN1_505	PS_MGTRRXN1_505	505	D28	I, DIFF	PS-GTR Lane1 High speed differential receiver negative.
C49	B2B_PS_MGTREFCLK1P_505	PS_MGTREFCLK1P_505	505	E21	I, DIFF	No Connect. Optionally connected to PS-GTR Lane1 High speed differential reference clock positive.
C50	B2B_PS_MGTREFCLK1N_505	PS_MGTREFCLK1N_505	505	E22	I, DIFF	No Connect. Optionally connected to PS-GTR Lane1 High speed differential reference clock negative.
PS GTR Lane2 Pins						
B59	PS_MGTRTXP2_505	PS_MGTRTXP2_505	505	C25	O, DIFF	PS-GTR Lane2 High speed differential transmitter positive.
B60	PS_MGTRTXN2_505	PS_MGTRTXN2_505	505	C26	O, DIFF	PS-GTR Lane2 High speed differential transmitter negative.
B55	PS_MGTRRXP2_505	PS_MGTRRXP2_505	505	B27	I, DIFF	PS-GTR Lane2 High speed differential receiver positive.
B56	PS_MGTRRXN2_505	PS_MGTRRXN2_505	505	B28	I, DIFF	PS-GTR Lane2 High speed differential receiver negative.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
B51	B2B_PS_MGTREFCLK2P_505	PS_MGTREFCLK2P_505	505	C21	I, DIFF	No Connect. Optionally connected to PS-GTR Lane2 High speed differential reference clock positive.
B52	B2B_PS_MGTREFCLK2N_505	PS_MGTREFCLK2N_505	505	C22	I, DIFF	No Connect. Optionally connected to PS-GTR Lane2 High speed differential reference clock negative.
PS GTR Lane3 Pins						
A57	PS_MGTRTXP3_505	PS_MGTRTXP3_505	505	B23	O, DIFF	PS-GTR Lane3 High speed differential transmitter positive.
A58	PS_MGTRTXN3_505	PS_MGTRTXN3_505	505	B24	O, DIFF	PS-GTR Lane3 High speed differential transmitter negative.
A53	PS_MGTRRXP3_505	PS_MGTRRXP3_505	505	A25	I, DIFF	PS-GTR Lane3 High speed differential receiver positive.
A54	PS_MGTRRXN3_505	PS_MGTRRXN3_505	505	A26	I, DIFF	PS-GTR Lane3 High speed differential receiver negative.
A49	B2B_PS_MGTREFCLK3P_505	PS_MGTREFCLK3P_505	505	A21	I, DIFF	No Connect. Optionally connected to PS-GTR Lane3 High speed differential reference clock positive.
A50	B2B_PS_MGTREFCLK3N_505	PS_MGTREFCLK3N_505	505	A22	I, DIFF	No Connect. Optionally connected to PS-GTR Lane3 High speed differential reference clock negative.

2.7.2 PL Interfaces

The interfaces which are supported in Board-to-Board Connector 1 from Zynq UltraScale+ MPSoC's PL is explained in the following section.

2.7.2.1 PL IOs – HP BANK66

The Zynq UltraScale+ MPSoC SOM supports 24 LVDS IOs/48 Single Ended (SE) IOs on Board-to-Board Connector-1 from MPSoC's PL High Performance (HP) Bank66. Upon these 24 LVDS IOs/48 SE IOs, upto 4 GC Global Clock Inputs and upto 16 PLSYSMON auxiliary differential analog inputs are available.

The IO voltage of PL Bank66 is connected from LDO9 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1V to 1.8V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO9 to output appropriate IO voltage for PL Bank66. By default, IO voltage of PL Bank66 is set as 1V and after U-boot bootup configurable up to 1.8V. For more details about supported IO standard, refer the Zynq UltraScale+ MPSoC datasheet.

In the Zynq UltraScale+ MPSoC SOM, PL Bank66 signals are routed as LVDS IOs to Board-to-Board Connector-1. Even though PL Bank66 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector-1 pins A4, A5, A6, A7, D9, D10, D11 and D12 are GC Global Clock Input capable pins of PL Bank66. Also, Board-to-Board Connector 1 pins A2, A3, A9, A10, B2, B3, B4, B5, B6, B7, B9, B10, B11, B12, B13, B14, C2, C3, C4, C5, C6, C7, C9, C10, C11, C12, C13, C14, D6, D7, D13 and D14 are PLSYSMON auxiliary analog Input capable pins of PL Bank66.

For more details on PL HP Bank66 pinouts on Board-to-Board Connector 1, refer the below table.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
A2	PL_B4_LVDS66_L10P_QBC	IO_L10P_T1U_N6_QBC_AD4P_66	HP Bank 66	B4	IO, 1.8V	PL Bank66 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input4 positive or Single ended I/O.
A3	PL_A4_LVDS66_L10N_QBC	IO_L10N_T1U_N7_QBC_AD4N_66	HP Bank 66	A4	IO, 1.8V	PL Bank66 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input4 negative or Single ended I/O.
A4	PL_D4_LVDS66_L11P_GC	IO_L11P_T1U_N8_GC_66	HP Bank 66	D4	IO, 1.8V	PL Bank66 IO11 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
A5	PL_C4_LVDS66_L11N_GC	IO_L11N_T1U_N9_GC_66	HP Bank 66	C4	IO, 1.8V	PL Bank66 IO11 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
A6	PL_C3_LVDS66_L12P_GC	IO_L12P_T1U_N10_GC_66	HP Bank 66	C3	IO, 1.8V	PL Bank66 IO12 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
A7	PL_C2_LVDS66_L12N_GC	IO_L12N_T1U_N11_GC_66	HP Bank 66	C2	IO, 1.8V	PL Bank66 IO12 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
A9	PL_C8_LVDS66_L22P_DBC	IO_L22P_T3U_N6_DBC_AD0P_66	HP Bank 66	C8	IO, 1.8V	PL Bank66 IO22 differential positive. Same pin can be configured as PLSYSMON differential analog input0 positive or Single ended I/O.
A10	PL_B8_LVDS66_L22N_DBC	IO_L22N_T3U_N7_DBC_AD0N_66	HP Bank 66	B8	IO, 1.8V	PL Bank66 IO22 differential negative. Same pin can be configured as PLSYSMON differential analog input0 negative or Single ended I/O.
A11	PL_A9_LVDS66_L23P	IO_L23P_T3U_N8_66	HP Bank 66	A9	IO, 1.8V	PL Bank66 IO23 differential positive. Same pin can be configured as Single ended I/O.
A12	PL_A8_LVDS66_L23N	IO_L23N_T3U_N9_66	HP Bank 66	A8	IO, 1.8V	PL Bank66 IO23 differential negative. Same pin can be configured as Single ended I/O. *This pin is not available for ZU3T Device configuration*
A13	PL_C9_LVDS66_L24P	IO_L24P_T3U_N10_66	HP Bank 66	C9	IO, 1.8V	PL Bank66 IO24 differential positive. Same pin can be configured as Single ended I/O.
A14	PL_B9_LVDS66_L24N	IO_L24N_T3U_N11_66	HP Bank 66	B9	IO, 1.8V	PL Bank66 IO24 differential negative. Same pin can be configured as Single ended I/O.
B2	PL_C1_LVDS66_L7P_QBC	IO_L7P_T1L_N0_QBC_AD13P_66	HP Bank 66	C1	IO, 1.8V	PL Bank66 IO7 differential positive. Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.
B3	PL_B1_LVDS66_L7N_QBC	IO_L7N_T1L_N1_QBC_AD13N_66	HP Bank 66	B1	IO, 1.8V	PL Bank66 IO7 differential negative. Same pin can be configured as PLSYSMON differential analog input13 negative or Single ended I/O.
B4	PL_A2_LVDS66_L8P	IO_L8P_T1L_N2_AD5P_66	HP Bank 66	A2	IO, 1.8V	PL Bank66 IO8 differential positive. Same pin can be configured as PLSYSMON differential analog input5 positive or Single ended I/O.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
B5	PL_A1_LVDS66_L8N	IO_L8N_T1L_N3_AD5N_66	HP Bank 66	A1	IO, 1.8V	PL Bank66 IO8 differential negative. Same pin can be configured as PLSYSMON differential analog input5 negative or Single ended I/O.
B6	PL_B3_LVDS66_L9P	IO_L9P_T1L_N4_AD12P_66	HP Bank 66	B3	IO, 1.8V	PL Bank66 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input12 positive or Single ended I/O.
B7	PL_A3_LVDS66_L9N	IO_L9N_T1L_N5_AD12N_66	HP Bank 66	A3	IO, 1.8V	PL Bank66 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input12 negative or Single ended I/O.
B9	PL_B5_LVDS66_L19P_DBC	IO_L19P_T3L_N0_DBC_AD9P_66	HP Bank 66	B5	IO, 1.8V	PL Bank66 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
B10	PL_A5_LVDS66_L19N_DBC	IO_L19N_T3L_N1_DBC_AD9N_66	HP Bank 66	A5	IO, 1.8V	PL Bank66 IO19 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
B11	PL_C6_LVDS66_L20P	IO_L20P_T3L_N2_AD1P_66	HP Bank 66	C6	IO, 1.8V	PL Bank66 IO20 differential positive. Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.
B12	PL_B6_LVDS66_L20N	IO_L20N_T3L_N3_AD1N_66	HP Bank 66	B6	IO, 1.8V	PL Bank66 IO20 differential negative. Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.
B13	PL_A7_LVDS66_L21P	IO_L21P_T3L_N4_AD8P_66	HP Bank 66	A7	IO, 1.8V	PL Bank66 IO21 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
B14	PL_A6_LVDS66_L21N	IO_L21N_T3L_N5_AD8N_66	HP Bank 66	A6	IO, 1.8V	PL Bank66 IO21 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
C2	PL_G3_LVDS66_L4P_DBC	IO_L4P_T0U_N6_DBC_AD7P_66	HP Bank 66	G3	IO, 1.8V	PL Bank66 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input7 positive or Single ended I/O.
C3	PL_F3_LVDS66_L4N_DBC	IO_L4N_T0U_N7_DBC_AD7N_66	HP Bank 66	F3	IO, 1.8V	PL Bank66 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input7 negative or Single ended I/O.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
C4	PL_E4_LVDS66_L5P	IO_L5P_T0U_N8_AD14P_66	HP Bank 66	E4	IO, 1.8V	PL Bank66 IO5 differential positive. Same pin can be configured as PLSYSMON differential analog input14 positive or Single ended I/O.
C5	PL_E3_LVDS66_L5N	IO_L5N_T0U_N9_AD14N_66	HP Bank 66	E3	IO, 1.8V	PL Bank66 IO5 differential negative. Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.
C6	PL_G5_LVDS66_L6P	IO_L6P_T0U_N10_AD6P_66	HP Bank 66	G5	IO, 1.8V	PL Bank66 IO6 differential positive. Same pin can be configured as PLSYSMON differential analog input6 positive or Single ended I/O.
C7	PL_F5_LVDS66_L6N	IO_L6N_T0U_N11_AD6N_66	HP Bank 66	F5	IO, 1.8V	PL Bank66 IO6 differential negative. Same pin can be configured as PLSYSMON differential analog input6 negative or Single ended I/O.
C9	PL_G8_LVDS66_L16P_QBC	IO_L16P_T2U_N6_QBC_AD3P_66	HP Bank 66	G8	IO, 1.8V	PL Bank66 IO16 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
C10	PL_F7_LVDS66_L16N_QBC	IO_L16N_T2U_N7_QBC_AD3N_66	HP Bank 66	F7	IO, 1.8V	PL Bank66 IO16 differential negative. Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.
C11	PL_F8_LVDS66_L17P	IO_L17P_T2U_N8_AD10P_66	HP Bank 66	F8	IO, 1.8V	PL Bank66 IO17 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
C12	PL_E8_LVDS66_L17N	IO_L17N_T2U_N9_AD10N_66	HP Bank 66	E8	IO, 1.8V	PL Bank66 IO17 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
C13	PL_E9_LVDS66_L18P	IO_L18P_T2U_N10_AD2P_66	HP Bank 66	E9	IO, 1.8V	PL Bank66 IO18 differential positive. Same pin can be configured as PLSYSMON differential analog input2 positive or Single ended I/O.
C14	PL_D9_LVDS66_L18N	IO_L18N_T2U_N11_AD2N_66	HP Bank 66	D9	IO, 1.8V	PL Bank66 IO18 differential negative. Same pin can be configured as PLSYSMON differential analog input2 negative or Single ended I/O.
D2	PL_G1_LVDS66_L1P_DBC	IO_L1P_T0L_N0_DBC_66	HP Bank 66	G1	IO, 1.8V	PL Bank66 IO1 differential positive. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
D3	PL_F1_LVDS66_L1N_DBC	IO_L1N_T0L_N1_DBC_66	HP Bank 66	F1	IO, 1.8V	PL Bank66 IO1 differential negative. Same pin can be configured as Single ended I/O.
D4	PL_E1_LVDS66_L2P	IO_L2P_T0L_N2_66	HP Bank 66	E1	IO, 1.8V	PL Bank66 IO2 differential positive. Same pin can be configured as Single ended I/O.
D5	PL_D1_LVDS66_L2N	IO_L2N_T0L_N3_66	HP Bank 66	D1	IO, 1.8V	PL Bank66 IO2 differential negative. Same pin can be configured as Single ended I/O.
D6	PL_F2_LVDS66_L3P	IO_L3P_T0L_N4_AD15P_66	HP Bank 66	F2	IO, 1.8V	PL Bank66 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input15 positive or Single ended I/O.
D7	PL_E2_LVDS66_L3N	IO_L3N_T0L_N5_AD15N_66	HP Bank 66	E2	IO, 1.8V	PL Bank66 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O.
D9	PL_D7_LVDS66_L13P_GC	IO_L13P_T2L_N0_GC_QBC_66	HP Bank 66	D7	IO, 1.8V	PL Bank66 IO13 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
D10	PL_D6_LVDS66_L13N_GC	IO_L13N_T2L_N1_GC_QBC_66	HP Bank 66	D6	IO, 1.8V	PL Bank66 IO13 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
D11	PL_E5_LVDS66_L14P_GC	IO_L14P_T2L_N2_GC_66	HP Bank 66	E5	IO, 1.8V	PL Bank66 IO14 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
D12	PL_D5_LVDS66_L14N_GC	IO_L14N_T2L_N3_GC_66	HP Bank 66	D5	IO, 1.8V	PL Bank66 IO14 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
D13	PL_G6_LVDS66_L15P	IO_L15P_T2L_N4_AD11P_66	HP Bank 66	G6	IO, 1.8V	PL Bank66 IO15 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
D14	PL_F6_LVDS66_L15N	IO_L15N_T2L_N5_AD11N_66	HP Bank 66	F6	IO, 1.8V	PL Bank66 IO15 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.

**IO Type of IOs originating from ZU5/4/3T/3/2/1 MPSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU5/4/3T/3/2/1 MPSoC datasheet.*

2.7.2.2 PL IOs – HP BANK65

The Zynq UltraScale+ MPSoC SOM supports 24 LVDS IOs/48 Single Ended (SE) IOs on Board-to-Board Connector-1 from MPSoC's PL High Performance (HP) Bank65. Upon these 24 LVDS IOs/48 SE IOs, upto 4 GC Global Clock Inputs and upto 18 PLSYSMON auxiliary differential analog inputs are available.

The IO voltage of PL Bank65 is connected from LDO6 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1V to 1.8V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO6 to output appropriate IO voltage for PL Bank65. By default, IO voltage of PL Bank65 is set as 1V and after U-boot bootup configurable up to 1.8V. For more details about supported IO standard, refer the Zynq UltraScale+ MPSoC datasheet.

In the Zynq UltraScale+ MPSoC SOM, PL Bank65 signals are routed as LVDS IOs to Board-to-Board Connector-1. Even though PL Bank65 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector-1 pins A20, A21, A22, A23, D25, D26, D27 and D28 are GC Global Clock Input capable pins of PL Bank66. Also, Board-to-Board Connector 1 pins A18, A19, A25, A26, B18, B19, B20, B21, B22, B23, B25, B26, B27, B28, B29, B30, C18, C19, C20, C21, C22, C23, C25, C26, C27, C28, C29, C30, D22, D23, D29 and D30 are PLSYSMON auxiliary analog Input capable pins of PL Bank65.

For more details on PL HP Bank65 pinouts on Board-to-Board Connector 1, refer the below table.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
A18	PL_H4_LVDS65_L10P_QBC	IO_L10P_T1U_N6_QBC_AD4P_65	HP Bank 65	H4	IO, 1.8V	PL Bank65 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input4 positive or Single ended I/O.
A19	PL_H3_LVDS65_L10N_QBC	IO_L10N_T1U_N7_QBC_AD4N_65	HP Bank 65	H3	IO, 1.8V	PL Bank65 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input4 negative or Single ended I/O.
A20	PL_K4_LVDS65_L11P_GC	IO_L11P_T1U_N8_GC_65	HP Bank 65	K4	IO, 1.8V	PL Bank65 IO11 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
A21	PL_K3_LVDS65_L11N_GC	IO_L11N_T1U_N9_GC_65	HP Bank 65	K3	IO, 1.8V	PL Bank65 IO11 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
A22	PL_L3_LVDS65_L12P_GC	IO_L12P_T1U_N10_GC_65	HP Bank 65	L3	IO, 1.8V	PL Bank65 IO12 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
A23	PL_L2_LVDS65_L12N_GC	IO_L12N_T1U_N11_GC_65	HP Bank 65	L2	IO, 1.8V	PL Bank65 IO12 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
A25	PL_K8_LVDS65_L22P_DBC	IO_L22P_T3U_N6_DBC_AD0P_65	HP Bank 65	K8	IO, 1.8V	PL Bank65 IO22 differential positive. Same pin can be configured as PLSYSMON differential analog input0 positive or Single ended I/O.
A26	PL_K7_LVDS65_L22N_DBC	IO_L22N_T3U_N7_DBC_AD0N_65	HP Bank 65	K7	IO, 1.8V	PL Bank65 IO22 differential negative. Same pin can be configured as PLSYSMON differential analog input0 negative or Single ended I/O.
A27	PL_K9_LVDS65_L23P_I2C_SCLK	IO_L23P_T3U_N8_I2C_SCLK_65	HP Bank 65	K9	IO, 1.8V	PL Bank65 IO23 differential positive. Same pin can be configured as PL I2C Clock Output or Single ended I/O.
A28	PL_J9_LVDS65_L23N	IO_L23N_T3U_N9_65	HP Bank 65	J9	IO, 1.8V	PL Bank65 IO23 differential negative. Same pin can be configured as Single ended I/O.
A29	PL_H9_LVDS65_L24P_PERSTN1_I2C_S	IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65	HP Bank 65	H9	IO, 1.8V	PL Bank65 IO24 differential positive. Same pin can be configured as PL I2C Data Pin, PCIe Reset or Single ended I/O.
A30	PL_H8_LVDS65_L24N_PERSTN0	IO_L24N_T3U_N11_PERSTN0_65	HP Bank 65	H8	IO, 1.8V	PL Bank65 IO24 differential negative. Same pin can be configured as PCIe Reset or Single ended I/O. *This pin is only available for ZU3/2/1 MPSoC Device Configurations.*
B18	PL_L1_LVDS65_L7P_QBC	IO_L7P_T1L_N0_QBC_AD13P_65	HP Bank 65	L1	IO, 1.8V	PL Bank65 IO7 differential positive. Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.
B19	PL_K1_LVDS65_L7N_QBC	IO_L7N_T1L_N1_QBC_AD13N_65	HP Bank 65	K1	IO, 1.8V	PL Bank65 IO7 differential negative. Same pin can be configured as PLSYSMON differential analog input13 negative or Single ended I/O.
B20	PL_J1_LVDS65_L8P	IO_L8P_T1L_N2_AD5P_65	HP Bank 65	J1	IO, 1.8V	PL Bank65 IO8 differential positive. Same pin can be configured as PLSYSMON differential analog input5 positive or Single ended I/O.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
B21	PL_H1_LVDS65_L8N	IO_L8N_T1L_N3_AD5N_65	HP Bank 65	H1	IO, 1.8V	PL Bank65 IO8 differential negative. Same pin can be configured as PLSYSMON differential analog input5 negative or Single ended I/O.
B22	PL_K2_LVDS65_L9P	IO_L9P_T1L_N4_AD12P_65	HP Bank 65	K2	IO, 1.8V	PL Bank65 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input12 positive or Single ended I/O.
B23	PL_J2_LVDS65_L9N	IO_L9N_T1L_N5_AD12N_65	HP Bank 65	J2	IO, 1.8V	PL Bank65 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input12 negative or Single ended I/O.
B25	PL_J5_LVDS65_L19P_DBC	IO_L19P_T3L_N0_DBC_AD9P_65	HP Bank 65	J5	IO, 1.8V	PL Bank65 IO19 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
B26	PL_J4_LVDS65_L19N_DBC	IO_L19N_T3L_N1_DBC_AD9N_65	HP Bank 65	J4	IO, 1.8V	PL Bank65 IO19 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
B27	PL_J6_LVDS65_L20P	IO_L20P_T3L_N2_AD1P_65	HP Bank 65	J6	IO, 1.8V	PL Bank65 IO20 differential positive. Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.
B28	PL_H6_LVDS65_L20N	IO_L20N_T3L_N3_AD1N_65	HP Bank 65	H6	IO, 1.8V	PL Bank65 IO20 differential negative. Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.
B29	PL_J7_LVDS65_L21P	IO_L21P_T3L_N4_AD8P_65	HP Bank 65	J7	IO, 1.8V	PL Bank65 IO21 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
B30	PL_H7_LVDS65_L21N	IO_L21N_T3L_N5_AD8N_65	HP Bank 65	H7	IO, 1.8V	PL Bank65 IO21 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
C18	PL_R8_LVDS65_L4P_DBC	IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65	HP Bank 65	R8	IO, 1.8V	PL Bank65 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input7 positive, PMBus alert, interrupt signal or Single ended I/O.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
C19	PL_T8_LVDS65_L4N_DBC	IO_L4N_T0U_N7_DBC_AD7N_65	HP Bank 65	T8	IO, 1.8V	PL Bank65 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input7 negative or Single ended I/O.
C20	PL_R7_LVDS65_L5P	IO_L5P_T0U_N8_AD14P_65	HP Bank 65	R7	IO, 1.8V	PL Bank65 IO5 differential positive. Same pin can be configured as PLSYSMON differential analog input14 positive or Single ended I/O.
C21	PL_T7_LVDS65_L5N	IO_L5N_T0U_N9_AD14N_65	HP Bank 65	T7	IO, 1.8V	PL Bank65 IO5 differential negative. Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.
C22	PL_R6_LVDS65_L6P	IO_L6P_T0U_N10_AD6P_65	HP Bank 65	R6	IO, 1.8V	PL Bank65 IO6 differential positive. Same pin can be configured as PLSYSMON differential analog input6 positive or Single ended I/O.
C23	PL_T6_LVDS65_L6N	IO_L6N_T0U_N11_AD6N_65	HP Bank 65	T6	IO, 1.8V	PL Bank65 IO6 differential negative. Same pin can be configured as PLSYSMON differential analog input6 negative or Single ended I/O.
C25	PL_P7_LVDS65_L16P_QBC	IO_L16P_T2U_N6_QBC_AD3P_65	HP Bank 65	P7	IO, 1.8V	PL Bank65 IO16 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
C26	PL_P6_LVDS65_L16N_QBC	IO_L16N_T2U_N7_QBC_AD3N_65	HP Bank 65	P6	IO, 1.8V	PL Bank65 IO16 differential negative. Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.
C27	PL_N9_LVDS65_L17P	IO_L17P_T2U_N8_AD10P_65	HP Bank 65	N9	IO, 1.8V	PL Bank65 IO17 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
C28	PL_N8_LVDS65_L17N	IO_L17N_T2U_N9_AD10N_65	HP Bank 65	N8	IO, 1.8V	PL Bank65 IO17 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
C29	PL_M8_LVDS65_L18P	IO_L18P_T2U_N10_AD2P_65	HP Bank 65	M8	IO, 1.8V	PL Bank65 IO18 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
C30	PL_L8_LVDS65_L18N	IO_L18N_T2U_N11_AD2N_65	HP Bank 65	L8	IO, 1.8V	PL Bank65 IO18 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
D18	PL_W8_LVDS65_L1P_DBC	IO_L1P_T0L_N0_DBC_65	HP Bank 65	W8	IO, 1.8V	PL Bank65 IO1 differential positive. Same pin can be configured as Single ended I/O.
D19	PL_Y8_LVDS65_L1N_DBC	IO_L1N_T0L_N1_DBC_65	HP Bank 65	Y8	IO, 1.8V	PL Bank65 IO1 differential negative. Same pin can be configured as Single ended I/O.
D20	PL_U9_LVDS65_L2P	IO_L2P_T0L_N2_65	HP Bank 65	U9	IO, 1.8V	PL Bank65 IO2 differential positive. Same pin can be configured as Single ended I/O.
D21	PL_V9_LVDS65_L2N	IO_L2N_T0L_N3_65	HP Bank 65	V9	IO, 1.8V	PL Bank65 IO2 differential negative. Same pin can be configured as Single ended I/O.
D22	PL_U8_LVDS65_L3P	IO_L3P_T0L_N4_AD15P_65	HP Bank 65	U8	IO, 1.8V	PL Bank65 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input15 positive or Single ended I/O.
D23	PL_V8_LVDS65_L3N	IO_L3N_T0L_N5_AD15N_65	HP Bank 65	V8	IO, 1.8V	PL Bank65 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O.
D25	PL_L7_LVDS65_L13P_GC	IO_L13P_T2L_N0_GC_QBC_65	HP Bank 65	L7	IO, 1.8V	PL Bank65 IO13 differential positive. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
D26	PL_L6_LVDS65_L13N_GC	IO_L13N_T2L_N1_GC_QBC_65	HP Bank 65	L6	IO, 1.8V	PL Bank65 IO13 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
D27	PL_M6_LVDS65_L14P_GC	IO_L14P_T2L_N2_GC_65	HP Bank 65	M6	IO, 1.8V	PL Bank65 IO14 differential positive. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
D28	PL_L5_LVDS65_L14N_GC	IO_L14N_T2L_N3_GC_65	HP Bank 65	L5	IO, 1.8V	PL Bank65 IO14 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
D29	PL_N7_LVDS65_L15P	IO_L15P_T2L_N4_AD11P_65	HP Bank 65	N7	IO, 1.8V	PL Bank65 IO15 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
D30	PL_N6_LVDS65_L15N	IO_L15N_T2L_N5_AD11N_65	HP Bank 65	N6	IO, 1.8V	PL Bank65 IO15 differential negative. Same pin can be configured as PLSYSMON differential analog

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
						input11 negative or Single ended I/O.

**IO Type of IOs originating from ZU5/4/3T/3/2/1 MPSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU5/4/3T/3/2/1 MPSoC datasheet.*

2.7.2.3 PL IOs – HD BANK44

The Zynq UltraScale+ MPSoC SOM supports 24 Single Ended (SE) IOs on Board-to-Board Connector 1 from MPSoC's PL High-Density (HD) Bank44. Upon these 22 Single Ended IOs, upto 4 HDGC Global Clock Inputs and upto 16 PLSYSMON auxiliary analog inputs are available.

The IO voltage of PL Bank44 is connected from LDO3 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.2V to 3.3V through software. While using as DIFF IOs or Single Ended IOs, make sure to set the PMIC LDO3 to output appropriate IO voltage for PL Bank44. By default, IO voltage of PL Bank44 is set as 1.2V and after U-boot bootup configurable upto 3.3V. For more details about supported IO standard, refer the Zynq UltraScale+ MPSoC datasheet.

In the Zynq UltraScale+ MPSoC SOM, PL Bank44 signals are routed as differential IOs to Board-to-Board Connector 1, these pins can be used as DIFF IOs if required. The Board-to-Board Connector 1 pins A36, A37, A38, A39, C36, C37, C38 and C39 are HDGC Global Clock Input capable pins of PL Bank44. Also, Board-to-Board Connector 1 pins A34, A35, B34, B35, B36, B37, B38, B39, C34, C35, D34, D35, D36, D37, D38 and D39 are PLSYSMON auxiliary analog Input capable pins of PL Bank44.

For more details on PL HD Bank44 pinouts on Board-to-Board Connector 1, refer the below table.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
A34	PL_Y12_LVDS44_L12P	IO_L12P_AD8P_44	HD Bank 44	Y12	IO, 1.8V	PL Bank44 IO12 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
A35	PL_AA12_LVDS44_L12N	IO_L12N_AD8N_44	HD Bank 44	AA12	IO, 1.8V	PL Bank44 IO12 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
A36	PL_AA13_LVDS44_L7P_HDGC	IO_L7P_HDGC_44	HD Bank 44	AA13	IO, 1.8V	PL Bank44 IO7 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.
A37	PL_AB13_LVDS44_L7N_HDGC	IO_L7N_HDGC_44	HD Bank 44	AB13	IO, 1.8V	PL Bank44 IO7 differential negative. Same pin can be configured as HDGC

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
						Global Clock Input differential negative or Single ended I/O.
A38	PL_AB15_LVDS44_L8P_HDGC	IO_L8P_HDGC_44	HD Bank 44	AB15	IO, 1.8V	PL Bank44 IO8 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.
A39	PL_AB14_LVDS44_L8N_HDGC	IO_L8N_HDGC_44	HD Bank 44	AB14	IO, 1.8V	PL Bank44 IO8 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
B34	PL_W14_LVDS44_L9P	IO_L9P_AD11P_44	HD Bank 44	W14	IO, 1.8V	PL Bank44 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
B35	PL_W13_LVDS44_L9N	IO_L9N_AD11N_44	HD Bank 44	W13	IO, 1.8V	PL Bank44 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
B36	PL_Y14_LVDS44_L10P	IO_L10P_AD10P_44	HD Bank 44	Y14	IO, 1.8V	PL Bank44 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
B37	PL_Y13_LVDS44_L10N	IO_L10N_AD10N_44	HD Bank 44	Y13	IO, 1.8V	PL Bank44 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
B38	PL_W12_LVDS44_L11P	IO_L11P_AD9P_44	HD Bank 44	W12	IO, 1.8V	PL Bank44 IO11 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
B39	PL_W11_LVDS44_L11N	IO_L11N_AD9N_44	HD Bank 44	W11	IO, 1.8V	PL Bank44 IO11 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
C34	PL_AE13_LVDS44_L4P	IO_L4P_AD12P_44	HD Bank 44	AE13	IO, 1.8V	PL Bank44 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input12 positive or Single ended I/O.
C35	PL_AF13_LVDS44_L4N	IO_L4N_AD12N_44	HD Bank 44	AF13	IO, 1.8V	PL Bank44 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input12 negative or Single ended I/O.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
C36	PL_AD15_LVDS44_L5P_HDGC	IO_L5P_HDGC_44	HD Bank 44	AD15	IO, 1.8V	PL Bank44 IO5 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.
C37	PL_AD14_LVDS44_L5N_HDGC	IO_L5N_HDGC_44	HD Bank 44	AD14	IO, 1.8V	PL Bank44 IO5 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
C38	PL_AC14_LVDS44_L6P_HDGC	IO_L6P_HDGC_44	HD Bank 44	AC14	IO, 1.8V	PL Bank44 IO6 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.
C39	PL_AC13_LVDS44_L6N_HDGC	IO_L6N_HDGC_44	HD Bank 44	AC13	IO, 1.8V	PL Bank44 IO6 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
D34	PL_AE15_LVDS44_L1P	IO_L1P_AD15P_44	HD Bank 44	AE15	IO, 1.8V	PL Bank44 IO1 differential positive. Same pin can be configured as PLSYSMON differential analog input15 positive or Single ended I/O.
D35	PL_AE14_LVDS44_L1N	IO_L1N_AD15N_44	HD Bank 44	AE14	IO, 1.8V	PL Bank44 IO1 differential negative. Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O.
D36	PL_AG14_LVDS44_L2P	IO_L2P_AD14P_44	HD Bank 44	AG14	IO, 1.8V	PL Bank44 IO2 differential positive. Same pin can be configured as PLSYSMON differential analog input14 positive or Single ended I/O.
D37	PL_AH14_LVDS44_L2N	IO_L2N_AD14N_44	HD Bank 44	AH14	IO, 1.8V	PL Bank44 IO2 differential negative. Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.
D38	PL_AG13_LVDS44_L3P	IO_L3P_AD13P_44	HD Bank 44	AG13	IO, 1.8V	PL Bank44 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.
D39	PL_AH13_LVDS44_L3N	IO_L3N_AD13N_44	HD Bank 44	AH13	IO, 1.8V	PL Bank44 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input13 negative or Single ended I/O.

**IO Type of IOs originating from ZU5/4/3T/3/2/1 MPSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU5/4/3T/3/2/1 MPSoC datasheet.*

2.7.2.4 PL IOs – HD BANK45

The Zynq UltraScale+ MPSoC SOM supports 24 Single Ended (SE) IOs on Board-to-Board Connector 1 from MPSoC's PL High-Density (HD) Bank45. Upon these 22 Single Ended IOs, upto 4 HDGC Global Clock Inputs and upto 16 PLSYSMON auxiliary analog inputs are available.

The IO voltage of PL Bank45 is connected from LDO4 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.2V to 3.3V through software. While using as DIFF IOs or Single Ended IOs, make sure to set the PMIC LDO4 to output appropriate IO voltage for PL Bank45. By default, IO voltage of PL Bank45 is set as 1.2V and after U-boot bootup configurable upto 3.3V. For more details about supported IO standard, refer the Zynq UltraScale+ MPSoC datasheet.

In the Zynq UltraScale+ MPSoC SOM, PL Bank45 signals are routed as differential IOs to Board-to-Board Connector 1, these pins can be used as DIFF/SE IOs if required. The Board-to-Board Connector 1 pins B41, B42, B43, B44, D41, D42, D43 and D44 are HDGC Global Clock Input capable pins of PL Bank45. Also, Board-to-Board Connector 1 pins A41, A42, A43, A44, A45, A46, B45, B46, C41, C42, C43, C44, C45, C46, D45 and D46 are PLSYSMON auxiliary analog Input capable pins of PL Bank45.

For more details on PL HD Bank45 pinouts on Board-to-Board Connector 1, refer the below table.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
A41	PL_B11_LVDS45_L10P	IO_L10P_AD10P_45	HD Bank 45	B11	IO, 1.8V	PL Bank45 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
A42	PL_A10_LVDS45_L10N	IO_L10N_AD10N_45	HD Bank 45	A10	IO, 1.8V	PL Bank45 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
A43	PL_A12_LVDS45_L11P	IO_L11P_AD9P_45	HD Bank 45	A12	IO, 1.8V	PL Bank45 IO11 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
A44	PL_A11_LVDS45_L11N	IO_L11N_AD9N_45	HD Bank 45	A11	IO, 1.8V	PL Bank45 IO11 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
A45	PL_D12_LVDS45_L12P	IO_L12P_AD8P_45	HD Bank 45	D12	IO, 1.8V	PL Bank45 IO12 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
A46	PL_C12_LVDS45_L12N	IO_L12N_AD8N_45	HD Bank 45	C12	IO, 1.8V	PL Bank45 IO12 differential negative. Same pin can be configured as

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
						PLSYSMON differential analog input8 negative or Single ended I/O.
B41	PL_G11_LVDS45_L5P_HDGC	IO_L5P_HDGC_45	HD Bank 45	G11	IO, 1.8V	PL Bank45 IO5 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.
B42	PL_F10_LVDS45_L5N_HDGC	IO_L5N_HDGC_45	HD Bank 45	F10	IO, 1.8V	PL Bank45 IO5 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
B43	PL_F12_LVDS45_L6P_HDGC	IO_L6P_HDGC_45	HD Bank 45	F12	IO, 1.8V	PL Bank45 IO6 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.
B44	PL_F11_LVDS45_L6N_HDGC	IO_L6N_HDGC_45	HD Bank 45	F11	IO, 1.8V	PL Bank45 IO6 differential negative Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
B45	PL_C11_LVDS45_L9P	IO_L9P_AD11P_45	HD Bank 45	C11	IO, 1.8V	PL Bank45 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
B46	PL_B10_LVDS45_L9N	IO_L9N_AD11N_45	HD Bank 45	B10	IO, 1.8V	PL Bank45 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
C41	PL_K13_LVDS45_L2P	IO_L2P_AD14P_45	HD Bank 45	K13	IO, 1.8V	PL Bank45 IO2 differential positive. Same pin can be configured as PLSYSMON differential analog input14 positive or Single ended I/O.
C42	PL_K12_LVDS45_L2N	IO_L2N_AD14N_45	HD Bank 45	K12	IO, 1.8V	PL Bank45 IO2 differential negative. Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.
C43	PL_H11_LVDS45_L3P	IO_L3P_AD13P_45	HD Bank 45	H11	IO, 1.8V	PL Bank45 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.
C44	PL_G10_LVDS45_L3N	IO_L3N_AD13N_45	HD Bank 45	G10	IO, 1.8V	PL Bank45 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input13 negative or Single ended I/O.
C45	PL_J12_LVDS45_L4P	IO_L4P_AD12P_45	HD Bank 45	J12	IO, 1.8V	PL Bank45 IO4 differential positive. Same pin can be configured as

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
						PLSYSMON differential analog input12 positive or Single ended I/O.
C46	PL_H12_LVDS45_L4N	IO_L4N_AD12N_45	HD Bank 45	H12	IO, 1.8V	PL Bank45 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input12 negative or Single ended I/O.
D41	PL_E10_LVDS45_L7P_HDGC	IO_L7P_HDGC_45	HD Bank 45	E10	IO, 1.8V	PL Bank45 IO7 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.
D42	PL_D10_LVDS45_L7N_HDGC	IO_L7N_HDGC_45	HD Bank 45	D10	IO, 1.8V	PL Bank45 IO7 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
D43	PL_E12_LVDS45_L8P_HDGC	IO_L8P_HDGC_45	HD Bank 45	E12	IO, 1.8V	PL Bank45 IO8 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.
D44	PL_D11_LVDS45_L8N_HDGC	IO_L8N_HDGC_45	HD Bank 45	D11	IO, 1.8V	PL Bank45 IO8 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
D45	PL_J11_LVDS45_L1P	IO_L1P_AD15P_45	HD Bank 45	J11	IO, 1.8V	PL Bank45 IO1 differential positive. Same pin can be configured as PLSYSMON differential analog input15 positive or Single ended I/O.
D46	PL_J10_LVDS45_L1N	IO_L1N_AD15N_45	HD Bank 45	J10	IO, 1.8V	PL Bank45 IO1 differential negative. Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O.

**IO Type of IOs originating from ZU5/4/3T/3/2/1 MPSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU5/4/3T/3/2/1 MPSoC datasheet.*

2.7.3 Power and Control Pins

The I/O supply voltages of HD Bank 44, HP Bank 65 and HP Bank 66 is connected to dedicated I/O voltage power pins located in Board-to-Board Connector 1. This connection enables expanded usage options and flexibility for both the carrier board and the end user. HP and HD Bank I/O supply voltages are configurable and it is described in the **MPSoC Power** section.

A Differential System Synchronization clock is provided from the Board-to-Board Connector 1 to the on-SOM clock synthesizer. This is an optional feature from the board-to-board connector. Also, a differential System Synchronization clock is provided from the on-board clock synthesizer to the Board-to-Board Connector 1.

To ensure proper electrical grounding, reduce EMI, and provide mechanical stability between the two boards, ground pins are distributed throughout the Board-to-Board Connectors.

For more details on these ground pins on Board-to-Board Connector 1, refer the below table.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
B1	VCCO_HD44	VCCO_44	PL HD Bank 44	AA14, AD13	Power	PL HD Bank 44 I/O Power Supply
C1	VCCO_HP65	VCCO_65	PL HP Bank 65	H5, J3, L4	Power	PL HP Bank 65 I/O Power Supply
D1	VCCO_HP66	VCCO_66	PL HP Bank 66	B7, D3, E6	Power	PL HP Bank 66 I/O Power Supply
A15	SYS_SYNC_CLOCKP[1]	-	-	-	I, DIFF	System Sync Clock Input Differential Pair Positive. (Optional)
A16	SYS_SYNC_CLOCKN[1]	-	-	-	I, DIFF	System Sync Clock Input Differential Pair Negative. (Optional)
A31	SYS_SYNC_CLK_OUTP	-	-	-	O, DIFF	System Sync Clock 125MHz output differential pair positive. This Synchronization clock is generated from OUT9 of on-som clock synthesizer.
A32	SYS_SYNC_CLK_OUTN	-	-	-	O, DIFF	System Sync Clock 125MHz output differential pair negative. This Synchronization clock is generated from OUT9b of on-som clock synthesizer.

B2B-1 Pin No	B2B Connector 1 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
A47	B2B_1PPS_IN	IO_L12N_AD0N_43	PL HD Bank 43	AB9	I, 1.8V LVCMOS	1Hz clock input from Carrier Board only for ZU5/4/3/2/1 MPSoC Devices.
		IO_L12N_AD0N_46	PL HD Bank 46	L13		1Hz clock input from Carrier Board only for ZU3T MPSoC Device.
A8, A17, A24, A33, A40, A48, A51, A52, A55, A56, A59, A60, B8, B17, B24, B33, B40, B49, B50, B53, B54, B57, B58, C8, C17, C24, C33, C40, C51, C52, C55, C56, C59, C60, D8, D17, D24, D33, D40, D49, D50, D53, D54, D57, D58	GND	NA	NA	NA	Power	Ground.

[1] Optional System Sync Clock Differential Clock input from the Board-to-Board Connector 1 is connected to the On-SOM Clock Synthesizer input.

2.8 Board-to-Board Connector 2

The Zynq UltraScale+ MPSoC SOM Board-to-Board Connector 2 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector 2 are explained in the following sections. The Board-to-Board Connector 2 is physically located on bottom side of the SOM as shown below.

Number of Pins	- 240
Connector Part Number	- ADM6-60-01.5-L-4-2-A-TR from Samtech
Mating Connector	- ADF6-60-03.5-L-4-2-A-TR from Samtech
Staking Height	- 5mm

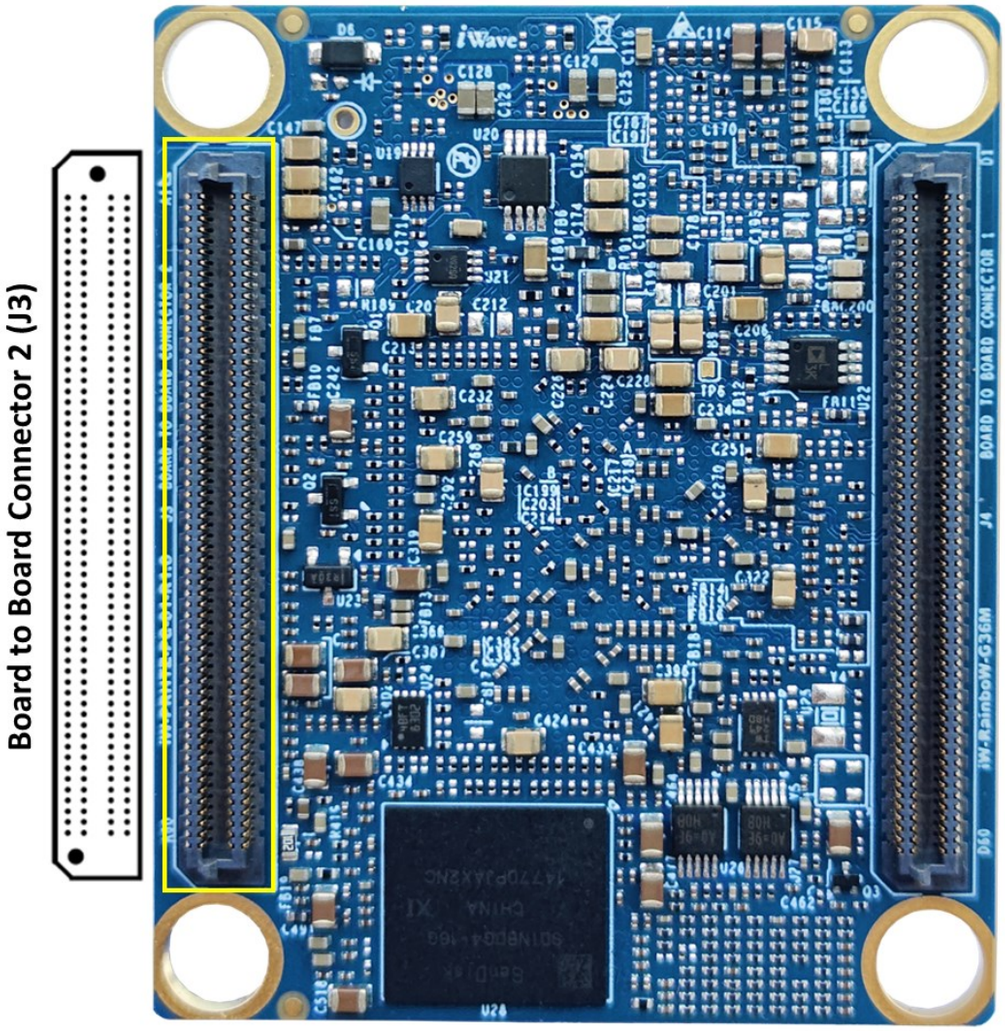

Figure 7: Board-to-Board Connector 2

Table 7: Board-to-Board Connector 2 Pinout

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	VCC_5V	**B1**	VCC_5V	**C1**	VCC_5V	**D1**	VCC_5V
A2	VCC_5V	**B2**	VCC_5V	**C2**	VCC_5V	**D2**	VCC_5V
A3	VCC_5V	**B3**	VCC_5V	**C3**	VCC_5V	**D3**	VCC_5V
A4	VCC_5V	**B4**	VCC_5V	**C4**	VCC_5V	**D4**	VCC_5V
A5	VCC_5V	**B5**	VCC_5V	**C5**	VCC_5V	**D5**	VCC_5V
A6	GND	**B6**	GND	**C6**	GND	**D6**	GND
A7	GND	**B7**	GND	**C7**	GND	**D7**	GND
A8	NC	**B8**	SOM_PWR_EN	**C8**	I2C0_SCL(PS_MIO10_500)	**D8**	NC
A9	PS_JTAG_TCK	**B9**	SOM_PWR_OK_1V8	**C9**	I2C0_SDA(PS_MIO11_500)	**D9**	VRTC_3V0
A10	PS_JTAG_TMS	**B10**	RESET_OUT#	**C10**	I2C1_SCL(PS_MIO24_500)	**D10**	SYSMON_DXP
A11	PS_JTAG_TDO	**B11**	RESET_SW_IN	**C11**	I2C1_SDA(PS_MIO25_500)	**D11**	SYSMON_DXN
A12	PS_JTAG_TDI	**B12**	PS_DONE	**C12**	GEM0_MDC(PS_MIO76_502)	**D12**	PS_MODE0
A13	UART0_TX(PS_MIO39_501)	**B13**	VCCO_HD45	**C13**	GEM0_MDIO(PS_MIO77_502)	**D13**	PS_MODE1
A14	UART0_RX(PS_MIO38_501)	**B14**	INT_IN	**C14**	SD1_WP/GEM3_INT(PS_MIO44_501)	**D14**	PS_MODE2
A15	GND	**B15**	GND	**C15**	GND	**D15**	GND
A16	USB_OTG_DM	**B16**	USB_PWR_EN	**C16**	GEM3_TX_CLK(PS_MIO64_502)	**D16**	PL_L14_SPI_SCLK
A17	USB_OTG_DP	**B17**	USB_OTG_ID	**C17**	GEM3_TXD0(PS_MIO65_502)	**D17**	PL_K14_SPI_MOSI
A18	GND	**B18**	VBUS_USB	**C18**	GEM3_TXD1(PS_MIO66_502)	**D18**	PL_J14_SPI_MISO
A19	GPHY_ATXRXM	**B19**	GPHY_ACTIVITY_LED1	**C19**	GEM3_TXD2(PS_MIO67_502)	**D19**	NC
A20	GPHY_ATXRXP	**B20**	GPHY_LINK_LED2	**C20**	GEM3_TXD3(PS_MIO68_502)	**D20**	PL_H14_SPI_SS1
A21	GND	**B21**	SD1_PWR(PS_MIO43_501)	**C21**	GEM3_TX_CTL(PS_MIO69_502)	**D21**	PL_H13_SPI_SS0
A22	GPHY_BTXRXM	**B22**	GND	**C22**	GND	**D22**	GND
A23	GPHY_BTXRXP	**B23**	SD1_CLK(PS_MIO51_501)	**C23**	GEM3_RX_CLK(PS_MIO70_502)	**D23**	UART1_TX(PS_MIO8_500)
A24	GND	**B24**	SD1_CMD(PS_MIO50_501)	**C24**	GEM3_RXD0(PS_MIO71_502)	**D24**	UART1_RX(PS_MIO9_500)
A25	GPHY_CTXRXM	**B25**	SD1_DATA0(PS_MIO46_501)	**C25**	GEM3_RXD1(PS_MIO72_502)	**D25**	SYSMON_VP
A26	GPHY_CTXRXP	**B26**	SD1_DATA1(PS_MIO47_501)	**C26**	GEM3_RXD2(PS_MIO73_502)	**D26**	SYSMON_VN
A27	GND	**B27**	SD1_DATA2(PS_MIO48_501)	**C27**	GEM3_RXD3(PS_MIO74_502)	**D27**	CAN1_RX(PS_MIO41_501)
A28	GPHY_DTXRXM	**B28**	SD1_DATA3(PS_MIO49_501)	**C28**	GEM3_RX_CTL(PS_MIO75_502)	**D28**	CAN1_TX(PS_MIO40_501)
A29	GPHY_DTXRXP	**B29**	SD1_CD(PS_MIO45_501)	**C29**	LS_PCIE_RSTN	**D29**	CAN0_RX(PS_MIO6_500)
A30	GND	**B30**	HS_PCIE_RSTN	**C30**	GND	**D30**	CAN0_TX(PS_MIO7_500)
A31	GTREFCLK0P_224	**B31**	GND	**C31**	B2B_GTREFCLK1P_224	**D31**	GND
A32	GTREFCLK0N_224	**B32**	GND	**C32**	B2B_GTREFCLK1N_224	**D32**	GND
A33	GND	**B33**	GTHRXP1_224	**C33**	GND	**D33**	GTHRXP3_224
A34	GND	**B34**	GTHRXN1_224	**C34**	GND	**D34**	GTHRXN3_224
A35	GTHRXP0_224	**B35**	GND	**C35**	GTHRXP2_224	**D35**	GND

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A36	GTHRXN0_224	**B36**	GND	**C36**	GTHRXN2_224	**D36**	GND
A37	GND	**B37**	GTHTXP1_224	**C37**	GND	**D37**	GTHTXP3_224
A38	GND	**B38**	GTHTXN1_224	**C38**	GND	**D38**	GTHTXN3_224
A39	GTHTXP0_224	**B39**	GND	**C39**	GTHTXP2_224	**D39**	GND
A40	GTHTXN0_224	**B40**	GND	**C40**	GTHTXN2_224	**D40**	GND
A41	GND	**B41**	PL_B15_LVDS46_L1P	**C41**	GND	**D41**	PL_C14_LVDS46_L4P
A42	GND	**B42**	PL_A15_LVDS46_L1N	**C42**	GND	**D42**	PL_C13_LVDS46_L4N
A43	NC	**B43**	GND	**C43**	PL_G13_LVDS46_L7P_HDGC	**D43**	GND
A44	NC	**B44**	GND	**C44**	PL_F13_LVDS46_L7N_HDGC	**D44**	GND
A45	GND	**B45**	PL_G15_LVDS46_L9P	**C45**	GND	**D45**	PL_B13_LVDS46_L3P
A46	GND	**B46**	NC	**C46**	GND	**D46**	PL_A13_LVDS46_L3N
A47	NC	**B47**	GND	**C47**	PL_E14_LVDS46_L6P_HDGC	**D47**	GND
A48	NC	**B48**	GND	**C48**	PL_E13_LVDS46_L6N_HDGC	**D48**	GND
A49	GND	**B49**	PL_F15_LVDS46_L8P_HDGC	**C49**	GND	**D49**	PL_B14_LVDS46_L2P
A50	GND	**B50**	PL_E15_LVDS46_L8N_HDGC	**C50**	GND	**D50**	PL_A14_LVDS46_L2N
A51	NC	**B51**	GND	**C51**	PL_AB11_LVDS43_L8P_HDGC	**D51**	GND
A52	NC	**B52**	GND	**C52**	PL_AC11_LVDS43_L8N_HDGC	**D52**	GND
A53	GND	**B53**	PL_W10_LVDS43_L10P	**C53**	GND	**D53**	PL_AE10_LVDS43_L4P
A54	GND	**B54**	PL_Y10_LVDS43_L10N	**C54**	GND	**D54**	PL_AF10_LVDS43_L4N
A55	PL_AB10_LVDS43_L12P	**B55**	GND	**C55**	PL_AD11_LVDS43_L7P_HDGC	**D55**	GND
A56	NC	**B56**	GND	**C56**	PL_AD10_LVDS43_L7N_HDGC	**D56**	GND
A57	GND	**B57**	PL_AA11_LVDS43_L9P	**C57**	GND	**D57**	PL_AH12_LVDS43_L3P
A58	GND	**B58**	PL_AA10_LVDS43_L9N	**C58**	GND	**D58**	PL_AH11_LVDS43_L3N
A59	PL_Y9_LVDS43_L11P	**B59**	GND	**C59**	PL_AC12_LVDS43_L6P_HDGC	**D59**	GND
A60	PL_AA8_LVDS43_L11N	**B60**	GND	**C60**	PL_AD12_LVDS43_L6N_HDGC	**D60**	GND

2.8.1 PS Interfaces

The interfaces which are supported in Board-to-Board Conenector2 from Zynq UltraScale+ MPSoC's PS is explained in the following section.

2.8.1.1 USB2.0 OTG Interface

The Zynq UltraScale+ MPSoC SOM supports one USB2.0 OTG interface on Board-to-Board Connector 2. USB0 OTG controller of Zynq UltraScale+ MPSoC PS is used for USB2.0 OTG interface. The USB OTG controller is capable of fulfilling a wide range of applications for USB2.0 implementations as a host, a device or On-the-Go. Also, this controller supports all high-speed, full-speed and low-speed transfers in both device and host modes. While using USB3.0 interface through PS-GTR, this USB2.0 OTG interface will co-work with USB3.0 interface.

The USB OTG controller uses the ULPI protocol to connect external ULPI PHY via the MIO pins. The Zynq UltraScale+ MPSoC SOM supports "USB3320" ULPI transceiver from Microchip and works at 1.8V IO voltage level. In Zynq UltraScale+ MPSoC SOM, PMIC GPIO "PC_GPIO7_RESET" is used for USB ULPI PHY reset. It supports active high power enable signal on Board-to-Board Connector 2 from USB PHY for external VBUS power control.

The reference clock for the on-board USB PHY is provided by the on-board clock synthesizer's OUT2 output, generating a single-ended 24 MHz clock.

Also, Zynq UltraScale+ MPSoC SOM supports USB ID & USB VBUS inputs from Board-to-Board Connector 2 and connected to USB PHY for USB Host/Device detection & VBUS monitoring respectively. If USB ID pin is grounded, then USB Host is detected and if it is floated, USB device is detected.

For more details on USB2.0 OTG Interface pinouts on Board-to-Board Connector 2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
A17	USB_OTG_DP	-	-	-	IO, USB	USB OTG data negative.
A16	USB_OTG_DM	-	-	-	IO, USB	USB OTG data positive.
B17	USB_OTG_ID	-	-	-	I, 3.3V CMOS	USB OTG ID input for USB host or device detection.
B18	VBUS_USB	-	-	-	I, 5V Power	USB active high power enable output to control external USB Vbus.
B16	USB_PWR_EN	-	-	-	O, 3.3V CMOS	USB active high power enable output to control external USB Vbus.

Note: if PS-GTR lane3 is selected as USB 3.0 then USB1 2.0 only can be used.

2.8.1.2 Gigabit Ethernet Interface

The Zynq UltraScale+ MPSoC SOM supports one 10/100/1000 Mbps Ethernet interface on Board-to-Board Connector 2. The MAC is integrated in the Zynq UltraScale+ MPSoC PS and connected to the external Gigabit Ethernet PHY "AR8031" on SOM. This Gigabit Ethernet PHY is interfaced with GEM0 interface of MPSoC's PS through MIO pins and works at 1.8V IO voltage level. The reference clock for the on-board Ethernet PHY is provided by the on-board clock synthesizer's OUT8 output, generating a single-ended 25 MHz clock.

In Zynq UltraScale+ MPSoC SOM, PMIC GPIO "PC_GPIO11_RESET" is used for Ethernet PHY reset. Also, SOM supports Ethernet PHY interrupt through PS GPIO "PS_MIO12_500". This PHY supports active high Link and Activity LED indication signals and available on Board-to-Board Connector 2. Since MAC and PHY are supported on SOM itself, only Magnetics is required on the carrier board.

In Zynq UltraScale+ MPSoC SOM, GEM0 Ethernet PHY Address is fixed to 001 as per below table.

PHYADDRESS2	PHYADDRESS1	PHYADDRESS0	Ethernet PHY Address
GPHY_ACTIVITY_LED1	RXD1	RXD0	**1**
0(PD)	0(PD)	1(PU)	

Important Note: GPHY_ACTIVITY_LED1 signal is muxed with PHYADDRESS2 pin. The same GPHY_ACTIVITY_LED1 signal is connected to B19th pin of Board-to-Board Connector 2 to support Gigabit Ethernet Activity LED.

For more details on Gigabit Ethernet Interface pinouts on Board-to-Board Connector 2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
A20	GPHY_ATXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 1 positive.
A19	GPHY_ATXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 1 negative.
A23	GPHY_BTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 2 positive.
A22	GPHY_BTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 2 negative.
A26	GPHY_CTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 3 positive.
A25	GPHY_CTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 3 negative.
A29	GPHY_DTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 4 positive.
A28	GPHY_DTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 4 negative.
B20	GPHY_LINK_LED 2	NA	NA	NA	O, 2.5V CMOS/ 10K PD	Gigabit Ethernet 1000Mbps Link status LED (Active High).

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
B19	GPHY_ACTIVITY_ LED1	NA	NA	NA	O, 2.5V CMOS/ 10K PD	Gigabit Ethernet Activity LED (Active High).

2.8.1.3 SD/SDIO Interface

The Zynq UltraScale+ MPSoC SOM supports SD/SDIO interface on Board-to-Board Connector 2. The SD1 controller of MPSoC's PS is used for SD/SDIO interface through MIO pins. This SD/SDIO controller is compatible with the standard SD Host Controller Specification Version 3.0. It supports different speed mode like Standard mode (19Mhz), High Speed mode (50Mhz), SDR12 (25Mhz), SDR25 (25Mhz), SDR50 (100Mhz), SDR104 (200Mhz) & DDR50 mode (50Mhz). Also in SD mode, data transfers in 1-bit and 4-bit modes.

The Zynq UltraScale+ MPSoC SOM supports Card Detect, Write Protect & Power Enable/Voltage Select pins through MIO pins.

For more details on SD/SDIO Interface pinouts on Board-to-Board Connector 2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
B23	SD1_CLK(PS_MIO 51_501)	PS_MIO51_501	501	L21	O, 1.8V LVCMOS/ 4.7K PU	SD1 Clock.
B24	SD1_CMD(PS_MI O50_501)	PS_MIO50_501	501	M19	IO, 1.8V LVCMOS/ 10K PU	SD1 Command.
B25	SD1_DATA0(PS_ MIO46_501)	PS_MIO46_501	501	L20	IO, 1.8V LVCMOS/ 10K PU	SD1 DATA0.
B26	SD1_DATA1(PS_ MIO47_501)	PS_MIO47_501	501	H21	IO, 1.8V LVCMOS/ 10K PU	SD1 DATA1.
B27	SD1_DATA2(PS_ MIO48_501)	PS_MIO48_501	501	J21	IO, 1.8V LVCMOS/ 10K PU	SD1 DATA2.
B28	SD1_DATA3(PS_ MIO49_501)	PS_MIO49_501	501	M18	IO, 1.8V LVCMOS/ 10K PU	SD1 DATA3.
B29	SD1_CD(PS_MIO4 5_501)	PS_MIO45_501	501	K20	IO, 1.8V LVCMOS/ 10K PU	SD1 Card Detect.
B21	SD1_PWR(PS_MI O43_501)	PS_MIO43_501	501	K19	O, 1.8V LVCMOS/ 4.7K PU	SD1 Power Enable/Voltage select.
C14	SD1_WP/GEM3_I NT(PS_MIO44_50 1)	PS_MIO44_501	501	J20	O, 1.8V LVCMOS/ 4.7K PU	SD1 Write Protect. This pin is multiplexed with GEM3 Interrupt pin.

Note: PS_MIO44_501 this pin is multiplexed with GEM3 Interrupt at the Board-to-board Connector 2.

2.8.1.4 RGMII Interface

The Zynq UltraScale+ MPSoC SOM supports RGMII or ULPI interface on Board-to-Board Connector 2. In Zynq UltraScale+ MPSoC PS, GEM3 RGMII interface and USB1 ULPI interface are multiplexed on the same pins. So, either one interface only can be used at a time. In Zynq UltraScale+ MPSoC SOM, these MIO pins are directly connected from MPSoC to Board-to-Board conenctor2. If RGMII/ULPI interface is not required on these pins, the same pins can be used as GPIOs or other alternate functions. Please refer PS Min Multiplexing section **2.9** for available alternate functions.

The Zynq UltraScale+ MPSoC gigabit Ethernet controller (GEM) implements a 10/100/1000 Mb/s Ethernet MAC that is compatible with the IEEE Standard for Ethernet (IEEE Std 802.3-2008). GEM controller supports MDIO interface for external PHY Management and it can be used through any PL Bank IOs through EMIO interface in SOM.

For more details on RGMII Interface pinouts on Board-to-Board Connector 2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
C16	GEM3_TX_CLK(PS_MIO64_502)	PS_MIO64_502	502	E19	O, 1.8V LVCMOS	GEM3 RGMII Transmit Clock. Or USB1 ULPI Clock.
C17	GEM3_TXD0(PS_MIO65_502)	PS_MIO65_502	502	A18	O, 1.8V LVCMOS	GEM3 RGMII Transmit DATA0. Or USB1 ULPI Direction Control.
C18	GEM3_TXD1(PS_MIO66_502)	PS_MIO66_502	502	G19	O, 1.8V LVCMOS	GEM3 RGMII Transmit DATA1. Or USB1 ULPI Bi-Directional Data2.
C19	GEM3_TXD2(PS_MIO67_502)	PS_MIO67_502	502	B18	O, 1.8V LVCMOS	GEM3 RGMII Transmit DATA2. Or USB1 ULPI NXT.
C20	GEM3_TXD3(PS_MIO68_502)	PS_MIO68_502	502	C18	O, 1.8V LVCMOS	GEM3 RGMII Transmit DATA3. Or USB1 ULPI Bi-Directional Data0.
C21	GEM3_TX_CTL(PS_MIO69_502)	PS_MIO69_502	502	D19	O, 1.8V LVCMOS	GEM3 RGMII Transmit Control. Or USB1 ULPI Bi-Directional Data1.
C23	GEM3_RX_CLK(PS_MIO70_502)	PS_MIO70_502	502	C19	I, 1.8V LVCMOS	GEM3 RGMII Receive Clock. Or USB1 ULPI STP.
C24	GEM3_RXD0(PS_MIO71_502)	PS_MIO71_502	502	B19	I, 1.8V LVCMOS	GEM3 RGMII Receive control. Or USB1 ULPI Bi-Directional Data7.
C25	GEM3_RXD1(PS_MIO72_502)	PS_MIO72_502	502	G20	I, 1.8V LVCMOS	GEM3 RGMII Receive DATA0. Or USB1 ULPI Bi-Directional Data3.
C26	GEM3_RXD2(PS_MIO73_502)	PS_MIO73_502	502	G21	I, 1.8V LVCMOS	GEM3 RGMII Receive DATA1. Or USB1 ULPI Bi-Directional Data4.
C27	GEM3_RXD3(PS_MIO74_502)	PS_MIO74_502	502	D20	I, 1.8V LVCMOS	GEM3 RGMII Receive DATA2. Or USB1 ULPI Bi-Directional Data5.
C28	GEM3_RX_CTL(PS_MIO75_502)	PS_MIO75_502	502	A19	I, 1.8V LVCMOS	GEM3 RGMII Recieve Control. Or USB1 ULPI Bi-Directional Data1.
C12	GEM0_MDC(PS_MIO76_502)	PS_MIO76_502	502	B20	O, 1.8V LVCMOS	MDC Clock Output

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
C13	GEM0_MDIO(PS_MIO77_502)	PS_MIO77_502	502	F20	IO, 1.8V LVCMOS	MDIO Data In/Out
C14	SD1_WP/GEM3_INT(PS_MIO44_501)	PS_MIO44_501	501	J20	O, 1.8V LVCMOS/ 4.7K PU	GEM3 Interrupt Input. This pin is multiplexed with SD1 Write protect.

** Signal direction is considering with respect to GEM3 RGMII interface.*

Note: When using PS_MIO44_501 pin for SD1 write protect function, GEM3 interrupt cannot be used on same pin.

2.8.1.5 SPI Interface

The Zynq UltraScale+ MPSoC SOM supports one SPI interface with two chips select pins on Board-to-Board Connector 2. The SPI1 controller of MPSoC's PS is used for SPI interface through PL IOs. It can function in master mode, slave mode or multi-master mode and supports full-duplex operation.

For more details on SPI Interface pinouts on Board-to-Board Connector 2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/Termination	Description
D16	PL_L14_SPI_SCLK	IO_L12P_AD0P_46	HD Bank 46	L14	O, 1.8V LVCMOS	SPI Clock
D18	PL_J14_SPI_MISO	IO_L11N_AD1N_46	HD Bank 46	J14	IO, 1.8V LVCMOS	SPI Master input Slave output.
D17	PL_K14_SPI_MOSI	IO_L11P_AD1P_46	HD Bank 46	K14	IO, 1.8V LVCMOS	SPI Master output Slave input.
D20	PL_H14_SPI_SS1	IO_L10P_AD2P_46	HD Bank 46	H14	O, 1.8V LVCMOS	SPI Chip select1
D21	PL_H13_SPI_SS0	IO_L10N_AD2N_46	HD Bank 46	H13	IO, 1.8V LVCMOS	SPI Chip select0. This chip select can be used for both master or slave mode.

2.8.1.6 Debug UART Interface

The Zynq UltraScale+ MPSoC SOM supports one Debug UART interface on Board-to-Board Connector 2. The UART0 controller of MPSoC's PS is used for Debug UART interface through MIO pins. This controller supports full-duplex asynchronous receiver and transmitter.

For more details on Debug UART pinouts on Board-to-Board Connector 2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
A13	UART0_TX(PS_MIO39_501)	PS_MIO39_500	500	H19	O, 1.8V LVCMOS	UART0 Transmit data line for Debug.
A14	UART0_RX(PS_MIO38_501)	PS_MIO38_500	500	H18	I, 1.8V LVCMOS	UART0 Receive data line for Debug.

2.8.1.7 Data UART Interface

The Zynq UltraScale+ MPSoC SOM supports one DATA UART interface on Board-to-Board Connector 2. The UART1 controller of MPSoC's PS is used for Data UART interface through MIO pins.

For more details on Data UART pinouts on Board-to-Board Connector 2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
D23	UART1_TX(PS_MIO8_500)	PS_MIO8_500	500	AF17	O, 1.8V LVCMOS	UART1 Transmit data line.
D24	UART1_RX(PS_MIO9_500)	PS_MIO9_500	500	AC16	I, 1.8V LVCMOS	UART1 Receive data line.

2.8.1.8 CAN Interface

The Zynq UltraScale+ MPSoC SOM supports two CAN interfaces on Board-to-Board Connector 2. The CAN0 & CAN1 controller of MPSoC's PS is used for CAN interface through MIO pins. This CAN controller is compatible with the ISO 11898-1, CAN 2.0A, and CAN 2.0B standards. And it supports bit rates up to 1Mb/s.

If CAN interface is not required on these pins, the same pins can be used as GPIOs or other alternate functions. Please refer PS Min Multiplexing section **2.9** for available alternate functions.

For more details on CAN Interface pinouts on Board-to-Board Connector 2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
D27	CAN1_RX(PS_MIO41_501)	PS_MIO41_501	501	J19	I, 1.8V LVCMOS	CAN1 Receive Data
D28	CAN1_TX(PS_MIO40_501)	PS_MIO40_501	501	K18	O, 1.8V LVCMOS	CAN1 Transmit Data
D30	CAN0_TX(PS_MIO7_500)	PS_MIO7_501	501	AH17	I, 1.8V LVCMOS	CAN0 Transmit Data
D29	CAN0_RX(PS_MIO6_500)	PS_MIO6_501	501	AF16	O, 1.8V LVCMOS	CAN0 Receive Data

Note: When using QSPI Flash with feedback clock functionality the CAN0 Interface is not available.

2.8.1.9 I2C Interface

The Zynq UltraScale+ MPSoC SOM supports two I2C interface on Board-to-Board Connector 2 I2C0 & I2C1. The I2C module of MPSoC's PS is used for I2C interface through MIO pins and compatible with the standard NXP I2C bus protocol. It supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. It can function as a master or a slave in a multi-master design. The master can be programmed to use both normal (7-bit) addressing and extended (10-bit) addressing modes. Since flexible I2C standard allows multiple devices to be connected to the single bus, I2C1 interface is also connected to On-SOM PMIC with I2C address 0x5A, 0X5B, On-SOM Clock Synthesizer with 0x76h and EEPROM with 0x50 & 0x51 addresses in the Zynq UltraScale+ MPSoC SOM. Also, one more I2C interface (I2C0) can be taken out on Board-to-Board Connector 2 which is multiplexed with PS GPIOs.

For more details on I2C Interface pinouts on Board-to-Board Connector 2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
C9	I2C0_SDA(PS_MIO11_500)	PS_MIO11_500	500	AE17	IO, 1.8V OD/ 4.7K PU	I2C0 data.
C8	I2C0_SCL(PS_MIO10_500)	PS_MIO10_500	500	AD17	O, 1.8V OD/ 4.7K PU	I2C0 clock.
C10	I2C1_SCL(PS_MIO24_500)	PS_MIO24_500	500	AB19	IO, 1.8V LVCMOS/ 4.7K PU	I2C1 Clock
C11	I2C1_SDA(PS_MIO25_500)	PS_MIO25_500	500	AB21	O, 1.8V LVCOMS/ 4.7K PU	I2C1 Data

2.8.1.10 JTAG Interface

The Zynq UltraScale+ MPSoC SOM supports JTAG interface on Board-to-Board Connector 2. The Zynq UltraScale+ MPSoC's PS and PL share a common set of JTAG pins and each have their own TAP controller which are chained together inside the Zynq UltraScale+ MPSoC.

For more details on JTAG Interface pinouts on Board-to-Board Connector 2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
A12	PS_JTAG_TDI	PS_JTAG_TDI	503	R18	I, 1.8V LVCMOS/ 4.7K	JTAG Test Data Input.
A10	PS_JTAG_TMS	PS_JTAG_TMS	503	N21	I, 1.8V LVCMOS/ 4.7K	JTAG Test Mode Select.
A9	PS_JTAG_TCK	PS_JTAG_TCK	503	R19	I, 1.8V LVCMOS/ 4.7K	JTAG Test Clock.
A11	PS_JTAG_TDO	PS_JTAG_TDO	503	T21	O, 1.8V LVCMOS	JTAG Test Data Output.

2.8.2 PL Interfaces

The interfaces which are supported in Board-to-Board Connector 2 from Zynq UltraScale+ MPSoC's PL is explained in the following section.

2.8.2.1 GTH High Speed Transceivers

The Zynq UltraScale+ MPSoC (ZU5/4/3T -EV, EG, CG) supports 4 GTH transceiver Lanes through one transceiver Bank 224 with line rate from 500Mbps to 12.5Gbps based on the speed grade of the MPSoC. These transceivers can be used to interface to multiple high-speed interface protocols. Each GTH transceiver quad supports two dedicated reference clock input pairs.

For more details on GTH transceiver pinouts on Board-to-Board Connector 2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
A36	GTHRXN0_224	MGTHRXN0_224	224	Y1	I, DIFF	GTH Bank224 channel0 High speed differential receiver negative.
B34	GTHRXN1_224	MGTHRXN1_224	224	V1	I, DIFF	GTH Bank224 channel1 High speed differential receiver negative.
C36	GTHRXN2_224	MGTHRXN2_224	224	T1	I, DIFF	GTH Bank224 channel2 High speed differential receiver negative.
D34	GTHRXN3_224	MGTHRXN3_224	224	P1	I, DIFF	GTH Bank224 channel3 High speed differential receiver negative.
A35	GTHRXP0_224	MGTHRXP0_224	224	Y2	I, DIFF	GTH Bank224 channel0 High speed differential receiver positive.
B33	GTHRXP1_224	MGTHRXP1_224	224	V2	I, DIFF	GTH Bank224 channel1 High speed differential receiver positive.
C35	GTHRXP2_224	MGTHRXP2_224	224	T2	I, DIFF	GTH Bank224 channel2 High speed differential receiver positive.
D33	GTHRXP3_224	MGTHRXP3_224	224	P2	I, DIFF	GTH Bank224 channel3 High speed differential receiver positive.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
A40	GTHTXN0_224	MGTHTXN0_224	224	W3	O, DIFF	GTH Bank224 channel0 High speed differential transmitter negative.
B38	GTHTXN1_224	MGTHTXN1_224	224	U3	O, DIFF	GTH Bank224 channel1 High speed differential transmitter negative.
C40	GTHTXN2_224	MGTHTXN2_224	224	R3	O, DIFF	GTH Bank224 channel2 High speed differential transmitter negative.
D38	GTHTXN3_224	MGTHTXN3_224	224	N3	O, DIFF	GTH Bank224 channel3 High speed differential transmitter negative.
A39	GTHTXP0_224	MGTHTXP0_224	224	W4	O, DIFF	GTH Bank224 channel0 High speed differential transmitter positive.
B37	GTHTXP1_224	MGTHTXP1_224	224	U4	O, DIFF	GTH Bank224 channel1 High speed differential transmitter positive.
C39	GTHTXP2_224	MGTHTXP2_224	224	R4	O, DIFF	GTH Bank224 channel2 High speed differential transmitter positive.
D37	GTHTXP3_224	MGTHTXP3_224	224	N4	O, DIFF	GTH Bank224 channel3 High speed differential transmitter positive.
A32	GTREFCLK0N_224	MGTREFCLK0N_224	224	Y5	I, DIFF	GTH Bank224 channel0 High speed differential reference clock0 negative.
A31	GTREFCLK0P_224	MGTREFCLK0P_224	224	Y6	I, DIFF	GTH Bank224 channel0 High speed differential reference clock0 positive.
C32	B2B_GTREFCLK1N_224	MGTREFCLK1N_224	224	V5	I, DIFF	No Connect. Optionally connected to GTH Bank224 channel1 High speed differential reference clock negative.
C31	B2B_GTREFCLK1P_224	MGTREFCLK1P_224	224	V6	I, DIFF	No Connect. Optionally connected to GTH Bank224 channel1 High speed differential reference clock positive.

2.8.2.2 PL IOs – HD BANK43

The Zynq UltraScale+ MPSoC SOM supports 17 Single Ended (SE) IOs on Board-to-Board Connector 2 from MPSoC's PL High-Density (HD) Bank43. Upon these 8 Differential IOs, 17 Single Ended IOs, upto 3 HDGC Global Clock Inputs and upto 8 PLSYSMON auxiliary analog inputs are available.

The IO voltage of PL Bank43 (& Bank46) is connected from LDO7 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.2V to 3.3V through software. While using as DIFF IOs or Single Ended IOs, make sure to set the PMIC

LDO7 to output appropriate IO voltage for PL Bank43. By default, IO voltage of PL Bank43 is set as 1.2V and after U-boot bootup configurable to up 3.3V. For more details about supported IO standard, refer the Zynq UltraScale+ MPSoC datasheet.

In the Zynq UltraScale+ MPSoC SOM, PL Bank43 signals are routed as LVDS IOs to Board-to-Board Connector 2. Even though PL Bank43 signals are routed as DIFF IOs, these pins can be used as DIFF IOs if required. The Board-to-Board Connector 2 pins C51, C52, C55, C56, C59 and C60 are HDGC Global Clock Input capable pins of PL Bank43. Also, Board-to-Board Connector 1 pins A59, A60, B53, B54, B57, B58, C51, C52, C55, C56, C59, C60, D53, D54, D57and D58 are PLSYSMON auxiliary analog Input capable pins of PL Bank43.

For more details on PL HD Bank43 pinouts on Board-to-Board Connector 2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
A55	PL_AB10_LVDS43_L12P	IO_L12P_AD0P_43	HD Bank 43	AB10	IO, 1.8V	PL Bank43 IO12 Single Ended
A59	PL_Y9_LVDS43_L11P	IO_L11P_AD1P_43	HD Bank 43	Y9	IO, 1.8V	PL Bank43 IO11 differential positive. Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.
A60	PL_AA8_LVDS43_L11N	IO_L11N_AD1N_43	HD Bank 43	AA8	IO, 1.8V	PL Bank43 IO11 differential negative. Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.
B53	PL_W10_LVDS43_L10P	IO_L10P_AD2P_43	HD Bank 43	W10	IO, 1.8V	PL Bank43 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input2 positive or Single ended I/O.
B54	PL_Y10_LVDS43_L10N	IO_L10N_AD2N_43	HD Bank 43	Y10	IO, 1.8V	PL Bank43 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input2 negative or Single ended I/O.
B57	PL_AA11_LVDS43_L9P	IO_L9P_AD3P_43	HD Bank 43	AA11	IO, 1.8V	PL Bank43 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
B58	PL_AA10_LVDS43_L9N	IO_L9N_AD3N_43	HD Bank 43	AA10	IO, 1.8V	PL Bank43 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.
C51	PL_AB11_LVDS43_L8P_HDGC	IO_L8P_HDGC_AD4P_43	HD Bank 43	AB11	IO, 1.8V	PL Bank43 IO8 differential positive Same pin can be configured as HDGC Global Clock Input differential positive, PLSYSMON differential analog input4 positive or Single ended I/O.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
C52	PL_AC11_LVDS43_L8N_HDGC	IO_L8N_HDGC_AD4N_43	HD Bank 43	AC11	IO, 1.8V	PL Bank43 IO8 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative, PLSYSMON differential analog input4 negative or Single ended I/O.
C55	PL_AD11_LVDS43_L7P_HDGC	IO_L7P_HDGC_AD5P_43	HD Bank 43	AD11	IO, 1.8V	PL Bank43 IO7 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive, PLSYSMON differential analog input5 positive or Single ended I/O.
C56	PL_AD10_LVDS43_L7N_HDGC	IO_L7N_HDGC_AD5N_43	HD Bank 43	AD10	IO, 1.8V	PL Bank43 IO7 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative, PLSYSMON differential analog input5 negative or Single ended I/O.
C59	PL_AC12_LVDS43_L6P_HDGC	IO_L6P_HDGC_AD6P_43	HD Bank 43	AC12	IO, 1.8V	PL Bank43 IO6 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive, PLSYSMON differential analog input6 positive or Single ended I/O.
C60	PL_AD12_LVDS43_L6N_HDGC	IO_L6N_HDGC_AD6N_43	HD Bank 43	AD12	IO, 1.8V	PL Bank43 IO6 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative, PLSYSMON differential analog input6 negative or Single ended I/O.
D53	PL_AE10_LVDS43_L4P	IO_L4P_AD8P_43	HD Bank 43	AE10	IO, 1.8V	PL Bank43 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
D54	PL_AF10_LVDS43_L4N	IO_L4N_AD8N_43	HD Bank 43	AF10	IO, 1.8V	PL Bank43 IO4 differential negative Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
D57	PL_AH12_LVDS43_L3P	IO_L3P_AD9P_43	HD Bank 43	AH12	IO, 1.8V	PL Bank43 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
D58	PL_AH11_LVDS43_L3N	IO_L3N_AD9N_43	HD Bank 43	AH11	IO, 1.8V	PL Bank43 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.

**IO Type of IOs originating from ZU5/4/3T/3/2/1 MPSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU5/4/3T/3/2/1 MPSoC datasheet.*

2.8.2.3 PL IOs –HD BANK46

The Zynq UltraScale+ MPSoC SOM supports 7 Differential/14 Single Ended (SE) IOs on Board-to-Board Connector 2 from MPSoC's PL High-Density (HD) Bank46. Upon these 7 Differential/15 Single Ended IOs, upto 3 HDGC Global Clock Inputs and upto 7 PLSYSMON auxiliary analog inputs are available.

The IO voltage of PL Bank46 (& Bank43) is connected from LDO7 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.2V to 3.3V through software. While using as DIFF IOs or Single Ended IOs, make sure to set the PMIC LDO7 to output appropriate IO voltage for PL Bank46. By default, IO voltage of PL Bank46 is set as 1.2V and after U-boot bootup configurable to up 3.3V. For more details about supported IO standard, refer the Zynq UltraScale+ MPSoC datasheet.

In the Zynq UltraScale+ MPSoC SOM, PL Bank46 signals are routed as LVDS IOs to Board-to-Board Connector 2. Even though PL Bank46 signals are routed as DIFF IOs, these pins can be used as SE/DIFF IOs if required. The Board-to-Board Connector 2 pins B49, B50, C43, C44, C47 and C48 are HDGC Global Clock Input capable pins of PL Bank46. Also, Board-to-Board Connector 2 pins B41, B42, B49, B50, C43, C44, C47, C48, D41, D42, D45, D46, D49 and D50 are PLSYSMON auxiliary analog Input capable pins of PL Bank46.

For more details on PL HD Bank46 pinouts on Board-to-Board Connector 2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
B41	PL_B15_LVDS46_L1P	IO_L1P_AD11P_46	HD Bank 46	B15	IO, 1.8V	PL Bank46 IO1 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
B42	PL_A15_LVDS46_L1N	IO_L1N_AD11N_46	HD Bank 46	A15	IO, 1.8V	PL Bank46 IO1 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
B45	PL_G15_LVDS46_L9P	IO_L9P_AD3P_46	HD Bank 46	G15	IO, 1.8V	PL Bank46 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
B49	PL_F15_LVDS46_L8P_HDGC	IO_L8P_HDGC_AD4P_46	HD Bank 46	F15	IO, 1.8V	PL Bank46 IO8 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive, PLSYSMON differential analog input4 positive or Single ended I/O.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
B50	PL_E15_LVDS46_L8N_HDGC	IO_L8N_HDGC_AD4N_46	HD Bank 46	E15	IO, 1.8V	PL Bank46 IO8 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative, PLSYSMON differential analog input4 negative or Single ended I/O.
C43	PL_G13_LVDS46_L7P_HDGC	IO_L7P_HDGC_AD5P_46	HD Bank 46	G13	IO, 1.8V	PL Bank46 IO7 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive, PLSYSMON differential analog input5 positive or Single ended I/O.
C44	PL_F13_LVDS46_L7N_HDGC	IO_L7N_HDGC_AD5N_46	HD Bank 46	F13	IO, 1.8V	PL Bank46 IO7 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative, PLSYSMON differential analog input5 negative or Single ended I/O.
C47	PL_E14_LVDS46_L6P_HDGC	IO_L6P_HDGC_AD6P_46	HD Bank 46	E14	IO, 1.8V	PL Bank46 IO6 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive, PLSYSMON differential analog input6 positive or Single ended I/O.
C48	PL_E13_LVDS46_L6N_HDGC	IO_L6N_HDGC_AD6N_46	HD Bank 46	E13	IO, 1.8V	PL Bank46 IO6 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative, PLSYSMON differential analog input6 negative or Single ended I/O.
D41	PL_C14_LVDS46_L4P	IO_L4P_AD8P_46	HD Bank 46	C14	IO, 1.8V	PL Bank46 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
D42	PL_C13_LVDS46_L4N	IO_L4N_AD8N_46	HD Bank 46	C13	IO, 1.8V	PL Bank46 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
D45	PL_B13_LVDS46_L3P	IO_L3P_AD9P_46	HD Bank 46	B13	IO, 1.8V	PL Bank46 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
D46	PL_A13_LVDS46_L3N	IO_L3N_AD9N_46	HD Bank 46	A13	IO, 1.8V	PL Bank46 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type*/ Termination	Description
D49	PL_B14_LVDS46_L2P	IO_L2P_AD10P_46	HD Bank 46	B14	IO, 1.8V	PL Bank46 IO2 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
D50	PL_A14_LVDS46_L2N	IO_L2N_AD10N_46	HD Bank 46	A14	IO, 1.8V	PL Bank46 IO2 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.

**IO Type of IOs originating from ZU5/4/3T/3/2/1 MPSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU5/4/3T/3/2/1 MPSoC datasheet.*

2.8.3 Power and Control Pins

The Zynq UltraScale+ MPSoC SOM uses a 5V power input (VCC) from Board-to-Board Connector 2 and generates all other necessary powers internally on the SOM itself. The SOM power can be turned on or off from the carrier board using the SOM Power enable pin (B8) in Board-to-Board Connector 2. Carrier Board will send the SOM Power Enable signal to enable on-SOM power regulators, eventually the Zynq UltraScale+ MPSoC SOM sends a SOM Power OK signal to the carrier board after the final power rail in the SOM becomes stable.

The Zynq UltraScale+ MPSoC SOM supports VCC_RTC coin cell power input from Board-to-Board Connector 2, which is connected to the PMIC's VBBAT pin for real-time clock backup voltage. It also supports a warm reset input from Board-to-Board Connector 2, dedicated RSTBTN# Pin from board-to-board connector 2 is connected to the PS_SRST_B pin of MPSoC.

For High Speed PCIe reset signal connection, it's connected to the Board-to-board Connector 2 (B30), and it is connected to HP bank 65's dedicated PCIe reset functioned pin (IO_L24N_T3U_N11_PERSTN0_65). Moreover, an option of the same pin is connected to HP bank 66 to support reset functionality in SoC configurations where HP Bank 65 is not available. It is recommended to use the dedicated PCIe reset pin from HP bank 65.

The PS GTR PCIe reset pin is connected by default from PS_MIO42_501. An optional connection of the PS GTR PCIe reset is given to PS_MIO37 when the PS PCIe needs to work as an Endpoint. Note that the GEM0 interface is not supported when using the PS_MIO37_501 as LS PCIe reset because the pin is used as one of the control signals of Ethernet PHY in the SOM.

A dedicated interrupt pin is provided as input from the Board-to-board connector. By Default, this interrupt pin is connected to the HD bank 43. Optionally this pin is connected to the HD bank 46 for SoCs where HD bank 43 is not available.

An extended option for selecting the boot media to the board-to-board connectors is available in the Zynq UltraScale+ MPSoC SOM. This feature allows the end user to choose the boot media in the carrier board itself without any hardware changes in the SOM. PS MODE Pins configuration is provided at the **MPSoC Boot Mode** Section.

Additionally, Ground pins are distributed throughout the Board-to-Board Connectors for better performance.

For more details on these pins on Board-to-Board Connector 2, refer the below table.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
D9	VRTC_3V0	NA	NA	NA	I, 3V Power	3V backup coin cell input for RTC.
B11	RESET_SW_IN	PS_SRST_B	PS Bank 503	AB27	I, 1.8V LVCMOS/ 4.7K PU	Active low reset input.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
B8	SOM_PWR_EN	NA	NA	NA	I, 5V Power	SOM Power Enable *Important Note:* *High – SOM power ON* *Low – SOM Power OFF*
B9	SOM_PWR_OK_1V8	NA	NA	NA	O, 1.8V Power	Active High SOM Power Good
B10	RESET_OUT#	IO_T2U_N12_66	HP Bank 66	E7	O, 1.8V, LVCMOS	Reset Out for ZU1/2/3T/3/4 MPSoC Configuration
		IO_T3U_N12_65	HP Bank 65	K5		Reset Out for ZU5/4 MPSoC Configurations.
B12	PS_DONE	PS_DONE	PS Bank 503	M21	1, 1.8V, LVCMOS/ 4.7K PU	Configuration done pin.
D12	PS_MODE0	PS_MODE0	PS Bank 503	P19	I, 1.8V LVCMOS	Boot Mode0 Select pin
D13	PS_MODE1	PS_MODE1	PS Bank 503	P20	I, 1.8V LVCMOS	Boot Mode1 Select pin
D14	PS_MODE2	PS_MODE2	PS Bank 503	R20	I, 1.8V LVCMOS	Boot Mode2 Select pin
B30	HS_PCIE_RSTN	IO_L24N_T3U_N11_PERSTN0_65	PL HP Bank 65	H8	IO, 1.8V LVCMOS	PL HS PCIe Reset for RP and EP Mode. *This pin is connected for ZU5/4 MPSoC SOM Configurations for HS PCIe Reset.*
		IO_L23N_T3U_N9_66	PL HP Bank 66	A8	IO, 1.8V LVCMOS	*For ZU3T MPSoC SOM Configuration this pin is utilized as PL HS PCIe Reset.*
C29	LS_PCIe_RSTn	PS_MIO42_501	PS Bank 501	L18	IO, 1.8V LVCMOS	LS PCIe Reset for RP Mode.
		PS_MIO37_501		J17		Optional LS PCIe Reset for EP Mode. GEM0 interface is unavailable while using this pin for EP Mode.
B14	INT_IN	IO_L5N_HDGC_AD7N_43	HD Bank 43	AF12	I, 1.8V LVCMOS	Dedicated interrupt input for ZU5/4/3/2/1 MPSoC Device configurations.
		IO_L5N_HDGC_AD7N_46	HD Bank 46	D14		Dedicated Interrupt input for ZU3T MPSoC Device configuration.

B2B-2 Pin No	B2B Connector 2 Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
D25	SYSMON_VP	VP	Bank 0	R13	I, 1.8V LVCMOS	System Monitor dedicated differential analog input (positive side).
D26	SYSMON_VN	VN	Bank 0	T12	I, 1.8V LVCMOS	System Monitor dedicated differential analog input (negative side).
D10	SYSMON_DXP	DXP	Bank 0	U13	NA	Optional Temperature-sensing diode anode pin.
D11	SYSMON_DXN	DXN	Bank 0	U12	NA	Optional Temperature-sensing diode cathode pin.
A1, A2, A3, A4, A5, B1, B2, B3, B4, B5, C1, C2, C3, C4, C5, D1, D2, D3, D4, D5	VCC_5V	NA	NA	NA	I, 5V Power	Supply Voltage.
A6, A7, A15, A18, A21, A24, A27, A30, A33, A34, A37, A38, A41, A42, A45, A46, A49, A50, A53, A54, A57, A58, B6, B7, B15, B22, B31, B32, B35, B36, B39, B40, B43, B44, B47, B48, B51, B52, B55, B56, B59, B60, C6, C7, C15, C22, C30 C33, C34, C37, C38, C41, C42, C45, C46, C49, C50, C53, C54, C57, C58, D6, D7, D15, D22, D31, D32, D35, D36, D39, D40, D43, D44, D47, D48, D51, D52, D55, D56, D59, D60	GND	NA	NA	NA	Power	Ground.

2.9 Zynq UltraScale+ MPSoC PS Pin Multiplexing on Board-to-Board Connectors

The Zynq UltraScale+ MPSoC PS IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also, most of MPSoC PS IO pins can be configured as GPIO if required. The below table provides the details of PS pin connections on Zynq UltraScale+ MPSoC SOM with selected pin function (highlighted) and available alternate functions. This table has been prepared by referring PS I/O configuration in Xilinx Vivado Design Suite. To know the complete available alternate functions, refer the PS I/O configuration in the latest Vivado Design Suite

Table 8: PS IOMUX on Zynq UltraScale+ MPSoC SOM

Interface/ Function	B2B Connector Pin Number	Zynq UltraScale+ MPSoC Pin Name	GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13
On SOM Features from MPSoC PS																
eMMC FLASH	NA	PS_MIO13_500	GPIO13	NFC_CE	eMMC_DATA0	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TDI	SPI0_SS2	-	-	UART1_RX	-
	NA	PS_MIO14_500	GPIO14	NFC_CLE	eMMC _DATA1	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TDO	SPI0_SS1	-	UART0_RX	-	-
	NA	PS_MIO15_500	GPIO15	NFC_ALE	eMMC_DATA2	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TMS	SPI0_SS0	-	UART0_TX	-	-
	NA	PS_MIO16_500	GPIO16	NFC_DATA0	eMMC _DATA3	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-	-	UART1_TX	-
	NA	PS_MIO17_500	GPIO17	NFC_DATA1	eMMC _DATA4	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MIOSI	-	-	UART1_RX	-
	NA	PS_MIO18_500	GPIO18	NFC_DATA2	eMMC _DATA5	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SCLK	UART0_RX	-	-
	NA	PS_MIO19_500	GPIO19	NFC_DATA3	eMMC _DATA6	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS2	UART0_TX	-	-
	NA	PS_MIO20_500	GPIO20	NFC_DATA4	eMMC _DATA7	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SS1	-	UART1_TX	-
	NA	PS_MIO21_500	GPIO21	NFC_DATA5	eMMC _CMD	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS0	-	UART1_RX	-
	NA	PS_MIO22_500	GPIO22	NFC_WE_B	eMMC _CLK	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	-
	NA	PS_MIO23_500	GPIO23	NFC_DATA6	eMMC_Reset	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	-
GEM0	NA	PS_MIO26_501	GPIO26	GEM0_TX_CLK	-	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TCK	SPI0_SCLK	-	UART0_RX	-	-
	NA	PS_MIO27_501	GPIO27	GEM0_TXD0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TDI	SPI0_SS2	-	UART0_TX	-	-
	NA	PS_MIO28_501	GPIO28	GEM0_TXD1	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TDO	SPI0_SS1	-	-	UART1_TX	-
	NA	PS_MIO29_501	GPIO29	GEM0_TXD2	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TMS	SPI0_SS0	-	-	UART1_RX	-
	NA	PS_MIO30_501	GPIO30	GEM0_TXD3	-	-	CAN0_RX	-	I2C0_SCL	-	-	SPI0_MISO	-	UART0_RX	-	-
	NA	PS_MIO31_501	GPIO31	GEM0_TX_CTL	-	-	CAN0_TX	-	I2C0_SDA	-	-	SPI0_MIOSI	-	UART0_TX	-	-
	NA	PS_MIO32_501	GPIO32	GEM0_RX_CLK	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SCLK	-	UART1_TX	-
	NA	PS_MIO33_501	GPIO33	GEM0_RXD0	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS2	-	UART1_RX	-
	NA	PS_MIO34_501	GPIO34	GEM0_RXD1	-	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SS1	UART0_RX	-	-
	NA	PS_MIO35_501	GPIO35	GEM0_RXD2	-	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS0	UART0_TX	-	-
	NA	PS_MIO36_501	GPIO36	GEM0_RXD3	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_MISO	-	UART1_TX	-
	NA	PS_MIO37_501	GPIO37	GEM0_RX_CTL	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_MIOSI	-	UART1_RX	-
	NA	PS_MIO76_502	GPIO76	GEM0_MDC	-	SD1_CLK	-	CAN1_TX	-	I2C1_SCL	-	-	-	-	-	-
	NA	PS_MIO77_502	GPIO77	GEM0_MDIO	-	SD1_CD	-	CAN1_RX	-	I2C1_SDA	-	-	-	-	-	-
	NA	PS_MIO12_500	GPIO12	-	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TCK	SPI0_SCLK	-	-	UART1_TX	-
	NA	PS_MIO42_501	GPIO42	GEM1_TXD3	eMMC _DATA1	-	CAN0_RX	-	I2C0_SCL	-	-	SPI0_MISO	-	UART0_RX	-	-
USB2.0	NA	PS_MIO52_502	GPIO52	GEM2_TX_CLK	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TCK	SPI0_SCLK	-	-	UART1_TX	USB0_CLK
	NA	PS_MIO53_502	GPIO53	GEM2_TXD0	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TDI	SPI0_SS2	-	-	UART1_RX	USB0_DIR
	NA	PS_MIO54_502	GPIO54	GEM2_TXD1	-	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TDO	SPI0_SS1	-	UART0_RX	-	USB0_DATA2
	NA	PS_MIO55_502	GPIO55	GEM2_TXD2	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TMS	SPI0_SS0	-	UART0_TX	-	USB0_NXT
	NA	PS_MIO56_502	GPIO56	GEM2_TXD3	-	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-		UART1_TX	USB0_DATA0
	NA	PS_MIO57_502	GPIO57	GEM2_TX_CTL	-	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MIOSI	-		UART1_RX	USB0_DATA1
	NA	PS_MIO58_502	GPIO58	GEM2_RX_CLK	-	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TCK	-	SPI1_SCLK	UART0_RX	-	USB0_STP
	NA	PS_MIO59_502	GPIO59	GEM2_RXD0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TDI	-	SPI1_SS2	UART0_TX	-	USB0_DATA3
	NA	PS_MIO60_502	GPIO60	GEM2_RXD1	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TDO	-	SPI1_SS1	-	UART1_TX	USB0_DATA4
	NA	PS_MIO61_502	GPIO61	GEM2_RXD2	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TMS	-	SPI1_SS0	-	UART1_RX	USB0_DATA5
	NA	PS_MIO62_502	GPIO62	GEM2_RXD3	-	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	USB0_DATA6
	NA	PS_MIO63_502	GPIO63	GEM2_RX_CTL	-	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	USB0_DATA7
Board-to-Board Connector 2 Interfaces from MPSoC PS																

Interface/ Function	B2B Connector Pin Number	Zynq UltraScale+ MPSoC Pin Name	GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13
GEM3	C16	PS_MIO64_502	GPIO64	GEM3_TX_CLK	eMMC _CLK	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_SCLK	-	-	UART1_TX	USB1_CLK
	C17	PS_MIO65_502	GPIO65	GEM3_TXD0	-	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_SS2	-	-	UART1_RX	USB1_DIR
	C18	PS_MIO66_502	GPIO66	GEM3_TXD1	eMMC _CMD	-	CAN0_RX	-	I2C0_SCL	-	-	SPI0_SS1	-	UART0_RX	-	USB1_DATA2
	C19	PS_MIO67_502	GPIO67	GEM3_TXD2	eMMC_DATA0	-	CAN0_TX	-	I2C0_SDA	-	-	SPI0_SS0	-	UART0_TX	-	USB1_NXT
	C20	PS_MIO68_502	GPIO68	GEM3_TXD3	eMMC _DATA1	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-	-	UART1_TX	USB1_DATA0
	C21	PS_MIO69_502	GPIO69	GEM3_TX_CTL	eMMC_DATA2	SD1_WP	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MIOSI	-	-	UART1_RX	USB1_DATA1
	C23	PS_MIO70_502	GPIO70	GEM3_RX_CLK	eMMC _DATA3	SD1_PWR	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SCLK	UART0_RX	-	USB1_STP
	C24	PS_MIO71_502	GPIO71	GEM3_RXD0	eMMC _DATA4	SD1_DATA0	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS2	UART0_TX	-	USB1_DATA3
	C25	PS_MIO72_502	GPIO72	GEM3_RXD1	eMMC _DATA5	SD1_DATA1	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SS1	-	UART1_TX	USB1_DATA4
	C26	PS_MIO73_502	GPIO73	GEM3_RXD2	eMMC _DATA6	SD1_DATA2	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS0	-	UART1_RX	USB1_DATA5
	C27	PS_MIO74_502	GPIO74	GEM3_RXD3	eMMC _DATA7	SD1_DATA3	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	USB1_DATA6
	C28	PS_MIO75_502	GPIO75	GEM3_RX_CTL	eMMC_Reset	SD1_CMD	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	USB1_DATA7
SD1(4-Bit)	C14	PS_MIO44_501	GPIO44	GEM1_RX_CLK	eMMC _DATA3	SD1_WP	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SCLK	-	UART1_TX	-
	B29	PS_MIO45_501	GPIO45	GEM1_RXD0	eMMC _DATA4	SD1_CD	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS2	-	UART1_RX	-
	B21	PS_MIO43_501	GPIO43	GEM1_TX_CTL	eMMC_DATA2	SD1_PWR	CAN0_TX	-	I2C0_SDA	-	-	SPI0_MIOSI	-	UART0_TX	-	-
	B25	PS_MIO46_501	GPIO46	GEM1_RXD1	eMMC _DATA5	SD1_DATA0	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SS1	UART0_RX	-	-
	B26	PS_MIO47_501	GPIO47	GEM1_RXD2	eMMC _DATA6	SD1_DATA1	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS0	UART0_TX	-	-
	B27	PS_MIO48_501	GPIO48	GEM1_RXD3	eMMC _DATA7	SD1_DATA2	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_MISO	-	UART1_TX	-
	B28	PS_MIO49_501	GPIO49	GEM1_RX_CTL	eMMC_Reset	SD1_DATA3	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_MIOSI	-	UART1_RX	-
	B24	PS_MIO50_501	GPIO50	GEM1_MDC	-	SD1_CMD	CAN0_RX	-	I2C0_SCL	-	-	-	-	UART0_RX	-	-
	B23	PS_MIO51_501	GPIO51	GEM1_MDIO	-	SD1_CLK	CAN0_TX	-	I2C0_SDA	-	-	-	-	UART0_TX	-	-
CAN0	D30	PS_MIO07_500	GPIO7				CAN0_TX		I2C0_SDA				SPI1_SS2		UART0_TX	
	D29	PS_MIO06_500	GPIO6				CAN0_RX		I2C0_SCL				SPI1_SCLK		UART0_RX	
UART1	D23	PS_MIO08_500	GPIO8	-	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SS1	-	UART1_TX	-
	D24	PS_MIO09_500	GPIO9	-	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS0	-	UART1_RX	-
I2C0	C9	PS_MIO11_500	GPIO11	-	-	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	-
	C8	PS_MIO10_500	GPIO10	NFC_RB_N	-	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	-
I2C1	C11	PS_MIO25_500	GPIO25	NFC_RE_N	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	-	-	UART1_RX	-
	C10	PS_MIO24_500	GPIO24	NFC_DATA7	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	-	-	UART1_TX	
JTAG	A12	PS_JTAG_TDI	-	PS_JTAG_TDI	-	-	-	-	-	-	-	-	-	-	-	-
	A10	PS_JTAG_TMS	-	PS_JTAG_TMS	-	-	-	-	-	-	-	-	-	-	-	-
	A9	PS_JTAG_TCK	-	PS_JTAG_TCK	-	-	-	-	-	-	-	-	-	-	-	-
	A11	PS_JTAG_TDO	-	PS_JTAG_TDO	-	-	-	-	-	-	-	-	-	-	-	-
QSPI0	NA	PS_MIO0_500	GPIO0	QSPI_SCLK	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TCK	SPI0_SCLK	-	-	UART1_TX	-
	NA	PS_MIO3_500	GPIO3	QSPI_SS0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TMS	SPI0_SS0	-	UART0_TX	-	-
	NA	PS_MIO4_500	GPIO4	QSPI_DQ0	-	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-	-	UART1_TX	-
	NA	PS_MIO5_500	GPIO5	QSPI_CS	-	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MOSI	-	-	UART1_RX	-
	NA	PS_MIO1_500	GPIO1	QSPI_MISO	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TDI	SPI0_SS2	-	-	UART1_RX	
	NA	PS_MIO2_500	GPIO2	QSPI_DQ2			CAN0_RX		I2C0_SCL		PJTAG_TDO	SPI0_SS2				
Debug UART (UART0)	A14	PS_MIO38_501	GPIO38	GEM1_TX_CLK	eMMC _CLK	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TCK	SPI0_SCLK	-	UART0_RX	-	-
	A13	PS_MIO39_501	GPIO39	GEM1_TXD0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TDI	SPI0_SS2	-	UART0_TX	-	-
CAN1	D28	PS_MIO40_501	GPIO40	GEM1_TXD1	eMMC _CMD	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TDO	SPI0_SS1	-	-	UART1_TX	-
	D27	PS_MIO41_501	GPIO41	GEM1_TXD2	eMMC_DATA0	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TMS	SPI0_SS0	-	-	UART1_RX	-

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM.

Table 9: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_5V[1]	4.75V	5V	5.25V	±50mV
2	VRTC_3V0[2]	0V	3V	3.15V	±20mV

[1] Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM is designed to work with VCC_5V input power rail from Board-to-Board Connector 2.

[2] Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM uses this voltage as backup power source to PMIC RTC when VCC_5V is off. This is an optional power and required only if RTC functionality is used.

3.1.2 Power Output Specification

The Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM provides and extension of HP Bank and HD Bank I/O Supply voltage to the Board-to-Board Connectors for various uses like IO Level shifting etc.

Table 10: Power Output Specification

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Output Current
To Board-to-Board Connector1					
1	VCCO_HD44	1.2V	1.8V	3.3V	40mA
2	VCCO_HP65	1V	1.8V	1.8V	40mA
3	VCCO_HP66	1V	1.8V	1.8V	40mA
To Board-to-Board Connector2					
1	VCCO_HD45	1.2V	1.8V	3.3V	40mA

3.1.3 Power Input Sequencing

The Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM Power Input sequence requirement is explained below.

Power up Sequence:

- VRTC_3V0 must come up at the same time or before VCC_5V comes up.
- SOMPWR_EN signal from Board-to-Board Connector 2 must be high at the same time or after VCC_5V comes up.

Power down Sequence:

- SOMPWR_EN signal from Board-to-Board Connector 2 must be low at the same time or before VCC_5V goes down.
- VCC_5V must go down at the same time or before VRTC_3V0 goes down.

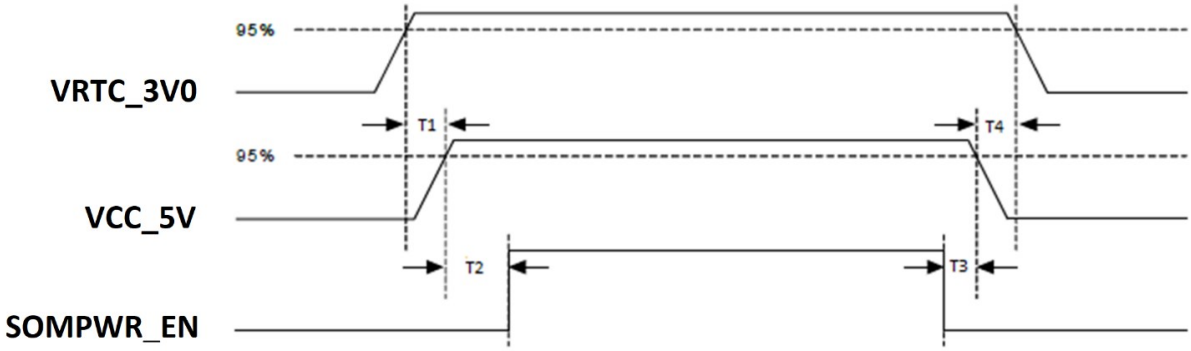

Figure 8: Power Input Sequencing

Table 11: Power Sequence Timing

Item	Description	Value
T1	VRTC_3V0[1] rise time to VCC_5V rise time	≥ 0 ms
T2	VCC_5V rise time to SOMPWR_EN rise time	≥ 0 ms
T3	SOMPWR_EN fall time to VCC_5V fall time	≥ 0 ms
T4	VCC_5V fall time to VRTC_3V0 fall time	≥ 0 ms

[1] VRTC_3V0 is the RTC Battery backup supply. This is an optional power.

Important Note: Make sure that from the carrier board IOs shall not driving before all the SOM powers are stable.

3.1.4 Power Consumption

For more accurate power estimation, iWave recommends to use Xilinx Power Estimator (XPE) tool and calculate the MPSoC power.

For reference, we have calculated the Zynq Ultrascale+ MPSoC (ZU5/4/3T/3/2/1) SOM Theoretical Power Estimation by using Xilinx Power Estimator (XPE) tool with various FPGA utilisation and ambient temperature as shown below.

FPGA Utilisation (%)	SOM Theoretical Power Estimation @ 5V	
	ZU5EV -3	
	25°C Ambient	60°C Ambient
25	5.742A/28.711W	6.025A/30.126W
50	6.204A/31.018W	6.872A/34.358W
80	6.978A/34.891W	7.628A/38.138W
100	7.436A/37.178W	8.225A/41.127W

Note: This calculation is done considering ZU5EV -3 Speed grade MPSoC.

3.2 Environmental Characteristics

3.2.1 Temperature Specification

The below table provides the Environment specification of Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM.

Table 12: Temperature Specification

Parameters	Min	Max
Operating temperature range - Industrial[1]	-40°C	85°C
Operating temperature range - Extended[1]	0°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.2.2 RoHS2 Compliance

iWave's Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM is designed by using RoHS2 compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.3 MechanicalCharacteristics

3.3.1 Zynq UltraScale+ MPSoC SOM Mechanical Dimensions

Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM PCB size is 60mm x 50mm x 2mm. SOM mechanical dimension is shown below.

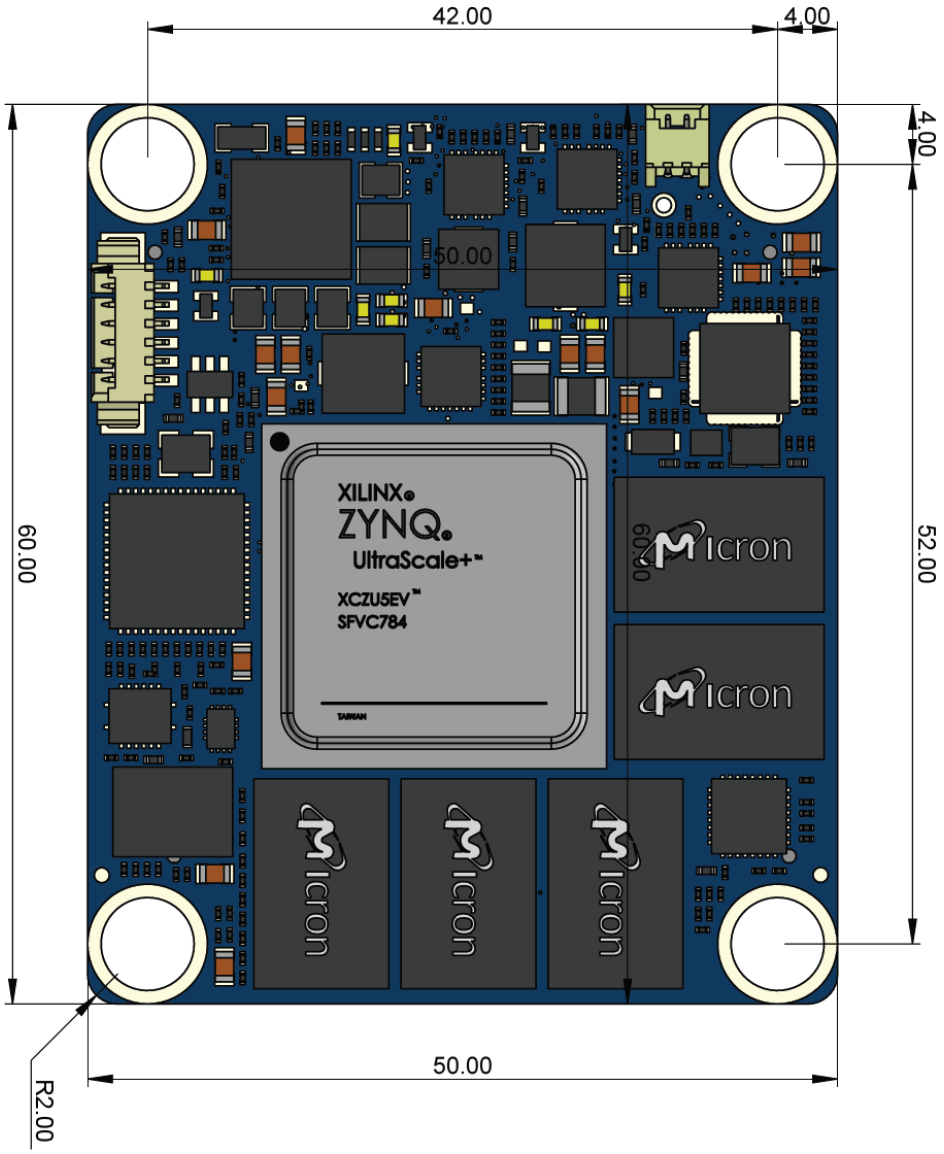

Figure 9: Mechanical dimension of Zynq UltraScale+ MPSoC SOM - Top View

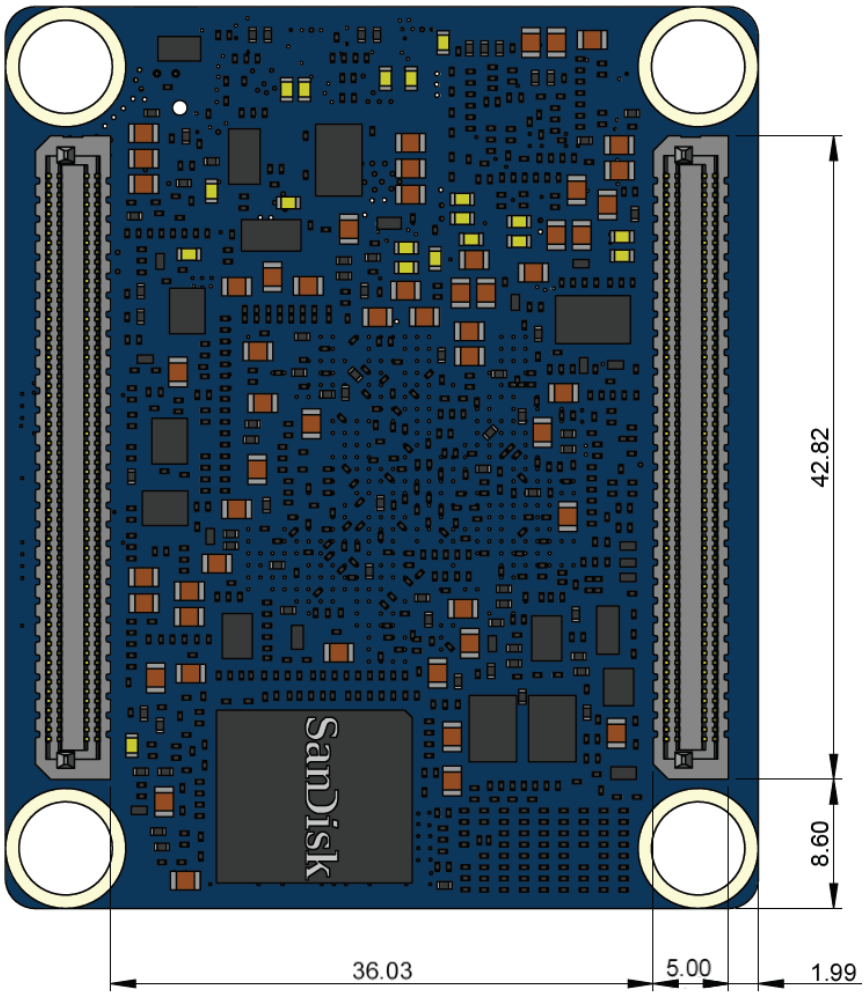

Figure 10: Mechanical dimension of Zynq UltraScale+ MPSoC SOM - Bottom View

Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) PCB thickness is 2.00mm±0.1mm, top side maximum height component is inductors L3 & L10 (4.3mm) and bottom side maximum height component is Board-to-Board connector 1 & 2 (4.02mm). Please refer the below figures which gives height details of the Zynq UltraScale+ MPSoC SOM.

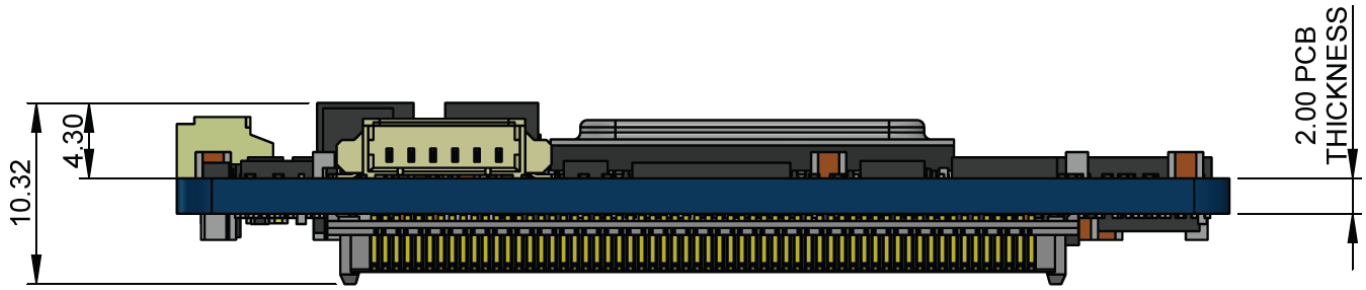

Figure 11:Mechanical dimension of Zynq UltraScale+ MPSoC SOM – Top Max. Heighted Component

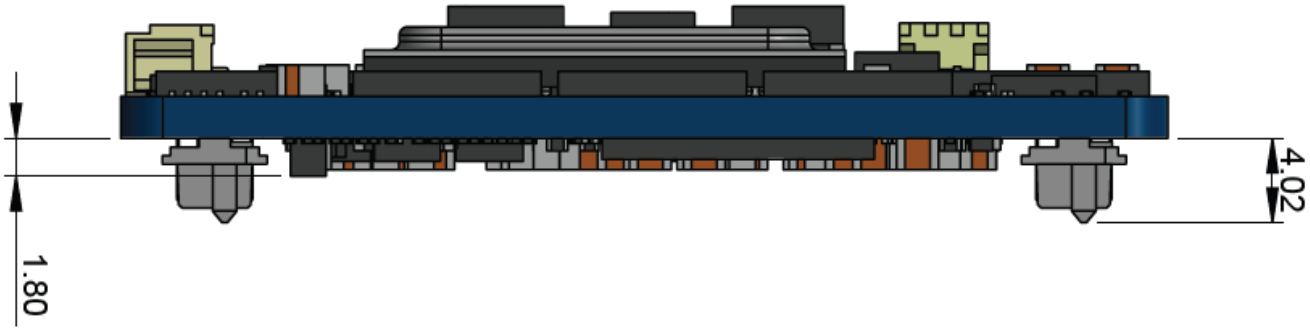

Figure 12: Mechanical dimension of Zynq UltraScale+ MPSoC SOM – Bottom Max. Heighted Component

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 13: Orderable Product Part Numbers

Product Part Number	Description	Temperature
ZU5 MPSoC based SOM		
iW-G36M-5EV1-4D004G-E016G-BEA	ZU5EV (-1) MPSOC, 4GB PS DDR4, 2GB PL DDR4, 16GB EMMC, extended	0°C - 100°C
ZU4 MPSoC based SOM		
iW-G36M-4EV1-4D004G-E016G-BEA	ZU4EV (-1) MPSOC, 4GB PS DDR4, 2GB PL DDR4, 16GB EMMC, extended	0°C - 100°C
ZU3T MPSoC based SOM		
iW-G36M-3TC1-4D004G-E016G-BEA	ZU3TCG (-1) MPSOC, 4GB PS DDR4, 16GB EMMC, extended	0°C - 100°C
ZU3 MPSoC based SOM		
iW-G36M-3EG1-4D004G-E016G-BIA	ZU3EG (-1) MPSOC, 4GB PS DDR4, 16GB EMMC, Industrial	-40°C - 85°C
ZU2 MPSoC based SOM		
iW-G36M-2CG1-4D004G-E016G-BEA	ZU2CG (-1) MPSOC, 4GB PS DDR4 16GB EMMC, extended	0°C - 100°C
ZU1 MPSoC based SOM		
TBD	TBD	TBD
TBD	TBD	TBD

5. APPENDIX

5.1 Zynq UltraScale+ MPSoC SOM Development Platform

iWave Systems supports iW-RainboW-G36D – Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM Development Platform which is targeted for quick validation of Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) based SOM. iWave's Zynq UltraScale+ MPSoC Development Board incorporates Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM and High-performance Carrier board with complete BSP support.

For more details on Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM Development Platform, visit the below web link.

https://www.iwavesystems.com/product/zynq-ultrascale-mpsoc-zu5-zu4-zu3t-zu3-zu2-zu1-system-on-module/#development-kit

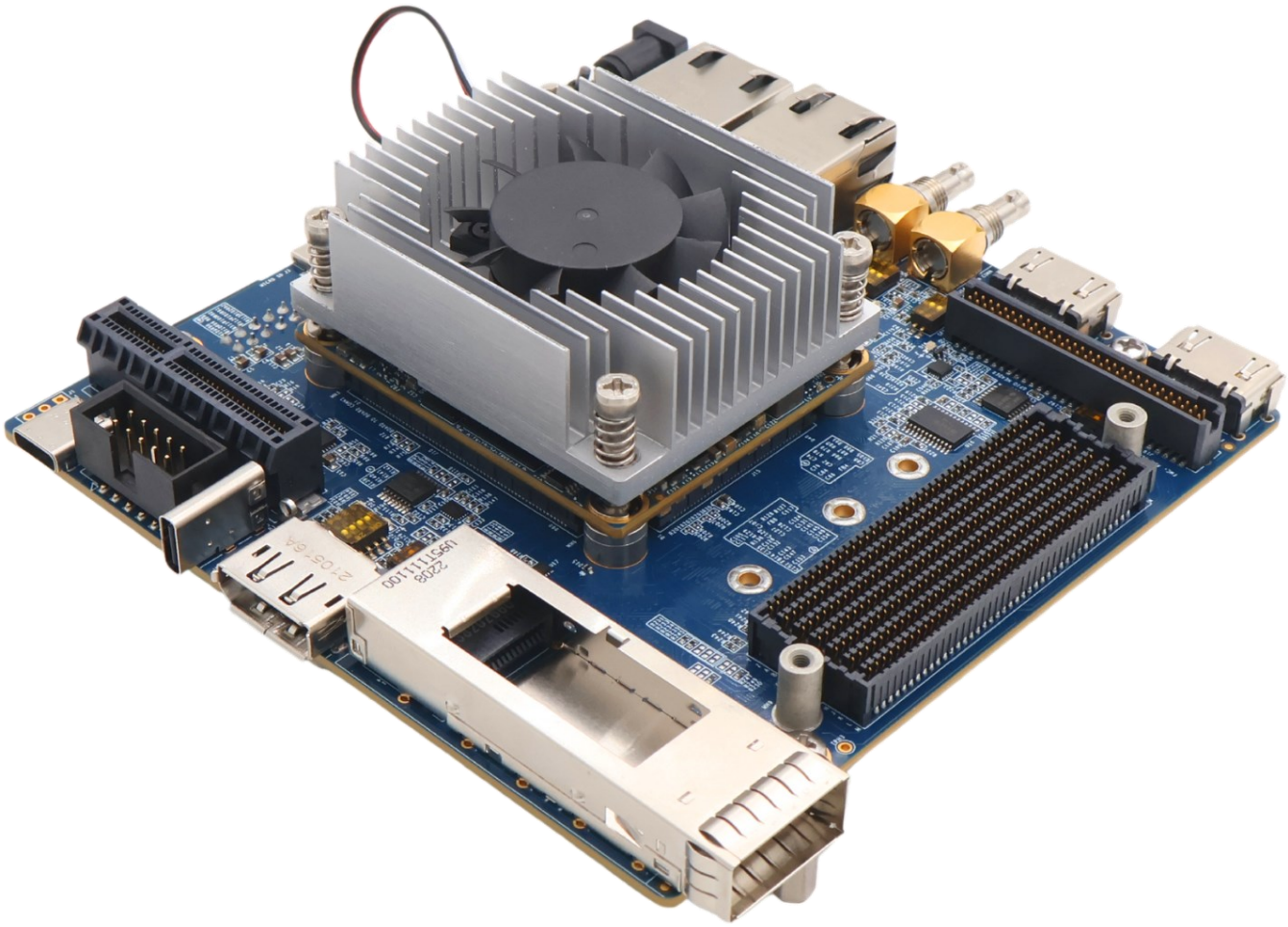

Figure 13: Zynq UltraScale+ MPSoC (ZU5/4/3T/3/2/1) SOM Development Platform

5.2 Bank Migration Info

The Zynq UltraScale+ MPSoC SOM contains two board-to-board connectors supporting a highspeed transceiver bank, high-performance IOs, and interfaces to the carrier board. The Zynq UltraScale+ MPSoC SOM supports several compatible MPSoCs with SFVC784 package and accommodates all speed grades MPSoC chips.

The supported high-speed transceiver limit is mentioned in the below table.

Zynq US+ MPSoC Speed Grade	GTH Transceiver line rate (min)	GTH Transceiver line rate (max)
-1LI Speed Grade	0.5Gb/s	10.3125Gb/s
-1 Speed Grade	0.5Gb/s	12.5Gb/s
-2 Speed Grade		
-3 Speed Grade		

The Zynq UltraScale+ MPSoC SOM offers support for a range of MPSoCs - ZU5, ZU4, ZU3T, ZU3, ZU2, and ZU1 (SFVC784 Package). Given the extensive coverage of MPSoCs, detailed bank migration information is provided below for seamless transition between these variants.

Table 14: Bank Migration Info

Device	ZU5	ZU4	ZU3T	ZU3	ZU2	ZU1
Board-to-Board Connector 1	HP-66	HP-66	HP-66	HP-66	HP-66	HP-66
	HP-65	HP-65	NA	HP-65	HP-65	HP-65
	HD-43	HD-43	NA	HD-44	HD-44	HD-44
	HD-44	HD-44	HD-44	HD-24	HD-24	NA
	HD-45	HD-45	HD-45	HD-25	HD-25	NA
Board-to-Board Connector 2	HD-43	HD-43	NA	HD-44	HD-44	HD-44
	HD-46	HD-46	HD-46	HD-26	HD-26	NA
	GTH-224	GTH-224	GTH-224	NA	NA	NA


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