

### Driver Characteristics

Parameter	Rating	Units
$V_{\text{OFFSET}}$	600	V
$I_{\text{O } \pm}$ (Source/Sink)	1.4 / 1.8	A
$V_{\text{BIAS}}$	10-20	V

### Features

- Floating Channel for Bootstrap Operation to +600V with an Absolute Maximum Rating of +700V
- Programmable Dead-Time
- Outputs Can Source 1.4A and Sink 1.8A
- Gate Drive Supply Range From 10V to 20V
- Tolerant to Negative Voltage Transients: dV/dt Immune
- 3.3V and 5V Logic Compatible
- Undervoltage Lockout for Both High-side and Low-Side Outputs
- Matched Propagation Delays

### Applications

- Switch Mode Power Supply
- Motor Driver Inverter
- DC/DC Converter
- Uninterruptible Power Supplies (UPS)

### Description

The IX21844 is a high voltage IC that can drive high speed MOSFETs and IGBTs that operate up to +600V. The IX21844 is configured with dependent high-side and low side referenced output channels which can source 1.4A and sink 1.8A. The floating high-side channel can drive an N-channel power MOSFET or IGBT 600V from the common reference.

Manufactured on IXYS Integrated Circuits Division's proprietary high-voltage BCDMOS on SOI (silicon on isolator) process, the IX21844 is extremely robust and virtually immune to negative transients. The UVLO circuit prevents the turn-on of the MOSFET or IGBT until there is sufficient  $V_{\text{BS}}$  or  $V_{\text{CC}}$  supply voltage. A programmable dead-time can be set between 400ns and 5 $\mu$ s to insure that both the high-side and low-side power MOSFET or IGBT are not enabled at the same time. Propagation delays are matched for use in high frequency applications.

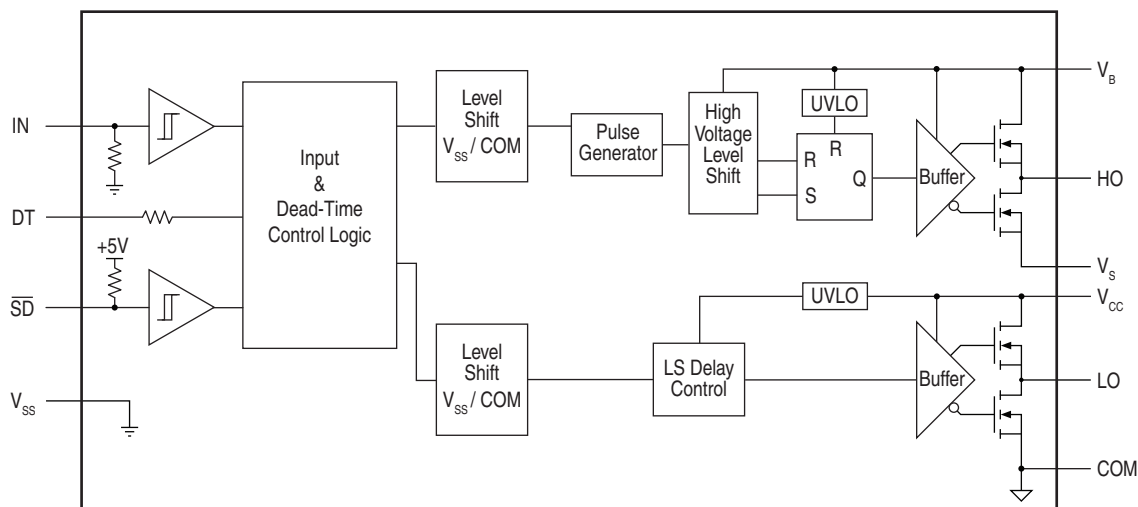
The IX21844 is available in 14-pin DIP and 14-pin SOIC (narrow body) packages. The 14-pin SOIC (narrow body) package is also available in tape & reel.

### Ordering Information

Part	Description
IX21844G	14-Pin DIP (25/Tube)
IX21844N	14-Pin SOIC (Narrow Body) (50/Tube)
IX21844NTR	14-Pin SOIC (Narrow Body) (2000/Reel)



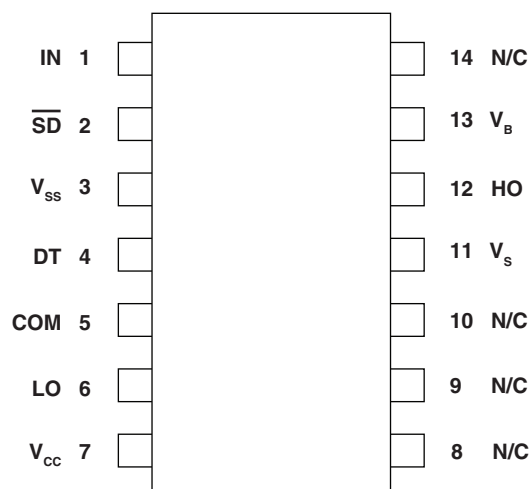
### IX21844 Functional Block Diagram



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## 1 Specifications

### 1.1 Package Pinout



### 1.2 Pin Description (DIP & SOIC)

Pin#	Name	Description
1	IN	Logic input for both high-side gate drive output (HO) and low-side gate drive output (LO). In phase with HO.
2	SD	Shut-down logic input. Active low.
3	V <sub>ss</sub>	Logic ground
4	DT	Programmable Dead-Time input
5	COM	Low-side return
6	LO	Low-side gate drive output
7	V <sub>cc</sub>	Low-side and logic supply
8	N/C	No connection
9	N/C	No connection
10	N/C	No connection
11	V <sub>s</sub>	High-side floating supply return
12	HO	High-side gate drive output
13	V <sub>b</sub>	High-side floating supply
14	N/C	No connection

### 1.3 Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM.

Parameter	Symbol	Min	Max	Units
High-Side Floating Absolute Voltage	$V_B$	-0.3	700	V
High-Side Floating Supply Offset Voltage	$V_S$	$V_B-20$	$V_B+0.3$	
High-Side Floating Output Voltage	$V_{HO}$	$V_S-0.3$	$V_B+0.3$	
Low-Side and Logic Fixed Supply Voltage	$V_{CC}$	-0.3	20	
Low-Side Output Voltage	$V_{LO}$	-0.3	$V_{CC}+0.3$	
Programmable Dead-Time Pin Voltage	DT	$V_{SS}-0.3$	$V_{CC}+0.3$	
Logic Input Voltage	$V_{IN}, V_{SD}$	$V_{SS}-0.3$	$V_{CC}+0.3$	
Logic ground	$V_{SS}$	$V_{CC}-20$	$V_{CC}+0.3$	
Allowable Offset Supply Voltage Transient	$dV_S/dt$	-	50	V/ns
Package Power Dissipation @ $T_A = 25^\circ\text{C}$	14-Pin PDIP	PD	1.6	W
	14-Pin SOIC		1	
Thermal Resistance, Junction to Ambient	14-Pin PDIP	$R_{\theta JA}$	75	$^\circ\text{C/W}$
	14-Pin SOIC		120	
Junction Temperature	$T_J$	-	150	$^\circ\text{C}$
Storage Temperature	$T_S$	-50	150	
Lead Temperature (Soldering, 10 Seconds)	$T_L$	-	300	

### 1.4 Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. The  $V_S$  and  $V_{SS}$  offset ratings are tested with all supplies biased at a 15V differential.

Parameter	Symbol	Min	Max	Units
High-Side Floating Supply Absolute Voltage	$V_B$	$V_S+10$	$V_S+20$	V
High-Side Floating Supply Offset Voltage	$V_S$	-5	600	
High-Side Floating Output Voltage	$V_{HO}$	$V_S$	$V_B$	
Low-Side and Logic Fixed Supply Voltage	$V_{CC}$	10	20	
Low-Side Output Voltage	$V_{LO}$	0	$V_{CC}$	
Logic Input Voltage	$V_{IN}, V_{SD}$	$V_{SS}$	$V_{SS} + 5$	
Programmable Dead-Time Pin Voltage	DT	$V_{SS}$	$V_{CC}$	
Logic Ground	$V_{SS}$	-5	5	
Ambient Temperature	$T_A$	-40	+125	$^\circ\text{C}$

### 1.5 Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ )=15V,  $V_{SS}$ =COM,  $DT=V_{SS}$ , and  $T_A=25^\circ\text{C}$  unless otherwise specified. The  $V_{IL}$ ,  $V_{IH}$ , and  $I_{IN}$  parameters are referenced to  $V_{SS}$ /COM and are applicable to the respective input leads: IN and  $\overline{SD}$ .  $V_O$  and  $I_O$  are referenced to COM and are applicable to the respective output leads: HO and LO.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Logic "1" Input Voltage	$V_{CC}=10\text{V to }20\text{V}$	$V_{IH}$	2	-	-	V
Logic "0" Input Voltage		$V_{IL}$	-	-	0.8	
SD Input Positive Going Threshold		$V_{SD,TH+}$	2	-	-	
SD Input Negative Going Threshold		$V_{SD,TH-}$	-	-	0.8	
High Level Output Voltage, $V_{BIAS} - V_O$	$I_O=0\text{A}$	$V_{OH}$	-	-	2.5	V
Low Level Output Voltage, $V_O$	$I_O=20\text{mA}$	$V_{OL}$	-	-	0.2	
Offset Supply Leakage Current	$V_B=V_S=600\text{V}$	$I_{LK}$	-	33	60	$\mu\text{A}$
Quiescent $V_{BS}$ Supply Current	$V_{IN}=0\text{V or }5\text{V}$	$I_{QBS}$	20	87	150	
Quiescent $V_{CC}$ Supply Current		$I_{QCC}$	0.4	1.8	2.2	$\text{mA}$
Logic "1" Input Bias Current	$IN=5\text{V}$	$I_{IN+}$	-	35	60	$\mu\text{A}$
Logic "0" Input Bias Current	$IN=0\text{V}$	$I_{IN-}$	-	-	1	
SD Logic "1" Input Bias Current	$V_{SD}=5\text{V}$	$I_{SD+}$	-	-	30	$\mu\text{A}$
SD Logic "0" Input Bias Current	$V_{SD}=0\text{V}$	$I_{SD-}$	-	15	60	$\mu\text{A}$
$V_{CC}$ and $V_{BS}$ Supply Under-voltage Positive Going Threshold	-	$V_{CCUV+}$ $V_{BSUV+}$	8	8.6	9.8	V
$V_{CC}$ and $V_{BS}$ Supply Under-voltage Negative Going Threshold		$V_{CCUV-}$ $V_{BSUV-}$	7.4	7.9	9	
Hysteresis		$V_{CCUVH}$ $V_{BSUVH}$	0.3	0.7	-	
Output High Short Circuit Pulsed Current	$V_O=0\text{V}$ , $PW \leq 10\mu\text{s}$	$I_{O+}$	1.4	2.2	-	A
Output Low Short Circuit Pulsed Current	$V_O=15\text{V}$ , $PW \leq 10\mu\text{s}$	$I_{O-}$	1.8	2.5	-	

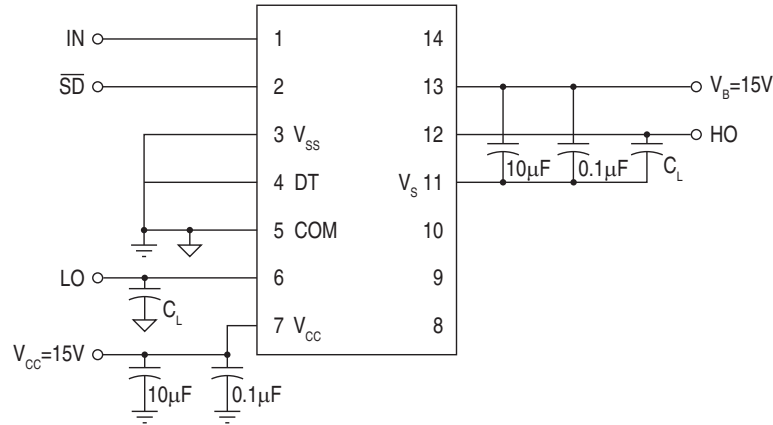
### 1.6 Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ )=15V,  $C_L=1000\text{pF}$ ,  $T_A=25^\circ\text{C}$ ,  $DT=V_{SS}$ , and  $V_{SS}$ =COM unless otherwise specified.

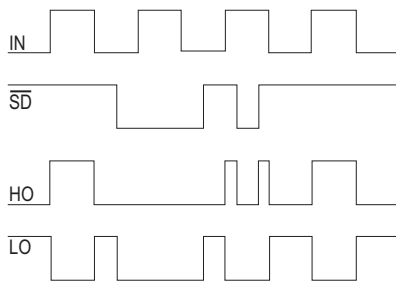
Parameter	Conditions	Symbol	Min	Typ	Max	Units
Turn-On Propagation Delay	$V_S=0\text{V}$	$t_{on}$	-	560	900	ns
Turn-Off Propagation Delay	$V_S=0\text{V or }600\text{V}$	$t_{off}$	-	200	400	
Shutdown propagation Delay	-	$t_{SD}$	-	225	400	
Delay Matching, HS & LS Turn-on		$MT_{on}$	-	0	90	
Delay Matching, HS & LS Turn-off		$MT_{off}$	-	0	40	
Turn-On Rise Time	$V_S=0\text{V}$	$t_r$	-	23	60	
Turn-Off Fall Time		$t_f$	-	14	35	$\mu\text{s}$
Dead-Time: LO Turn-off to HO Turn-on ( $DT_{LO-HO}$ )	$R_{DT}=0\Omega$	DT	280	355	520	
& HO Turn-off to LO Turn-on ( $DT_{HO-LO}$ )	$R_{DT}=200\text{k}\Omega$		4	5	6	ns
Dead-Time Matching: ( $DT_{LO-HO}$ ) - ( $DT_{HO-LO}$ )	$R_{DT}=0\Omega$	MDT	-	0	50	
	$R_{DT}=200\text{k}\Omega$		-	0	600	

## 1.7 Test Waveforms

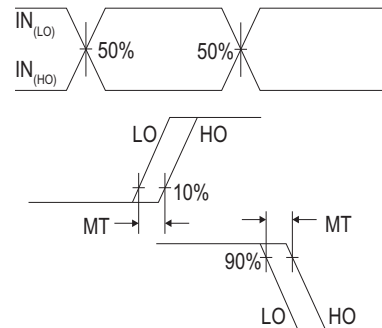
### 1.7.1 Switching Time Test Circuit



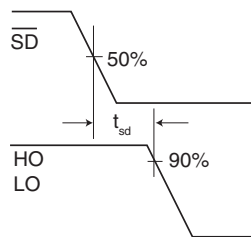
### 1.7.2 Input/Output Timing Diagram



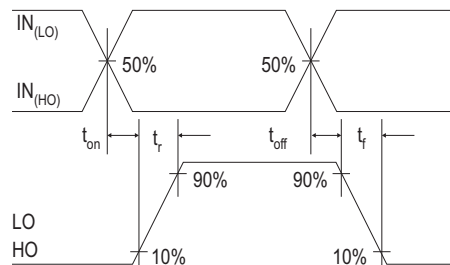
### 1.7.5 Delay Matching Waveform Definitions



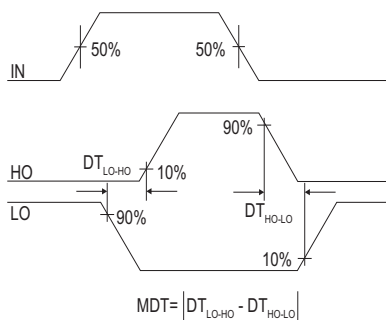
### 1.7.3 Shutdown Waveform Definition



### 1.7.6 Switching Time Waveform Definitions



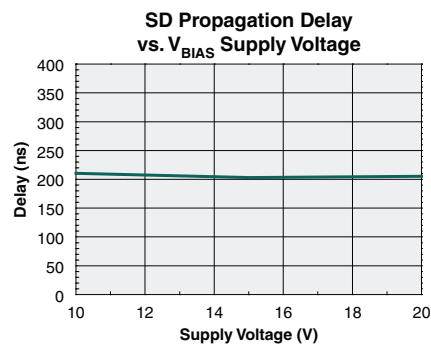
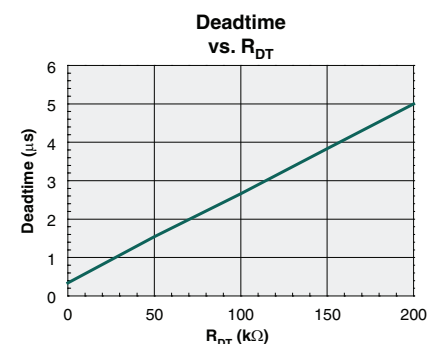
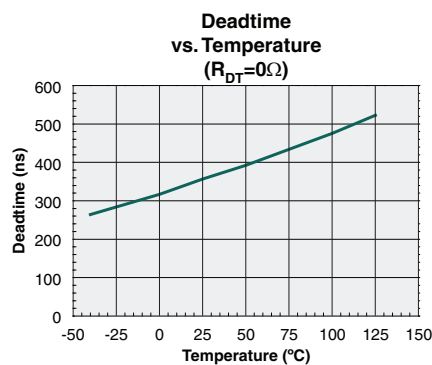
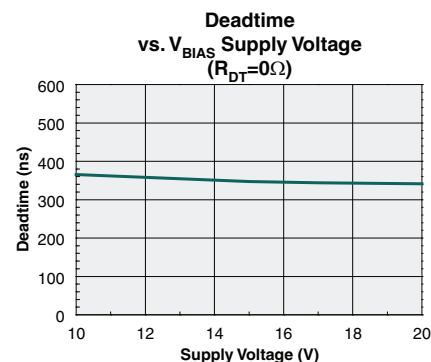
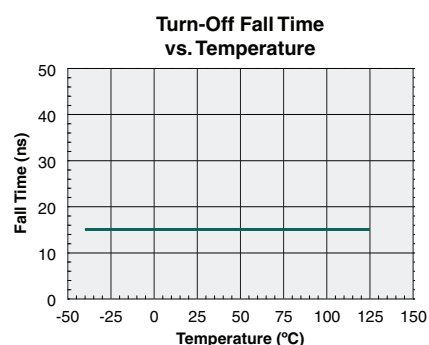
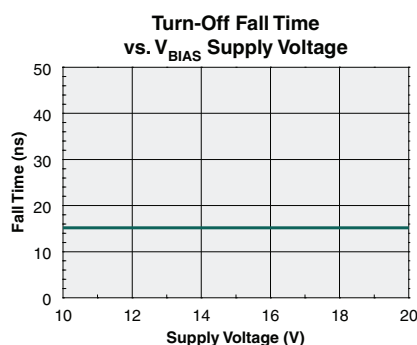
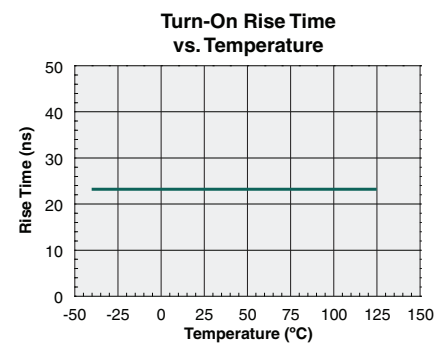
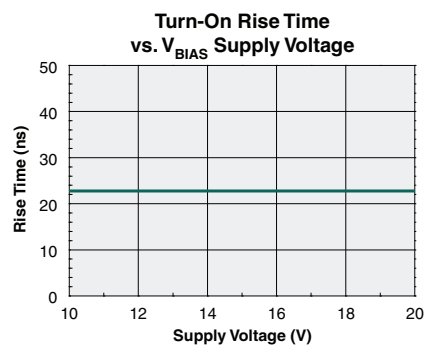
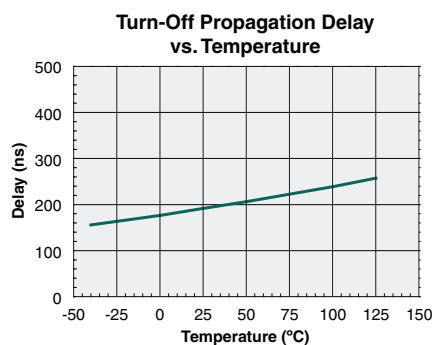
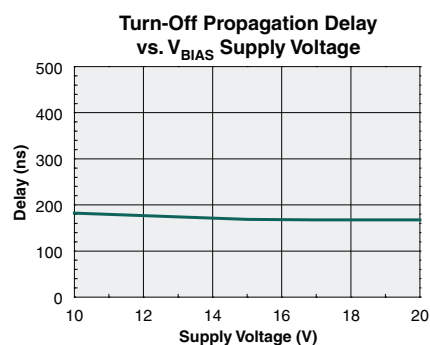
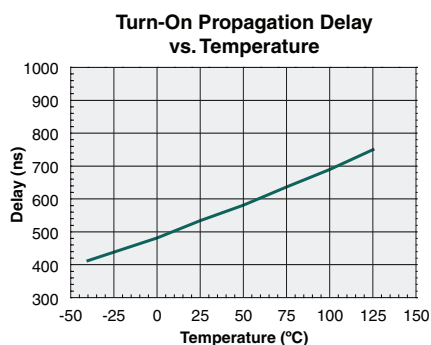
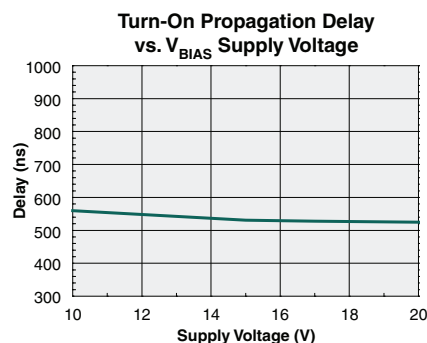
### 1.7.4 Dead-Time Waveform Definition

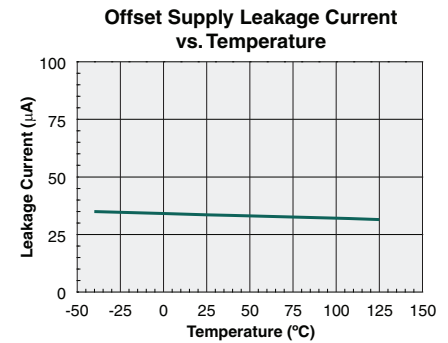
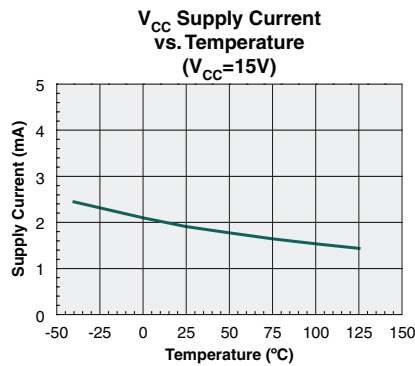
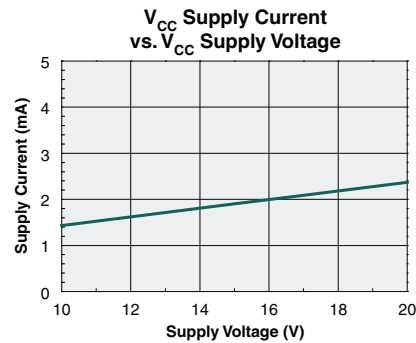
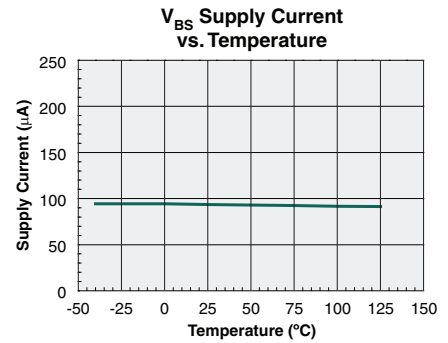
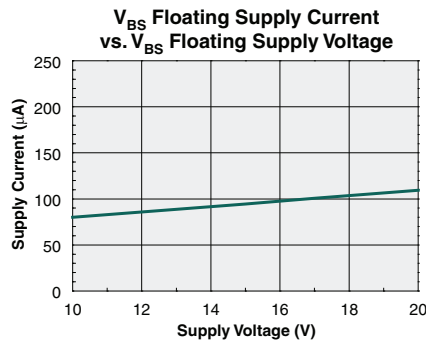
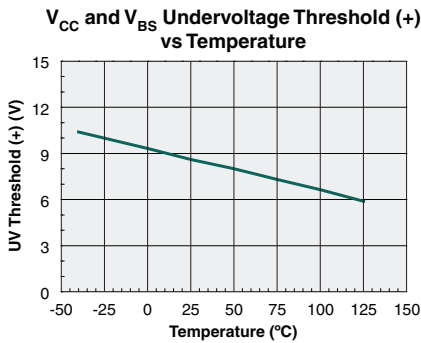
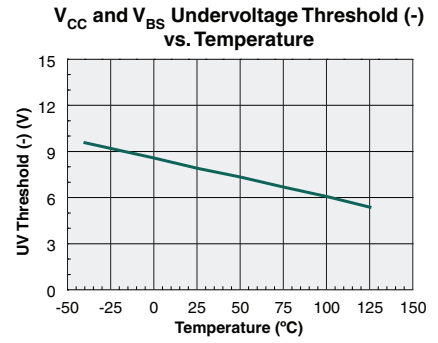
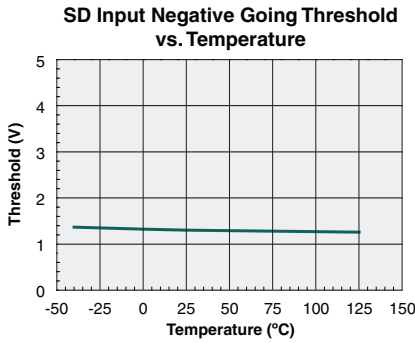
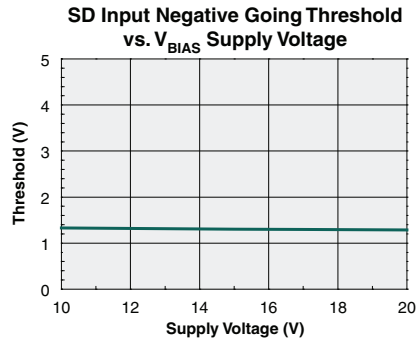
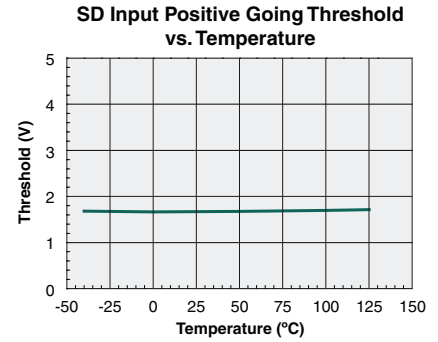
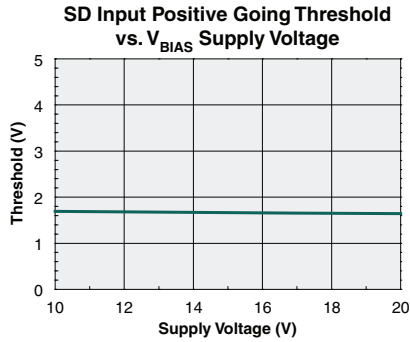
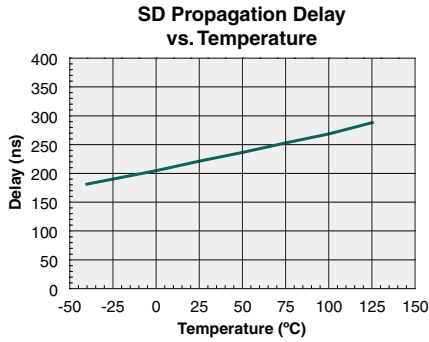


### 1.7.7 Truth Table

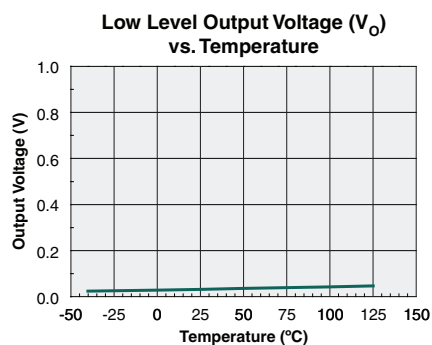
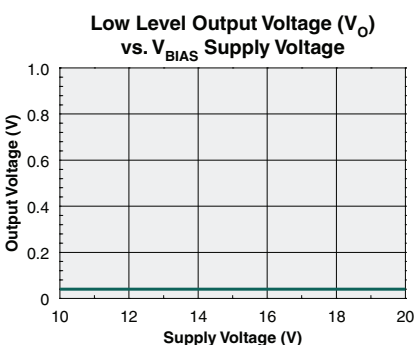
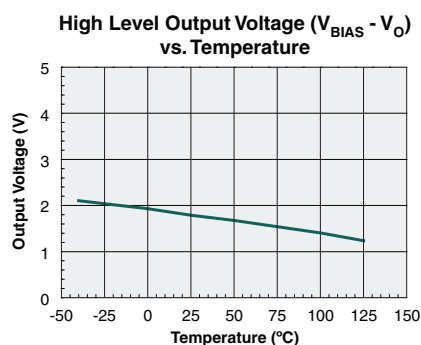
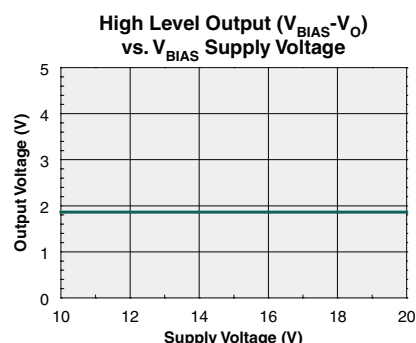
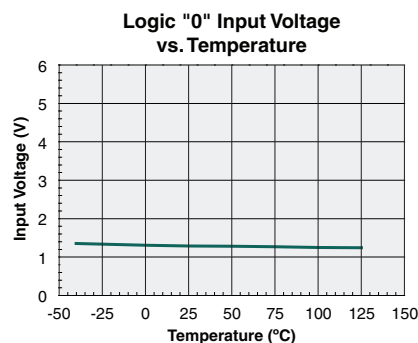
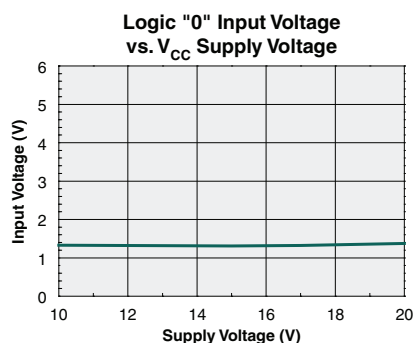
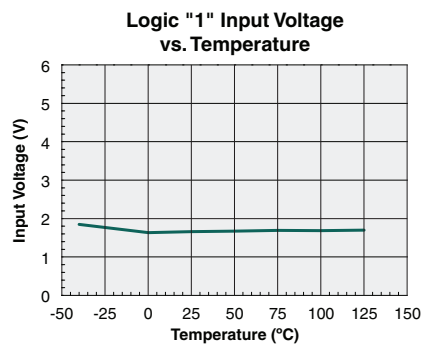
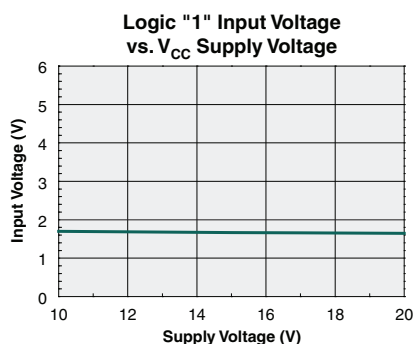
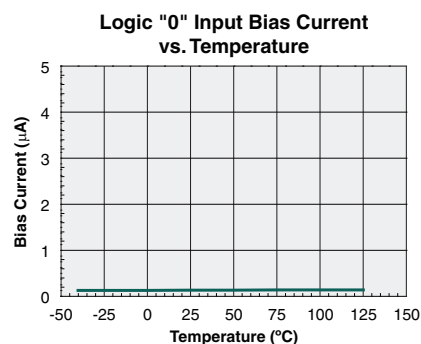
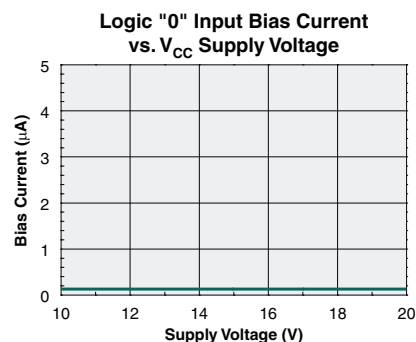
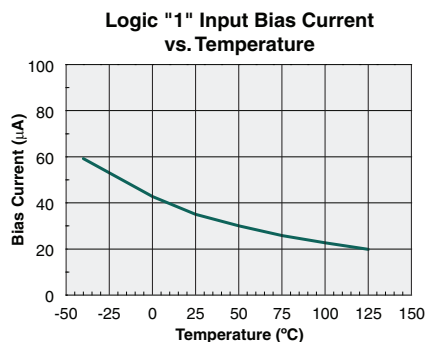
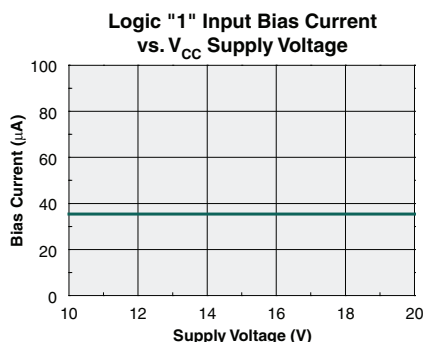
IN	$\overline{SD}$	HO	LO
1	1	H	L
0	1	L	H
X	0	L	L

## 2 Performance Characteristics









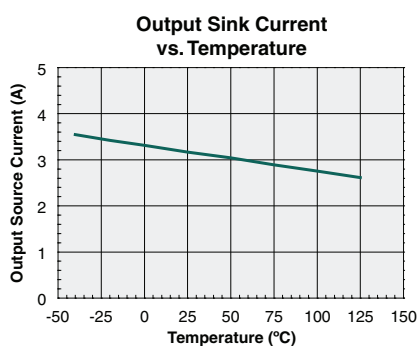
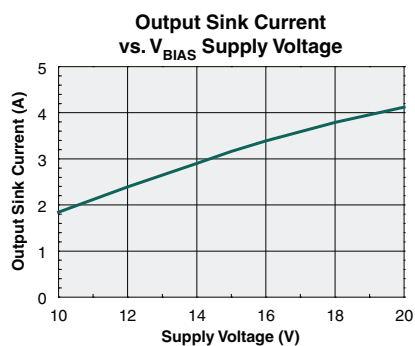
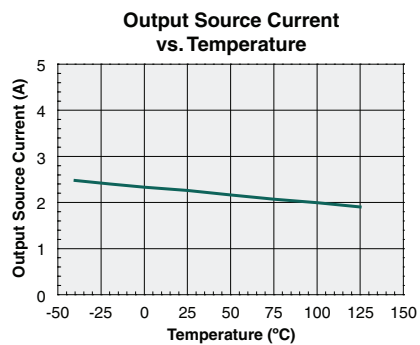
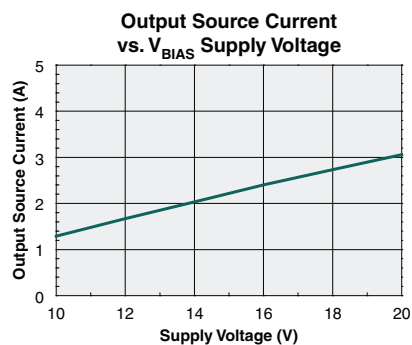
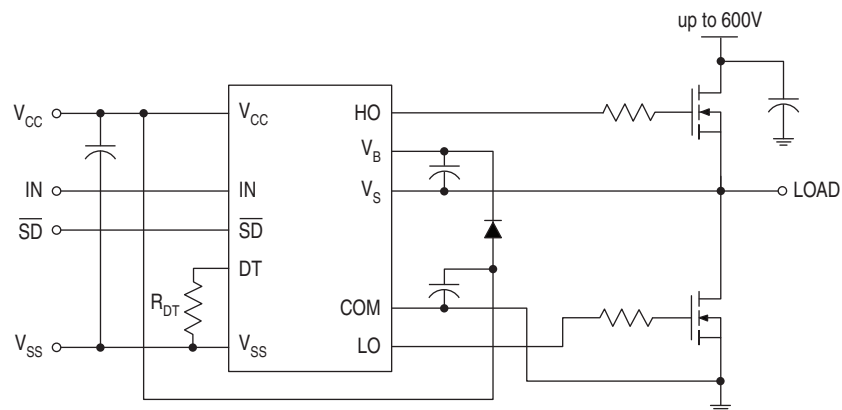


Figure 1. Typical Connection Diagram



### 3 Manufacturing Information

#### 3.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. IXYS Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
IX21844G / IX21844N	MSL 1

#### 3.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

#### 3.3 Reflow Profile

This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

Device	Maximum Temperature x Time
IX21844G (DIP)	245°C for 30 seconds
IX21844N (SOIC)	260°C for 30 seconds

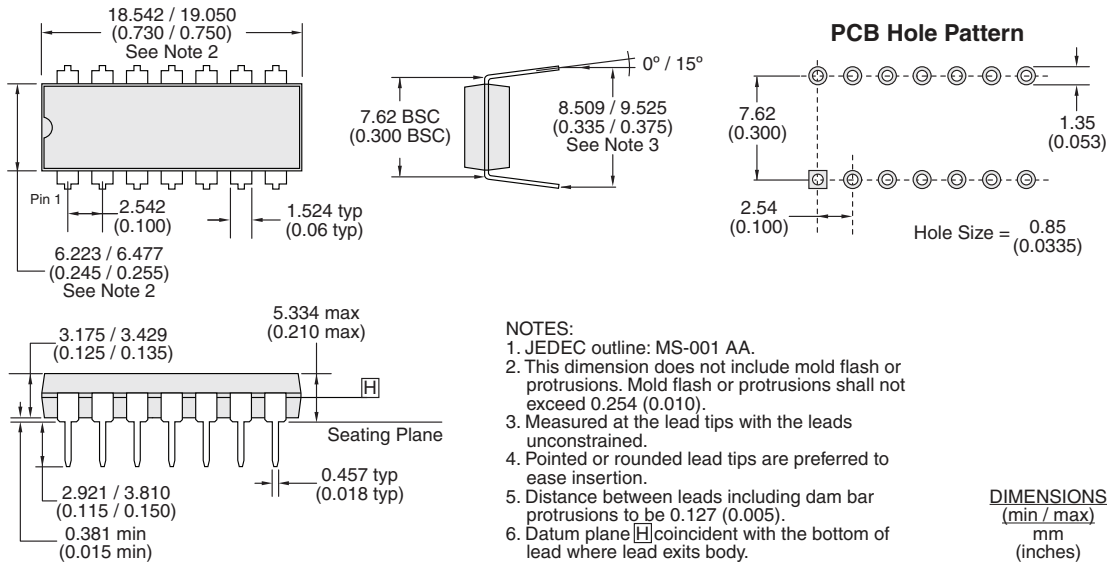
#### 3.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable, and the use of a short drying bake may be necessary. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.

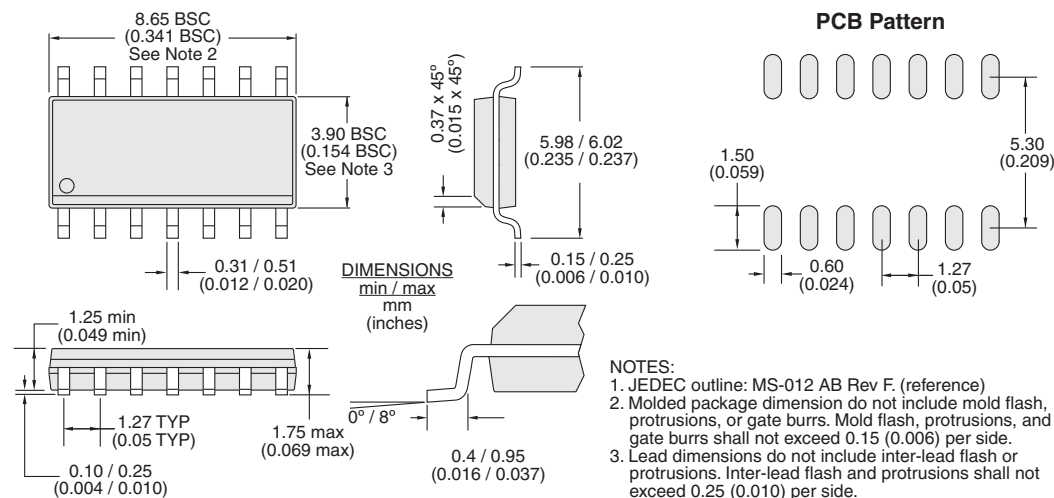


### 3.5 Mechanical Dimensions

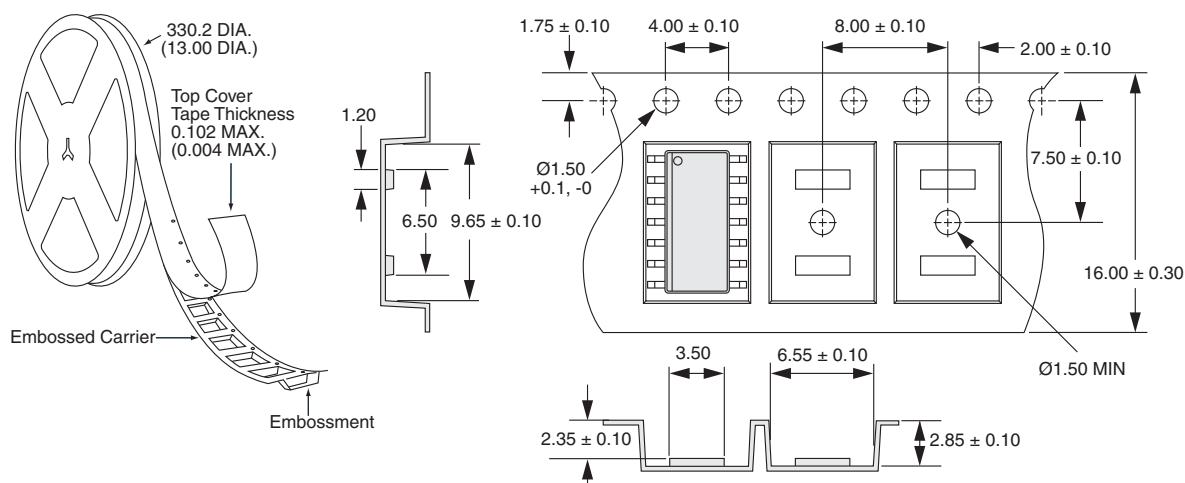
#### 3.5.1 IX21844G 14-Pin DIP Package



#### 3.5.2 IX21844N 14-Pin SOIC (Narrow Body) Package



### 3.5.3 IX21844NTR Tape & Reel Packaging



**NOTES:**

1. All dimensions in millimeters
2. 10 sprocket hole pitch cumulative tolerance ± 0.20.
3. Carrier camber is within 1mm in 250mm.
4. Tape material : Black Conductive Polystyrene Alloy.
5. All dimensions meet EIA-481-C requirements.
6. Thickness : 0.30 ± 0.05mm.

**For additional information please visit our website at: [www.ixysic.com](http://www.ixysic.com)**

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