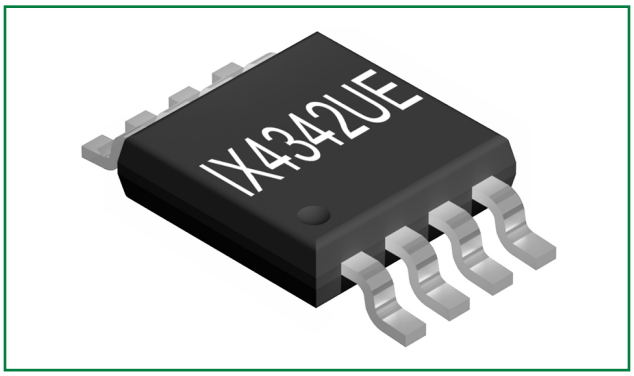
IX4342

5A Dual, One Inverting & One Non-Inverting, Low-Side MOSFET Driver



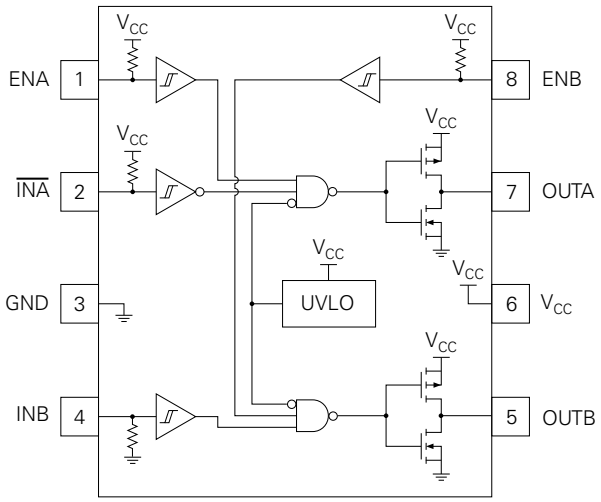
Features

- Two Independent Drivers, One Inverting and One Non-inverting
- Each Driver Capable of Sourcing and Sinking 5A
- CMOS and TTL Compatible Inputs
- Independent Enable for Each Driver
- 4.5V to 18V Supply Voltage Range
- -40°C to +125°C Extended Operating Temperature Range
- ±2kV ESD Rating (Human Body Model)
- Thermally enhanced 8-pin MSOP and narrow SOIC packages and standard 8-pin narrow SOIC package
- Under Voltage Lockout Circuitry
- Fast Propagation Delays (16ns typical)
- Fast Rise and Fall Times (7ns typical)

Applications

- Switch-Mode Power Supplies
- DC-DC Converters
- Motor Controllers
- Power Inverters

IX4342 Functional Block Diagram



Description

The IX4342 is a dual, high current, low side gate driver with one inverting and one non-inverting input. With a maximum voltage rating of 18V, each of the two outputs is capable of sourcing and sinking 5A of peak current. For higher current applications, the two independent outputs can be paralleled. Fast propagation delay times (16ns typical) with fast rise and fall times (7ns typical) make the IX4342 well suited for high frequency applications.

The inputs are TTL and CMOS logic compatible and each driver has a dedicated Enable function. Under Voltage Lock Out (UVLO) circuitry prevents the driver outputs from going high until sufficient supply voltage is available. An internal pull up resistor at $\overline{\text{INA}}$ and pull down resistor at INB prevent the outputs from going high whenever the inputs are floating (open).

The IX4342 is available in a standard 8-pin narrow SOIC and thermally enhanced 8-pin MSOP and narrow SOIC packages.

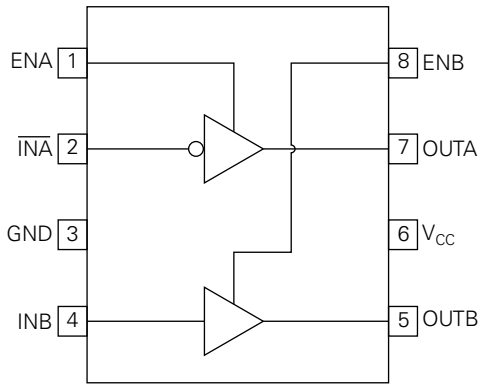
Ordering Information

Part #	Description
IX4342N	8-pin Narrow SOIC (100/tube)
IX4342NTR	8-pin Narrow SOIC (4000/reel)
IX4342NE	8-pin Narrow SOIC, exposed thermal pad (100/tube)
IX4342NETR	8-pin Narrow SOIC, exposed thermal pad (4000/reel)
IX4342UE	8-pin MSOP, exposed thermal pad (80/tube)
IX4342UETR	8-pin MSOP, exposed thermal pad (5000/reel)

PP 2/14/2024
IX4342_R01

1 Specifications

1.1 Package Pinout



1.2 Logic Table

$\overline{INA}$	ENA	INB	ENB	UVLO [2]	OUTA
0	1[1]	X	X	0	1
1[1]					0
X	0				0
X	X			1	0

$\overline{INA}$	ENA	INB	ENB	UVLO [2]	OUTB
X	X	0[1]	1[1]	0	0
		1			1
		X	0		0
		X	X	1	0

Notes:
[1] Or floating (open)
[2] UVLO = 0 - Drivers available
UVLO = 1 - Both drivers are disabled
UVLO is common to both drivers

1.3 Pin Definitions

Pin	Name	Description
1	ENA	Enable input for Channel A. ENA=1 (or floating) enables $\overline{INA}$ control of OUTA. ENA=0 forces OUTA low.
2	$\overline{INA}$	Channel A inverting logic input with internal pull up to V_{CC}.
3	GND	Ground
4	INB	Channel B non-inverting logic input with internal pull down to GND.
5	OUTB	Channel B gate drive output.
6	V_{CC}	Supply voltage.
7	OUTA	Channel A gate drive output.
8	ENB	Enable input for Channel B. ENB = 1 (or floating) enables INB control of OUTB. ENB = 0 forces OUTB low.

It is highly recommended the exposed bottom side pad (not shown) of the IX4342NE and IX4342UE be connected to GND (Pin 3). It may be left floating but must not be connected to any other net and is not intended to carry current.

1.4 Absolute Maximum Ratings

Parameter	Symbol	Value		Units
		Minimum	Maximum	
Supply voltage	V_{CC}	-0.3	20	V
Input voltage ($\overline{INA}$, INB, ENx)	V_{IN}	-0.3	V_{CC}+0.3	
Output voltage (OUTx)	V_{OUT}	-0.3	V_{CC}+0.3	
Output current (OUTx)	I_{OUT}	-	±5	A
ESD rating (Human Body Model)	V_{ESD}	-	±2	kV
Junction temperature	T_J	-55	+150	°C
Storage temperature	T_{STG}	-65	+150	

Absolute maximum electrical ratings are at 25°C.

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.5 Recommended Operating Conditions

Parameter	Symbol	Value		Units
		Minimum	Maximum	
Supply voltage	V_{CC}	4.5	18	V
Input voltage ($\overline{INA}$, INB, ENx)	V_{IN}	0	V_{CC}	
Output voltage (OUTx)	V_{OUT}	0	V_{CC}	
Switching frequency	f_{IN}	-	1	MHz
Ambient temperature	T_A	-40	+125	°C

1.6 Electrical Characteristics

Unless otherwise noted, V_{CC} = 12V, and -40°C ≤ T_A ≤ +125°C.

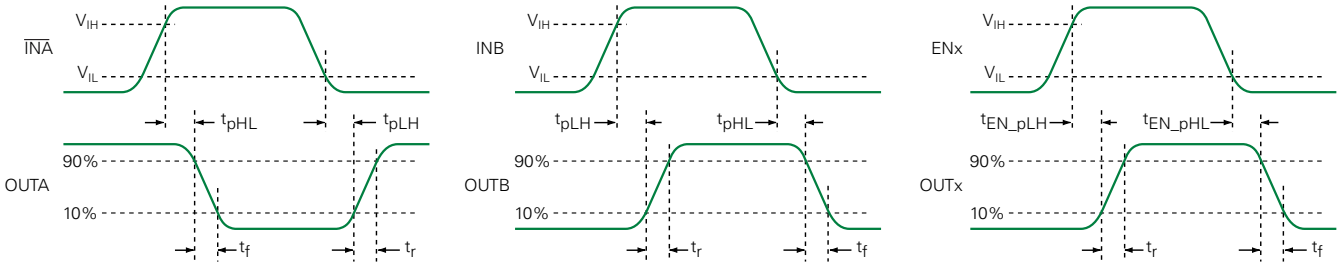
Typical values are characteristic of the device at T_A = 25°C and are the result of engineering evaluations. They are provided for informational purposes only and are not part of the manufacturing testing requirements.

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Supply						
Supply current	OUTA = OUTB = Open	I_{CC}	-	1.4	2.5	mA
Under Voltage Lockout (UVLO)						
UVLO Threshold	V_{CC} rising	$V_{CCUV\_th(r)}$	3.5	3.85	4.2	V
	V_{CC} falling	$V_{CCUV\_th(f)}$	3.1	3.3	3.5	
UVLO Hysteresis	-	V_{CCUV_hys}	0.2	0.5	-	
Logic Inputs ($\overline{INA}$, INB, ENx)						
Input voltage						
Logic low	-	V_{IL}	-	-	0.8	V
Logic high		V_{IH}	2.5	-	-	
Hysteresis		V_{I_hys}	0.2	0.5	-	
Input pull-up resistance ($\overline{INA}$, ENx)	-	R_{IN}	-	95	130	kΩ
Input pull-down resistance (INB)						
Driver Outputs (OUTx)						
Output high on-resistance	I_{OUT} = -100mA, T_J = 25°C	R_{OH}	-	1	1.5	Ω
	I_{OUT} = -100mA		-	-	1.8	
Output low on-resistance	I_{OUT} = 100mA, T_J = 25°C	R_{OL}	-	0.6	1.1	
	I_{OUT} = 100mA		-	-	1.4	

1.7 Switching Characteristics

Unless otherwise noted, V_{CC}=12V, V_{INL}=0V, V_{INH}=5V, f_{IN}=100kHz, D=50%, C_L=1.8nF, and -40°C≤T_A≤+125°C.

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Input propagation delay	$V_{EN}=V_{CC}$					ns
Low to high		t_{pLH}	5	16	30	
High to low		t_{pHL}	5	15	30	
Matching	Matching A to B	t_{pM}	-5	-	5	
Enable propagation delay	$V_{\overline{INA}}=0V$, $V_{INB}=V_{CC}$					
Low to high		t_{EN_pLH}	5	16.25	30	
High to low		t_{EN_pHL}	5	15.4	30	
Matching	Matching A to B	t_{EN_pM}	-5	-	5	
Rise time	-	t_r	-	7	15	
Fall time	-	t_f	-	7	15	



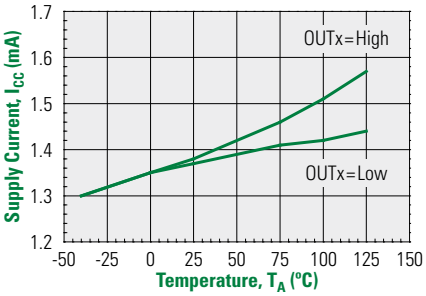
1.8 Thermal Characteristics

Parameter	Symbol	Rating	Units
IX4342N Thermal Impedance, Junction to Ambient	θ_{JA}	120	°C/W
IX4342NE Thermal Impedance, Junction to Ambient	θ_{JA}	85	
IX4342NE Thermal Impedance, Junction to Case	θ_{JC}	10	
IX4342UE Thermal Impedance, Junction to Ambient	θ_{JA}	40	
IX4342UE Thermal Impedance, Junction to Case	θ_{JC}	10	

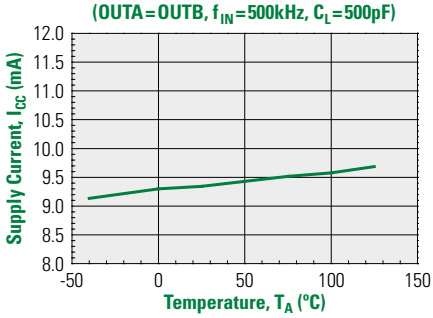
2 Performance Data

Unless otherwise noted, data presented in these graphs is typical of device operation with V_{CC}=12V, ENx=V_{CC}, and T_A=25ºC.

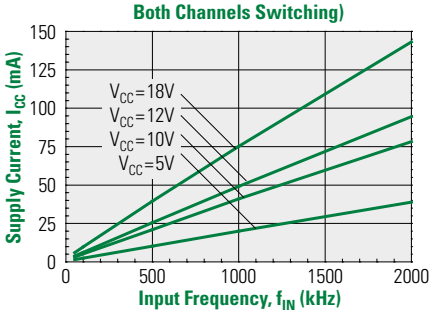
Supply Current vs. Temperature (OUTA=OUTB, f_{IN}=0Hz)



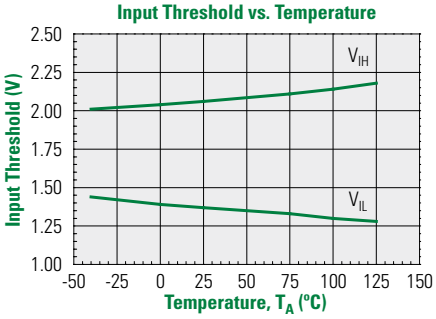
Operating Supply Current vs. Temperature (OUTA=OUTB, f_{IN}=500kHz, C_L=500pF)



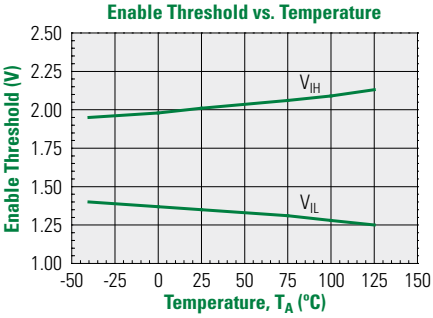
Operating Supply Current vs. Frequency (OUTA=OUTB, C_L=1.8nF, Both Channels Switching)



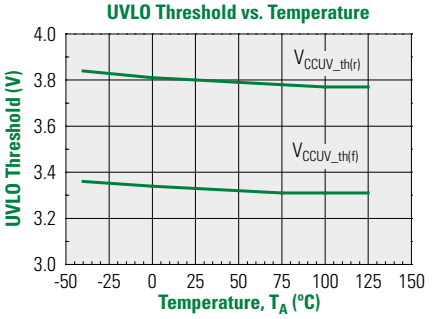
Input Threshold vs. Temperature



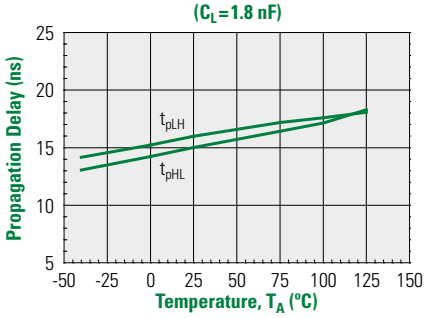
Enable Threshold vs. Temperature



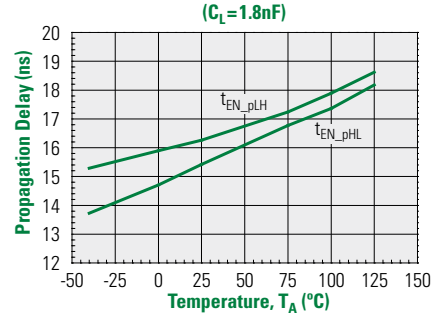
UVLO Threshold vs. Temperature



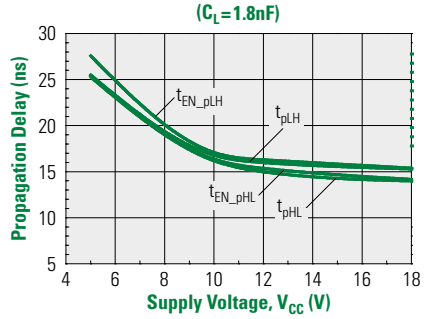
Input To Output Propagation Delay vs. Temperature (C_L=1.8 nF)

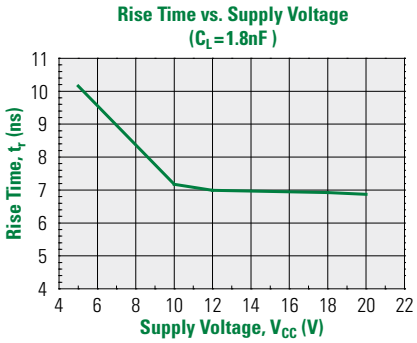


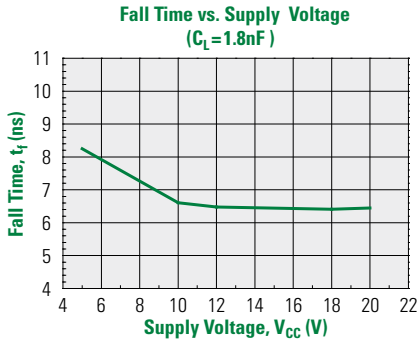
Enable to Output Propagation Delay vs. Temperature (C_L=1.8nF)

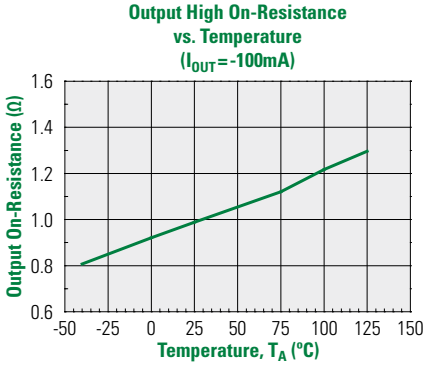


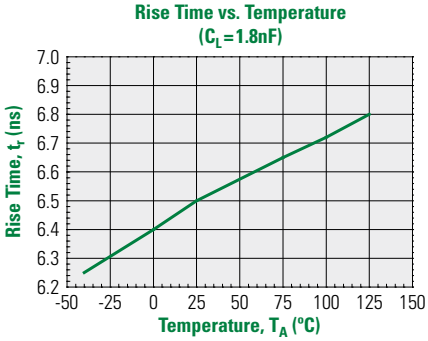
Propagation Delay vs. Supply Voltage (C_L=1.8nF)

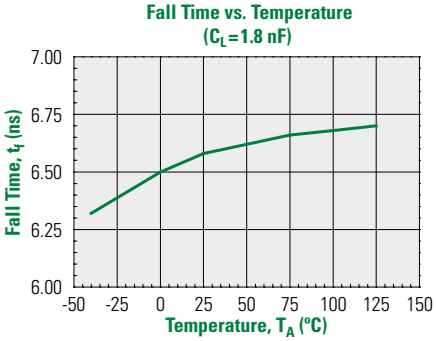


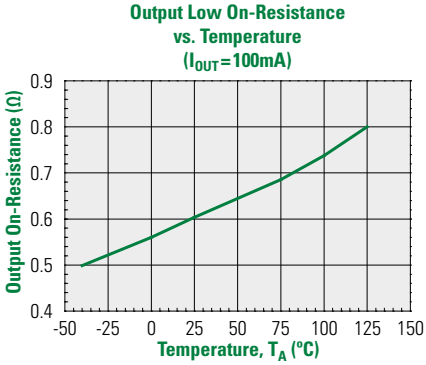












3 Manufacturing Information

3.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. Littelfuse classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a Moisture Sensitivity Level (MSL) classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
All Versions	MSL 1

3.2 ESD Sensitivity

This product is ESD Sensitive, and should be handled according to the industry standard **JESD-625**.

3.3 Soldering Profile

Provided in the table below is the **IPC/JEDEC J-STD-020** Classification Temperature (T_c) and the maximum dwell time the body temperature of these surface mount devices may be (T_c - 5)°C or greater. The Classification Temperature sets the Maximum Body Temperature allowed for these devices during reflow soldering processes.

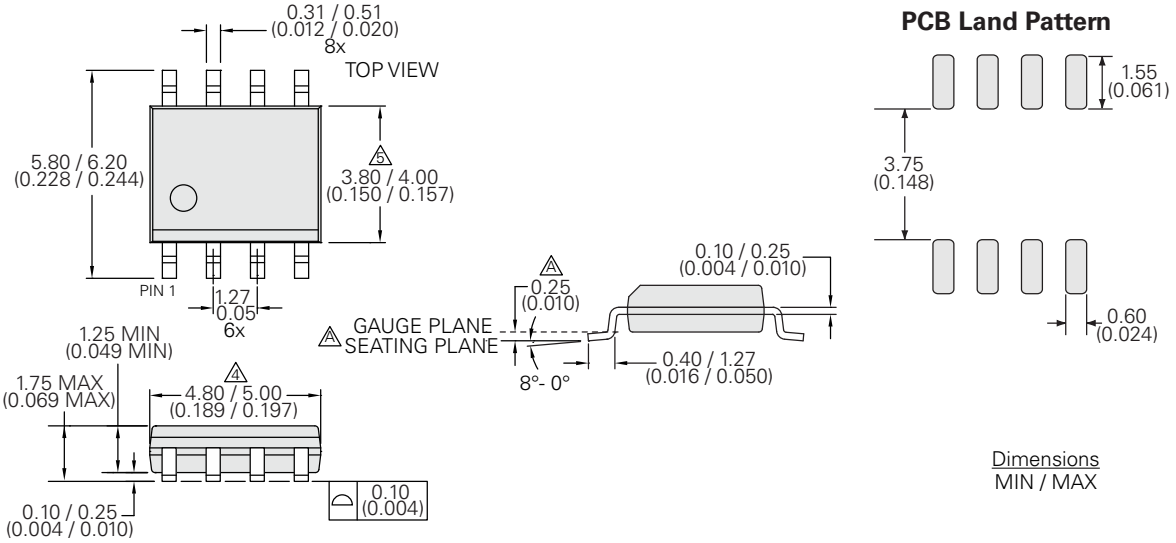
Device	Classification Temperature (T_c)	Dwell Time (t_P)	Maximum Reflow Cycles
All Versions	260°C	30 seconds	3

3.4 Board Wash

Littelfuse recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

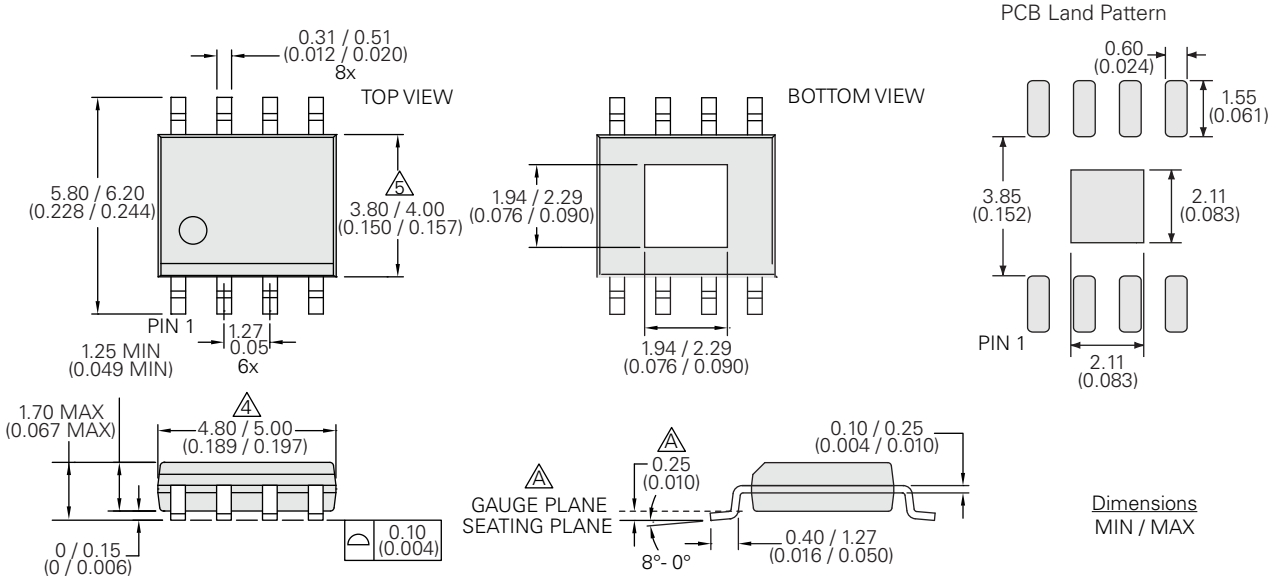
3.5 Mechanical Dimensions

3.5.1 IX4342N 8-Pin Narrow SOIC



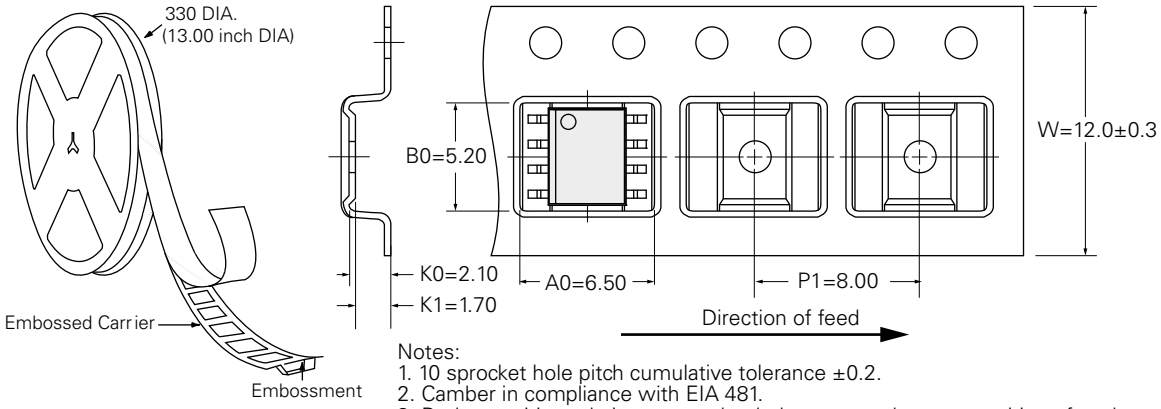
Notes:
1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation AA, Rev. F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per end.
5. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
6. Lead thickness includes plating.

3.5.2 IX4342NE 8-Pin Narrow SOIC with Exposed Bottom Side Pad



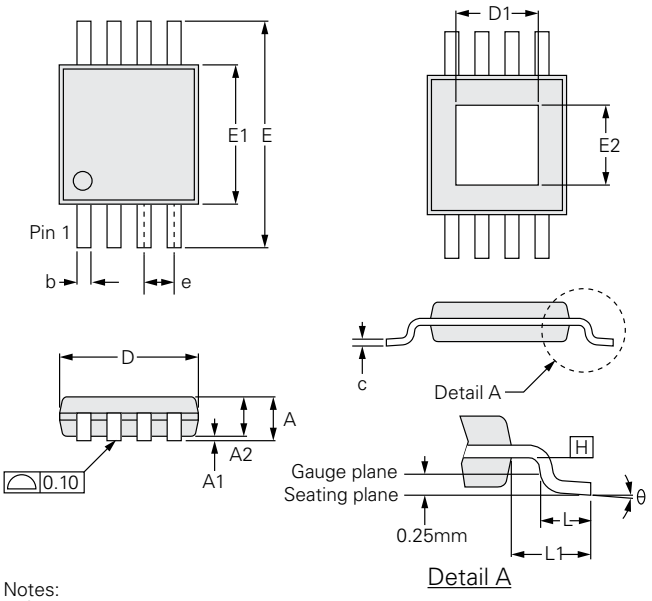
Notes:
1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation BA, Rev. F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per end.
5. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
6. Lead thickness includes plating.
7. It is highly recommended the bottom side exposed pad be connected to GND (Pin 3). It may be left floating but must not be connected to any other net and is not intended to carry current.

3.5.3 IX4342NTR & IX4342NETR Tape & Reel Dimensions



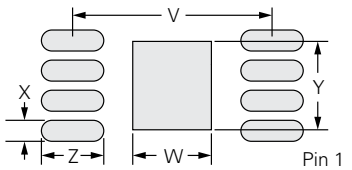
Notes:
1. 10 sprocket hole pitch cumulative tolerance ±0.2.
2. Camber in compliance with EIA 481.
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
4. All dimensions in millimeters.

3.5.4 IX4342UE 8-Pin MSOP with Exposed Bottom Side Pad



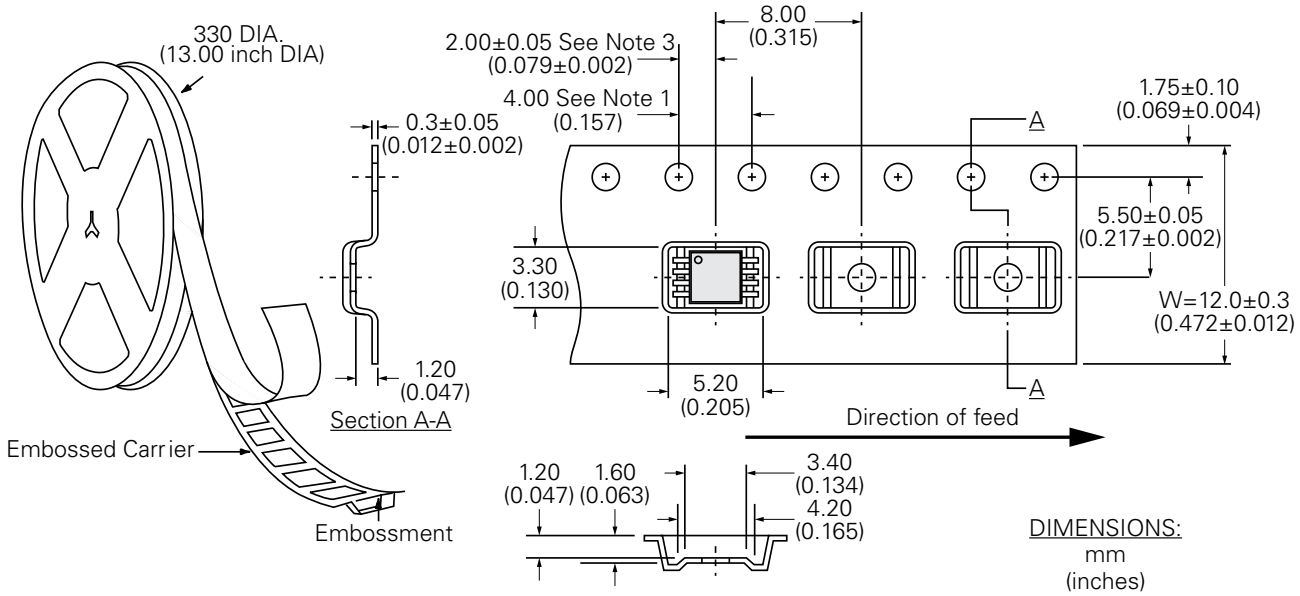
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.10	-	-	0.043
A1	0.00	-	0.15	0.00	-	0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22	-	0.38	0.009	-	0.015
c	0.08	-	0.23	0.003	-	0.009
D	3.00 BSC			0.118 BSC		
D1	1.42	-	1.93	0.056	-	0.076
E	4.90 BSC			0.193 BSC		
E1	3.00 BSC			0.118 BSC		
E2	1.38	-	1.73	0.054	-	0.068
e	0.65 BSC			0.026 BSC		
L	0.40	0.60	0.80	0.016	0.024	0.031
L1	0.95 REF			0.037 REF		
θ	0°	-	8°	0°	-	8°
LAND PATTERN						
V	-	4.30	-	-	0.169	-
W	-	1.70	-	-	0.067	-
X	-	0.45	-	-	0.018	-
Y	-	1.90	-	-	0.075	-
Z	-	1.35	-	-	0.053	-

Recommended PCB Land Pattern



Notes:
1. Controlling dimension: millimeters.
2. JEDEC outline: Thermally enhanced: MO-187 AA-T.
3. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per end.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and an adjacent lead shall not be less than 0.07mm.
5. D and E1 dimensions are determined at datum H.
6. Lead thickness includes plating.
7. It is highly recommended the bottom side exposed pad be connected to GND (Pin 3). It may be left floating but must not be connected to any other net and is not intended to carry current.

3.5.5 IX4342UETR Tape & Reel Dimensions



1. 10 sprocket hole pitch cumulative tolerance: ±0.2 (0.008).
2. Camber in compliance with EIA 481.
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

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