IX6611
IGBT Gate Driver

Features

- Input Compatible with Pulse Transformer
- 10A Peak Source and Sink Current Gate Drive
- Separate Source and Sink Outputs
- Negative Gate Drive Capability
- Over Current Protection with Adjustable Blanking Time
- Advanced Active Clamping Protection
- Under Voltage Lockout Protection
- Over Voltage Lockout Protection
- Two One-Amp Pulse Transformer drivers for Fault Communication

Applications

- AC and DC Motor Drives
- UPS Systems
- High Voltage DC/DC Converters

Description

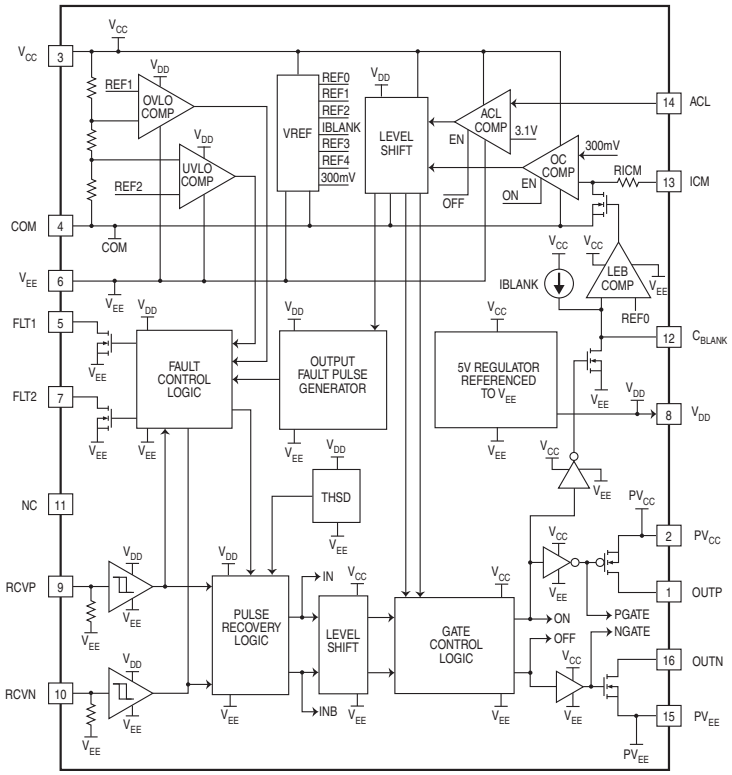
The IX6611 is a secondary side, intelligent, high speed gate driver designed to drive IXYS IGBTs as well as power MOSFET devices. The IX6611 gate driver contains the necessary circuit blocks for pulse transformer isolated applications. High frequency, narrow pulses are used for bidirectional data transfer across the isolation boundary to avoid duty cycle restrictions and to prevent transformer saturation. The IX6611 includes the necessary monitor/protection functions such as Supply Under Voltage Lockout, Supply Over Voltage Lockout, Thermal Shut down, external IGBT Over Current and Over Voltage protection.

The IX6611 is designed to operate over a temperature range of -40°C to +125°C. The IX6611 is available in a 16-lead SOIC with an exposed thermal pad.

Ordering Information

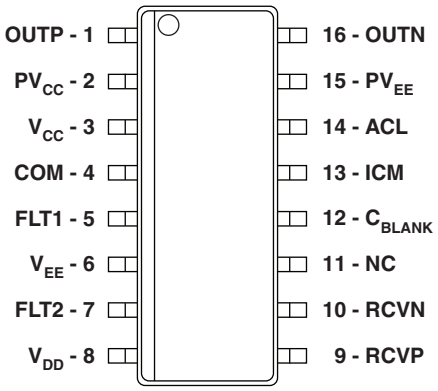
Part	Description
IX6611T	16-Pin SOIC in Tubes (50/Tube)
IX6611TR	16-Pin SOIC Tape & Reel (1000/Reel)
IX6611	Tested Die

Figure 1. IX6611 Block Diagram



1. Specifications

1.1 Package Pinout Pin Description



1.2 Pin Configuration and Definitions

Pin#	Name	Description
1	OUTP	Gate driver source output terminal
2	PV_{CC}	Gate driver positive power supply input terminal (connects to the power converter secondary)
3	V_{CC}	Device positive power supply input terminal (connects to the power converter secondary)
4	COM	Device common ground terminal (connects to the power converter secondary and the IGBT emitter terminal)
5	FLT1	Fault signal transformer primary positive terminal
6	V_{EE}	Device negative power supply input terminal (connects to the power converter secondary)
7	FLT2	Fault signal transformer primary negative terminal
8	V_{DD}	5V regulator output terminal referenced to V_{EE} (connects to an external bypass capacitor)
9	RCVP	Positive input terminal (connects to the pulse transformer secondary positive terminal)
10	RCVN	Negative input terminal (connects to the pulse transformer secondary negative terminal)
11	NC	No connection
12	C_{BLANK}	Over current comparator blanking time capacitor terminal
13	ICM	Current sense input terminal (connects to the IGBT current sense resistor)
14	ACL	Active clamping detect input terminal (connects to the external IGBT collector terminal through a blocking diode)
15	PV_{EE}	Gate driver negative power supply input terminal (connects to the power converter secondary)
16	OUTN	Gate driver sink output terminal

1.3 Absolute Maximum Ratings @ 25°C

Parameter	Symbol	Limit	Units
Supply voltage range	(V_{CC}-V_{EE}), (PV_{CC}-PV_{EE})	-0.3 to 40	V
Positive supply voltage V_{CC} , PV_{CC}	(V_{CC}-V_{COM}), (PV_{CC}-V_{COM})	-0.3 to 32	V
Negative supply voltage V_{EE} , PV_{EE}	(V_{EE}-V_{COM}), (PV_{EE}-V_{COM})	- 10 to 0	V
Driver output voltages	OUTP, OUTN	(PV_{EE}-0.3) to (PV_{CC}+0.3)	V
Regulator output terminal voltage	V_{DD}-V_{EE}	-0.3 to 7	V
Analog input terminal voltages	ICM	(V_{COM}-0.3) to (V_{CC}+0.3)	V
Analog input terminal voltages	ACL	(V_{EE}-0.3) to V_{CC}+0.3)	V
Fault output terminal voltages	FLT1, FLT2, C_{BLANK}	(V_{EE}-0.3) to V_{CC}+0.3)	V
Input terminal voltages	RCVP, RCVN	(V_{EE}-0.3) to (V_{EE}+7)	V
Operating junction temperature range	t_J	-55 to +150	°C
Storage temperature	T_{STG}	-65 to +150	°C

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 ESD Warning

ESD (electrostatic discharge) sensitive device. Electrostatic charges can readily accumulate on test equipment and the human body in excess of 4000 Volts. This energy can discharge without detection. Although the IX6611 features proprietary ESD protection circuitry, permanent damage might be sustained if subjected to high energy electrostatic discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

1.5 Electrical Characteristics

T_A=-40°C to +125°C unless otherwise noted.

1.5.1 Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal resistance, junction to ambient	Θ_{JA}	41	°C/W

1.5.2 Power Supply Terminals

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Logic power supply voltage range	V_{CC}	V_{CC}-V_{COM}	13	15	25	V
Logic power supply voltage range	V_{EE}	V_{EE}-V_{COM}	-10	-5	0	V
Output driver positive power supply voltage range	PV_{CC}	PV_{CC}-V_{COM}	13	15	25	V
Output driver negative power supply voltage range	PV_{EE}	PV_{EE}-V_{COM}	-10	-5	0	V
Static power supply current	I_{CCQ}	V_{CC}= PV_{CC}=15V, V_{EE}= PV_{EE}= -5V No load, static output condition	-	3	5	mA
	I_{COMQ}		-	0.2	0.5	
	I_{EEQ}		-	3	5	
Dynamic power supply current	I_{CC}	V_{CC}= PV_{CC}=15V, V_{EE}= PV_{EE}= -5V, C_L=10nF Normal mode, F_{OUT}=50kHz	-	15	20	mA
	I_{COM}		-	0.2	0.5	
	I_{EE}		-	15	20	

1.5.3 V_{DD} Regulator (Logic Supply)

V_{CC}=PV_{CC}=15V, V_{EE}=PV_{EE}= -5V. V_{DD} regulator voltage is referenced to V_{EE}. Examples: If V_{EE}=-5V, then V_{DD}=0V; or If V_{EE}=-10V, then V_{DD}=-5V; or If V_{EE}=0V, then V_{DD}=+5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Regulator output voltage	V_{DD}	V_{CC}=15V, V_{EE}=- 5V I_{DD}=5mA	-1	0	0.5	V
Input line regulation	ΔV_{DD}	(V_{CC}–V_{EE})=15V to 25V @ V_{EE}=-10V @ I_{DD}=5mA	-	0.2	-	V
Output load regulation	ΔV_{DD_IDD}	V_{CC}=15V, V_{EE}=-5V I_{DD}=1mA to 10mA	-	0.5	-	V
Output bypass capacitor ESR	C_{VDD_ESR}	1mA $\leq I_{DD} \leq$ 10mA	-	0.3	-	Ω

1.5.4 Input Terminals

V_{CC}=PV_{CC}=15V, V_{EE}=PV_{EE}=-5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Receive input pull-down current @ V_{DD}=0V	I_{RCVN_DD}, I_{RCVP_DD}	Measured at RCVP and RCVN terminals @ V_{DD}=0V	3	5	10	mA
Analog input leakage current @ V_{CC} & V_{COM}	I_{ACL_CC}, I_{ACL_COM}	Measured at ACL terminal	-1	-	1	µA
Analog input leakage current @ V_{COM}	I_{ICM_COM}	Measured at ICM terminal	-1	-	1	µA

1.5.5 Input Interface/Pulse Recovery

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Receive input resistance	R_{RCVP_IN}, R_{RCVN_IN}	Measured at terminals RCVP, RCVN with respect to V_{EE}	0.5	1	1.5	kΩ
Receive input high voltage	V_{RCVP_IH} V_{RCVN_IH}	Measured with respect to V_{EE} at RCVP and RCVN terminals by monitoring the state change at the IGBT driver output terminals (OUTP and OUTN). @ V_{DD}=0V	2.2	-	-	V
Receive input low voltage	V_{RCVP_IL} V_{RCVN_IL}		-	-	1	V
Receive input hysteresis	V_{HST}		0.5	1	-	V
Minimum input pulse width detect	T_{DET_RCVP} T_{DET_RCVN}	Measured at RCVP and RCVN terminals by monitoring the state change at the IGBT driver output terminals @ V_{DD}=0V	100	200	-	ns

1.5.6 Thermal Shutdown Circuit

V_{CC}=PV_{CC}=15V, V_{EE}=PV_{EE}=-5V. Not production tested. Specifications are characterized and guaranteed by design.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Thermal shutdown rising threshold	t_{SHDN_RISE}	-	130	145	160	°C
Thermal shutdown hysteresis	t_{SHDN_HYS}		-	20	-	°C

1.5.7 UVLO Circuit

FLT1 output is connected to a 50kΩ pullup resistor.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
(V_{CC}-V_{COM}) UVLO rising threshold	$UVLO\_V_{TH\text{-}RISE}$	V_{COM}=0V, V_{EE}=PV_{EE}=0 to -10V UVLO rising threshold is measured by monitoring state change at FLT1 terminal	8	9.5	11	V
(V_{CC}-V_{COM}) UVLO hysteresis	$UVLO\_V_{HYST}$		-	1.5	-	V

1.5.8 OVLO Circuit

FLT1 and FLT2 outputs are connected to 50kΩ pullup resistors.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
(V_{CC}-V_{COM}) OVLO rising threshold	$OVLO\_V_{TH\text{-}RISE}$	V_{COM}=0V, V_{EE}=PV_{EE}=0 to -10V OVLO rising threshold is measured by monitoring state change at FLT1 and FLT2 terminals	26	28	30	V
(V_{CC}-V_{COM}) OVLO hysteresis	$OVLO\_V_{HYST}$		-	2	-	V

1.5.9 Leading Edge Blanking Circuit (LEB)

V_{CC}=PV_{CC}=15V, V_{EE}=PV_{EE}= -5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Blanking source current	I_{BLNK_SRC}	Measured at C_{BLANK} terminal during the blanking period	180	225	300	µA
Blanking sink current (DC test)	$I_{BLNK\_SNK\_DC}$	Force CBLANK to V_{DD} during the IGBT driver off state	11	18	25	mA
Blanking time (see note)	t_{BLNK_OPEN}	IGBT driver turn-on to turn-off delay time is measured with ICM terminal set at 500mV and C_{BLANK} terminal open ΔV_{BLANK}=3V	200	400	600	ns
Blanking time (see note)	t_{BLNK_220pF}	IGBT driver turn-on to turn-off delay time is measured with ICM terminal set at 500mV and C_{BLANK}=220pF	2	3.5	5	µs

Note: *All timing measurements are from 90% input stimulus change to the 10% output response change.*

1.5.10 Over Current Comparator

V_{CC}=PV_{CC}=15V, V_{EE}=PV_{EE}= -5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Over current comparator threshold with respect to COM	V_{OCTH}	VOCTH is measured during the ON time of the driver at ICM terminal by monitoring the state change at the IGBT driver output	240	300	360	mV
Over current comparator response time (see note)	t_{OCR}	Step input at the ICM terminal with ±50mV overdrive (delay time is measured from ICM input to gate drive output)	-	150	250	ns
Over current comparator input series resistor	R_{ICM}	Measured at ICM terminal during blanking time	1	2	3	kΩ
Over current comparator input shorting switch on-resistance	R_{ON_ICM}	Specification guaranteed by design	-	75	-	Ω

Note: *Timing measurements are from 90% input stimulus change to the 10% output response change.*

1.5.11 Active Clamp Comparator

V_{CC}=PV_{CC}=15V, V_{EE}=PV_{EE}= -5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
ACL comparator threshold with respect to V_{EE}	VACLTH	VACLTH is measured during the OFF time of the driver at ACL terminal by monitoring the state change at the IGBT driver output, IGBT driver output is connected to 50Ω to COM terminal	2.6	3.1	3.6	V
ACL comparator response time (see note)	TACLR	Step input with ± 500mV overdrive at the ACL terminal (Information parameter)	-	150	-	ns
ACL comparator to driver output tri-state delay time (see note)	TACL_TRI	Step input at the ACL terminal with ± 500mV overdrive (delay time is measured from ACL input to IGBT driver output, IGBT driver output is connected to 50Ω to COM terminal)	-	300	-	ns

Note: *Timing measurements are from 90% input stimulus change to the 10% output response change.*

1.5.12 Fault Outputs and Control Logic

V_{CC}=PV_{CC}=15V, V_{EE}=PV_{EE}= -5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Fault signal transformer primary switch sink resistance	R_{FLT1}, R_{FLT2}	V_{DD}=0V, measured at FLT1 and FLT2 terminals @ I_{SINK} = 100mA	-	1	2	W
Fault signal transformer primary switch peak sink current	I_{PK_FLT1}, I_{PK_FLT2}	V_{DD}=0V, measured at FLT1 and FLT2 terminals 200ns pulse (Characterized but not production tested)	0.7	1	-	A
Fault signal transformer primary switch low level output voltage	V_{OL_FLT1}, V_{OL_FLT2}	V_{DD}=0V, measured at FLT1 and FLT2 terminals with 5Ω pull-up resistance connected to V_{DD}	-	0.5	1.5	V
Fault signal transformer primary switch off-state max drain voltage	V_{DSMAX_FLT1} V_{DSMAX_FLT2}	@ I_{DS_LEAK}=1uA	15	-	-	V
Fault signal pulse width	T_{PW_FLT1} T_{PW_FLT2}	Measured at FLT1 and FLT2 terminals with 100Ω pull-up and C_L=50pF resistance connected to V_{DD} (characterized but not production tested)	100	200	400	ns

1.5.13 IGBT Driver Output

V_{CC}=PV_{CC}=15V, V_{EE}=PV_{EE}= -5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
High level output voltage	V_{OHP}	I_{SOURCE}=100mA Measured at OUTP terminal	V_{CC}-0.15	-	-	V
Low level output voltage	V_{OLN1}	I_{SINK}=100mA Measured at OUTN terminal	-	-	0.15	V
Output source resistance	R_{OH}	I_{SOURCE}=100mA Measured at OUTP terminal	-	0.8	1.7	Ω
Output sink resistance	R_{OL}	I_{SINK}=100mA Measured at OUTN terminal	-	0.7	1.5	Ω
Output peak source and sink current	I_{PK_SRC}, I_{PK_SNK}	@ T_A=25°C, C_{LOAD}=330nF Measured at OUTP and OUTN terminals	-	±10	-	A
Continuous output current	I_{DC}	@ T_A=25°C, measured at OUTP and OUTN terminals (limited by package power dissipation) information parameter	-	±2	-	A
On-time propagation delay	t_{ON_DLY}	C_{LOAD}=10nF Measured from RCVP to OUTP	-	50	125	ns
Off-time propagation delay	t_{OFF_DLY}	C_{LOAD}=10nF Measured from RCVN to OUTN	-	50	125	ns
High impedance state delay time	t_{TRI_DLY}	R_{LOAD}=50 , C_{LOAD}=No load	-	300	-	ns
High impedance PFET leakage	I_{PLEAK}	-	-	<1	10	µA
High impedance NFET lockage	I_{NLEAK}	-	-	<2	20	µA

2. Timing Diagrams

Figure 2. UVLO Condition FAULT1 Timing Diagram

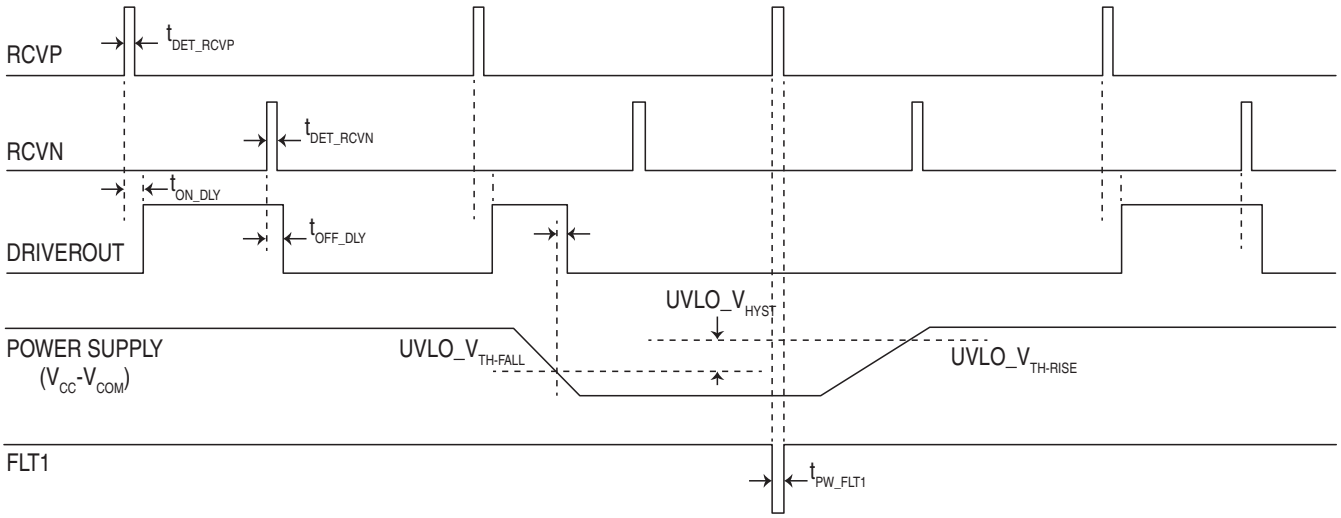


Figure 3. OVLO Condition FLT1 & FLT2 Timing Diagram

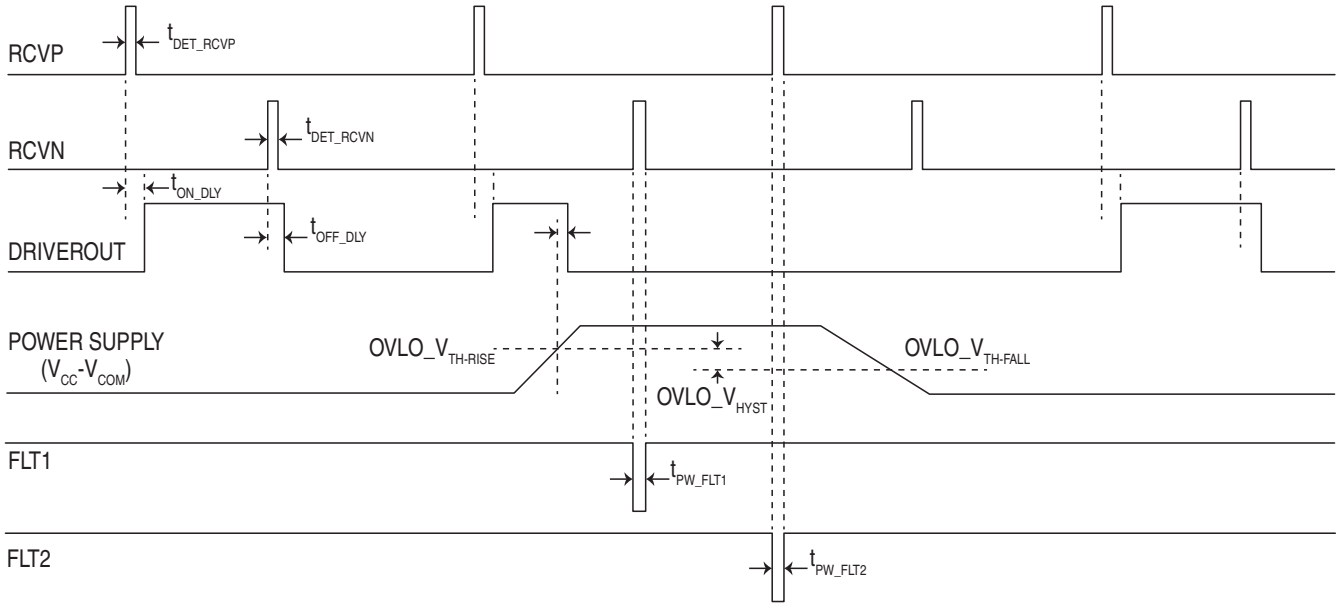


Figure 4. Over Current Condition FLT2 Timing Diagram

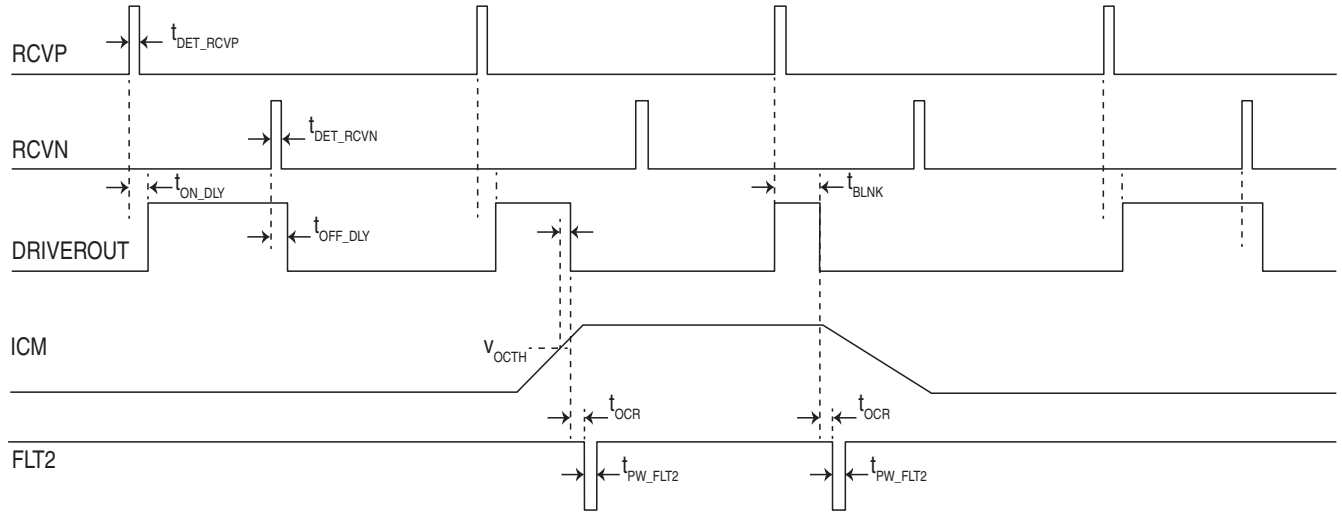


Figure 5. Active Clamp Condition Timing Diagram

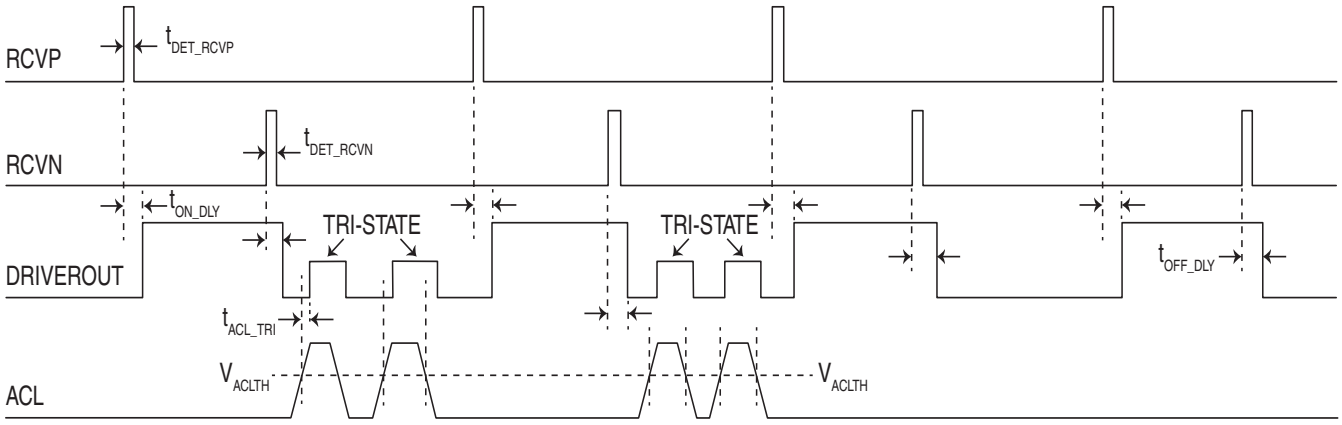
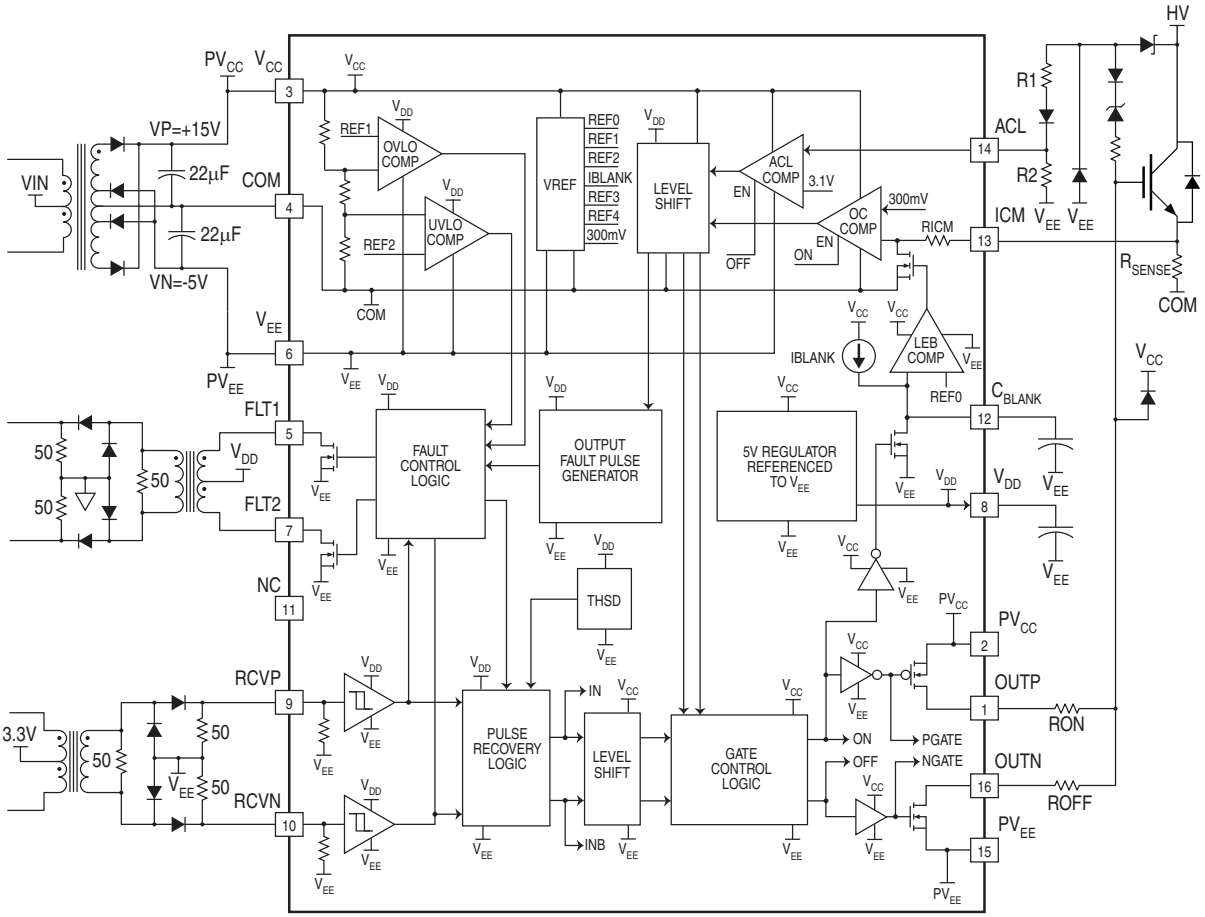


Figure 6. IX6611 Typical Application Diagram



3. Theory of Operation

The IX6611 integrated circuit is designed to provide gate drive for high power IGBT modules. The device converts the incoming isolated PWM logic signals into a +15V/-5V bipolar gate drive signal with a typical 10A peak drive current capability.

3.1 Detailed Circuit Description

3.1.1 Input Interface

The Input Interface block of the gate driver is designed to be compatible with pulse transformers. The receiver inputs, RCVP and RCVN, are connected to the pulse transformer secondary through a diode/resistor network as shown on the typical application diagram **Figure 6 on page 11**. The Input Interface contains high speed Schmitt trigger buffers with 1V typical hysteresis. To reject noise and high frequency interference, a well matched full differential architecture is used for the Schmitt trigger buffer receivers.

3.1.2 Pulse Recovery Logic

The Pulse Recovery Logic block receives the leading edge pulse and trailing edge pulse signals from the Input Interface and reconstructs the complementary IN and INB drive signals. These complementary signals are level shifted to drive the Gate Control Logic block.

3.1.3 Gate Control Logic

The Gate Control Logic block inserts a fixed dead time between the incoming IN and INB signals to generate non-overlapping PGATE drive and NGATE drive signals. This dead time is sufficient to prevent

shoot-through in the large output P-channel and N-channel devices.

The Gate Control Logic block also receives power supply status, IGBT over-current status, and IGBT collector over-voltage status signals. Based on these signals the output stage is conditioned accordingly as shown in **Figure 2 on page 9**, **Figure 3 on page 9**, **Figure 4 on page 10** and **Figure 5 on page 10**.

If a supply under-voltage or a supply over-voltage fault event is detected during the leading edge of the input PWM gate drive cycle, then the driver is disabled for the entire duration of the cycle. Normal operation resumes at the beginning of the next cycle only if there is no supply fault condition.

If an IGBT over-current fault occurs during the ON time of the PWM cycle, then the IGBT driver output is forced low for the remainder of the cycle. Normal operation resumes at the beginning of the next PWM gate drive cycle.

During the OFF time of the IGBT driver, if an IGBT collector over-voltage fault occurs, then for the remainder of the cycle the output PFET is turned off and the output NFET state is controlled by the ACL comparator as shown in the **Figure 5 on page 10**. Normal operation resumes at the beginning of the next PWM gate drive cycle.

3.1.4 IGBT Drive Outputs

IX6611 contains separate 10A peak source and sink outputs. Separated sink and source outputs allow independent gate charge and discharge control without an external diode. The internal dead-time circuit eliminates the cross conduction of the source and sink outputs.

3.1.5 Over Current Comparator

IX6611 contains an Over Current Comparator (OC COMP) with a 300mV threshold. This comparator is used for sensing over-current conditions in the external IGBT.

Emitter current sense can be implemented either by using a low value current shunt or an IGBT with a secondary current sense output.

The current-sense method works well for high gain IGBTs that do not have inherent short circuit protection. Careful application board layout is mandatory due to low sense voltage.

Traditional de-saturation protection can also be implemented using a large ratio resistor divider connected across the collector and the emitter. A noise filter (RC) at the current sense input may be required due to low sense voltage.

3.1.6 Leading Edge Blanking Circuit

To prevent false tripping of the OC Comparator, its input is grounded for a fixed amount of time during the turn-on of the IGBT.

Leading Edge Blanking Circuit sets the blanking time and it is programmable through an external capacitor. The OC Comparator input is also grounded during the off time of the driver.

3.1.7 Active Clamp Comparator

IX6611 contains an Active Clamp Comparator (ACL COMP) with a 3.1V threshold that can be used for implementing an advanced active clamping technique as shown in application circuit diagram **Figure 6 on page 11**. ACL COMP threshold is with respect to V_{EE}.

During the turn off of the IGBT, the ACL comparator can detect an over voltage, if the collector voltage rises above the breakdown voltage of the diode connected at the collector. In the over voltage condition the ACL comparator forces the gate driver output to a tri-state condition and the IGBT starts to turn on due to the break down diode current charging the IGBT gate. Once the IGBT turns on, its collector voltage falls, the diode recovers from break down, and the ACL comparator turns on the NMOS output and forces the IGBT gate low. This sequence may repeat several times until the energy in the external inductance is dissipated.

ACL comparator is active only when the driver output PFET is OFF.

3.1.8 Thermal Shutdown (THSD)

IX6611 contains a Thermal Shutdown circuit to protect the device against the damage due to excessive die temperature. When the junction temperature exceeds 150°C, the input signals to the gate driver and the ACL comparator are disabled and the gate driver output is forced low. Device resumes normal operation when the junction temperature falls below 130°C.

3.1.9 Output Fault Pulse Generator

An IGBT over current fault event can occur any time during the ON time of the gate drive signal. When an

over current occurs the Output Faults Pulse Generator creates a narrow 200ns pulse that will be used by the Fault Control Logic to communicate the fault condition to the primary side across the barrier.

3.1.10 5V Regulator

The 5V regulator provides power to the internal low voltage circuits that are referenced to VEE. Regulator is powered from V_{CC} and V_{EE} and its output voltage is referenced to V_{EE}. An external bypass capacitor is required to provide the transient currents.

3.1.11 Under Voltage and Over Voltage Lockout

IX6611 contains an Under Voltage Lockout Comparator (UVLO COMP) and an Over Voltage Lockout Comparator (OVLO COMP). These comparators monitor the positive power supply terminal "V_{CC}" with respect to "COM" terminal. At the beginning of each PWM cycle, if the difference in power supply voltage (V_{CC}-V_{COM}) is below the UVLO threshold or above the OVLO threshold the gate driver output is disabled (driven low) for that PWM cycle. Once the PWM cycle starts with no power supply faults then the gate driver is enabled and the UVLO and OVLO faults are ignored for the reminder of the cycle. Power supply fault are not latched. Normal operation resumes automatically on the next PWM input cycle after the power supply recovers from the fault condition.

The UVLO circuit is operational at V_{CC} no greater than 3V and it keeps the gate driver output low until V_{CC} is raises above the UVLO threshold.

3.1.12 Fault Control Logic

Fault information is communicated to the primary side through the pulse transformer interface. Fault Control Logic provides the gate drive to the high current switches connected to the primary terminals of the pulse transformer. Narrow pulses are used to drive the high current switches. Based on the fault type, the fault control logic selects the narrow pulses either from the input interface or from the output fault pulse generator and drives the appropriate high current switch.

UVLO fault condition is communicated to the primary side by driving the FLT1 high current switch on the leading edge of the PWM gate drive ON cycle.

OVLO fault condition is communicated to the primary side by driving the FLT1 high current switch on the leading edge and the FLT2 high current switch on the trailing edge of the PWM gate drive ON cycle. The primary side recognizes the OVLO fault condition if and only if both FLT1 and FLT2 flags are set.

IGBT Over Current condition is communicated to the primary side by driving the FLT2 high current switch with a pulse from the output fault pulse generator.

4. Manufacturing Information

4.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Corporation classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) classification** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IX6611T	MSL 1

4.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

4.3 Soldering Profile

Provided in the table below is the Classification Temperature (T_C) of this product and the maximum dwell time the body temperature of this device may be above (T_C - 5)°C. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through hole devices, and any other processes, the guidelines of **J-STD-020** must be observed.

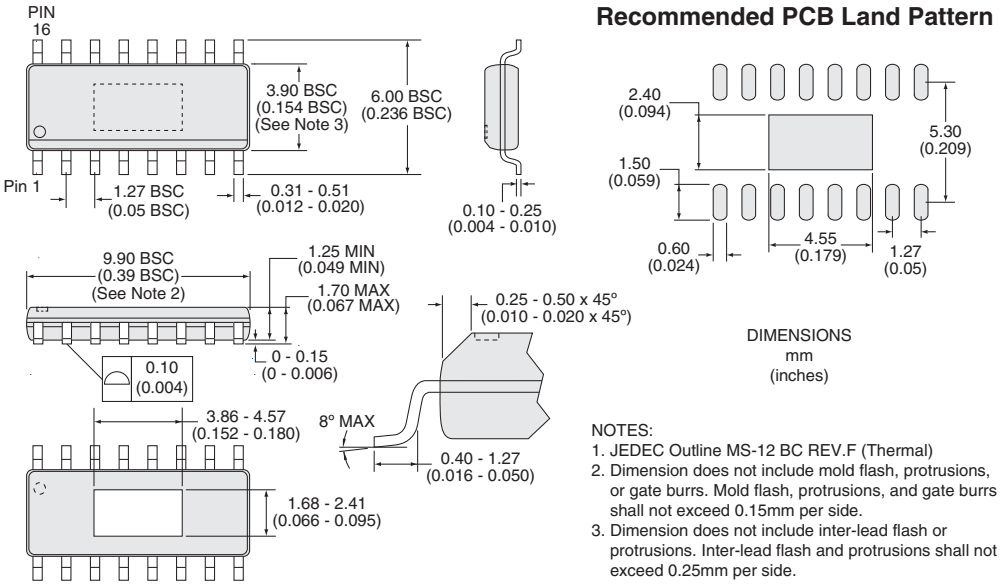
Device	Classification Temperature (T_C)	Dwell Time (t_p)	Max Reflow Cycles
IX6611T	260°C	30 seconds	3

4.4 Board Wash

IXYS Corporation recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include, but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based.

4.5 Package Mechanical Dimensions

4.5.1 IX6611T 16-Pin SOIC



NOTES:
1. JEDEC Outline MS-12 BC REV.F (Thermal)
2. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15mm per side.
3. Dimension does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.25mm per side.

4.5.2 IX6611TTR Tape & Reel

TBD

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Specification: DS-IX6611-R00A

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