

### Features

- Precision reference, error amplifier, and a high voltage Darlingtion transistor in a single package
- 1.299V±1% reference @25°C (±1.5% @-40°C to 85°C)
- Error amplifier supply voltage range: 1.3V to 12.5V over temperature
- Breakdown voltage of Darlingtion transistor: 350V

### Applications

- LED lamps
- Low voltage power supply feedback
- AC-to-DC off-line power supplies
- DC-to-DC converters

### Description

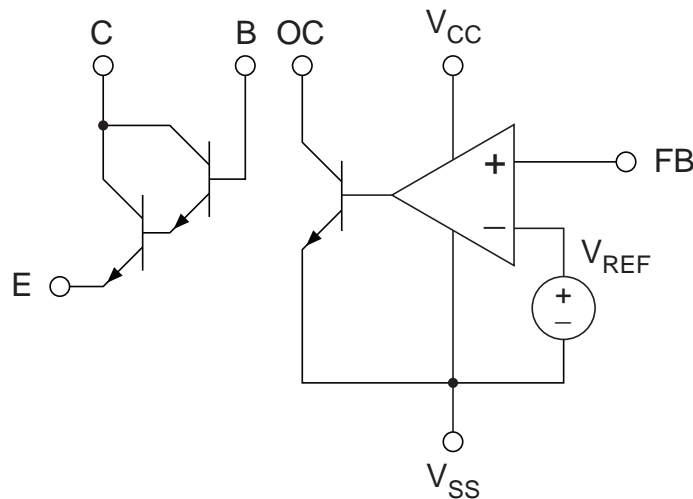
The IX9915 integrates an error amplifier with a precision reference and a 350V Darlingtion transistor in a single package. The error amplifier can be operated from 1.3V to 12.5V over the operational temperature range. The breakdown voltage of the Darlingtion transistor is 350V.

The integrated combination of a 4-terminal 431 type shunt regulator with a high voltage Darlingtion transistor is ideal for use in LED lamp bleeder control circuits.

### Ordering Information

Part	Description
IX9915N	8-pin SOIC, Tube (100/Tube)
IX9915NTR	8-pin SOIC, Tape & Reel (2000/Reel)

### IX9915 Block Diagram

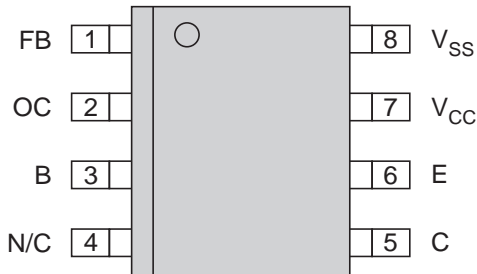


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## 1. Specifications

### 1.1 Package Pinout



### 1.2 Pin Description

Pin#	Name	Description
1	FB	Input Voltage
2	OC	Output Current
3	B	Darlington Base
4	N/C	Not Connected
5	C	Darlington Collector
6	E	Darlington Emitter
7	V <sub>CC</sub>	Supply Input
8	V <sub>SS</sub>	Supply Return

### 1.3 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Collector-Emitter Voltage	V <sub>CEO</sub>	350	V
Emitter-Collector Voltage	V <sub>ECO</sub>	2	V
Collector Current	I <sub>CE</sub>	200	mA
Supply Voltage (Referenced to V <sub>SS</sub> )	V <sub>CC</sub>	15	V
Output DC Current	I <sub>OC</sub>	20	mA
Power Dissipation (Shunt Regulator)	P <sub>A</sub>	30	mW
Power Dissipation, Darlington Transistor <sup>1</sup>	P <sub>D</sub>	250	mW
Total Power Dissipation <sup>1</sup>	P <sub>T</sub>	250	mW
ESD Rating (Human Body Model)	-	2	kV
Operating Temperature	T <sub>OPR</sub>	-40 to +85	°C
Storage Temperature	T <sub>STG</sub>	-55 to +130	°C

<sup>1</sup> Derate linearly 2.83 mW/°C.

Unless otherwise specified, Absolute Maximum electrical ratings are at 25°C.

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied.

Typical values are characteristic of the device at 25°C, and are the result of engineering evaluations. They are provided for information purposes only, and are not part of the manufacturing testing requirements.

### 1.4 Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Input Characteristics @25°C (Unless Otherwise Specified)</b>						
Supply voltage	$V_{CC}$	$T_A=-40^{\circ}\text{C to }+85^{\circ}\text{C}$	1.3	-	12.5	V
Reference voltage <sup>1</sup>	$V_{REF}$	$V_{CC}=1.6\text{V, }I_{OC}=10\text{mA (Fig. 1)}$				V
		$T_A=25^{\circ}\text{C}$	1.286	1.299	1.312	
		$T_A=-40^{\circ}\text{C to }+85^{\circ}\text{C}$	1.280	1.299	1.318	
Deviation of $V_{REF}$ over temperature <sup>2</sup>	$V_{REF(DEV)}$	$V_{CC}=1.6\text{V, }I_{OC}=10\text{mA, }T_A=-40^{\circ}\text{C to }+85^{\circ}\text{C (Fig. 1)}$	-	8	21	mV
Ratio of $V_{REF}$ variation to $V_{CC}$ change	$\Delta V_{REF}/\Delta V_{CC}$	$1.3\text{V} \leq V_{CC} \leq 12.5\text{V, }I_{OC}=10\text{mA (Fig. 1)}$	-	-0.37	-2.7	mV/V
FB input bias current	$I_{IB}$	$V_{CC}=1.6\text{V, }I_{OC}=10\text{mA (Fig. 1)}$	0.1	0.34	0.5	$\mu\text{A}$
Deviation of $I_{IB}$ over temperature <sup>2</sup>	$I_{IB(DEV)}$	$V_{CC}=1.6\text{V, }I_{OC}=10\text{mA, (Fig. 1)}$ $T_A=-40^{\circ}\text{C to }+85^{\circ}\text{C}$	-	0.4	0.6	$\mu\text{A}$
Quiescent bias current	$I_Q$	$V_{CC}=1.6\text{V, }V_{FB} = V_{REF, }I_{OC}=0\text{mA (Fig. 3)}$	-	75	100	$\mu\text{A}$
Error amplifier Off-State current	$I_{CC(off)}$	$V_{OC}=V_{CC}=12.5\text{V, }V_{FB}=0\text{V (Fig. 2)}$		0.001	0.1	$\mu\text{A}$
Shunt Transconductance <sup>3</sup>	$g_m (\Delta I_{OC}/\Delta V_{FB})$	$V_{CC}=1.6\text{V, }I_{OC} = 0.2\text{mA to }10\text{mA, }f=1\text{kHz}$	-	1	-	S
<b>Darlington Characteristics @25°C (Unless Otherwise Specified)</b>						
Collector-emitter voltage breakdown	$BV_{CEO}$	$I_{CE}=100\mu\text{A}$	350	-	-	V
Collector current	$I_{CE}$	$V_{CE}=200\text{V, }R_B=1\text{M}\Omega \text{ (Fig. 4)}$	-	-	100	nA
Base-emitter On voltage	$V_{BE(ON)}$	$I_{CE}=40\text{mA, }V_{CE}=2\text{V}$	-	-	1.8	V
Collector-emitter saturation voltage	$V_{CE(SAT)}$	$I_C=100\text{mA, }I_B=150\mu\text{A}$	-	-	1.2	V
Current gain	$h_{FE}$	$I_{CE}=40\text{mA, }V_{CE}=2\text{V}$	2500	-	40000	-

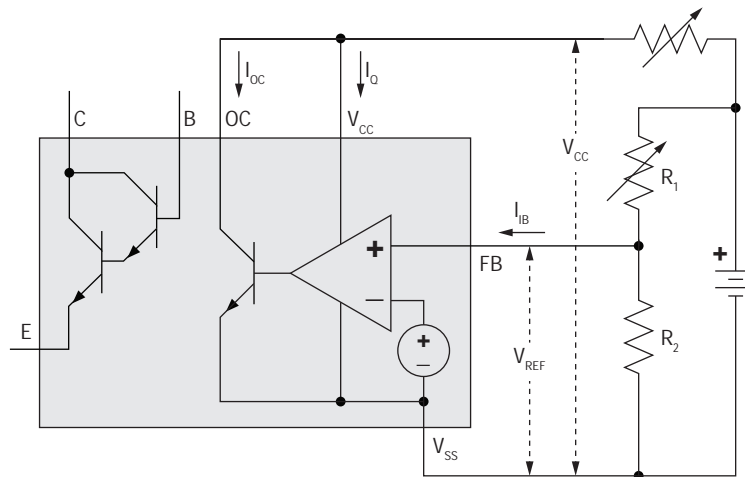
1 Reference voltage measured at Pin FB under the specified conditions.

2 Deviation parameters  $V_{REF(DEV)}$  and  $I_{IB(DEV)}$  are defined as the difference between the minimum and maximum values obtained over the rated temperature range.

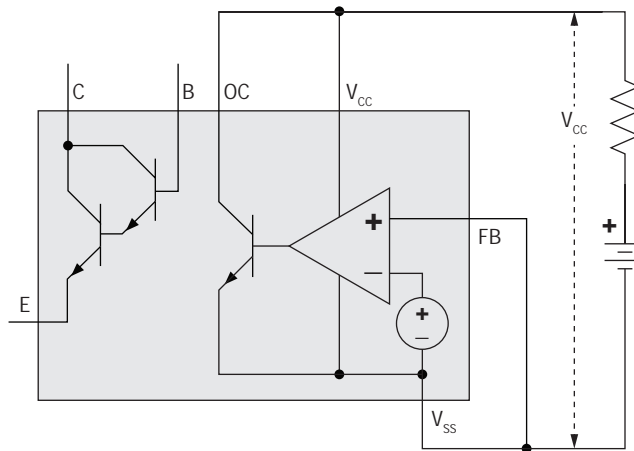
3 With two external resistors, the total shunt transconductance of the circuit is defined as:  $g'_m = \frac{g_m}{1 + \frac{R_1}{R_2}}$

### 1.5 Test Diagrams

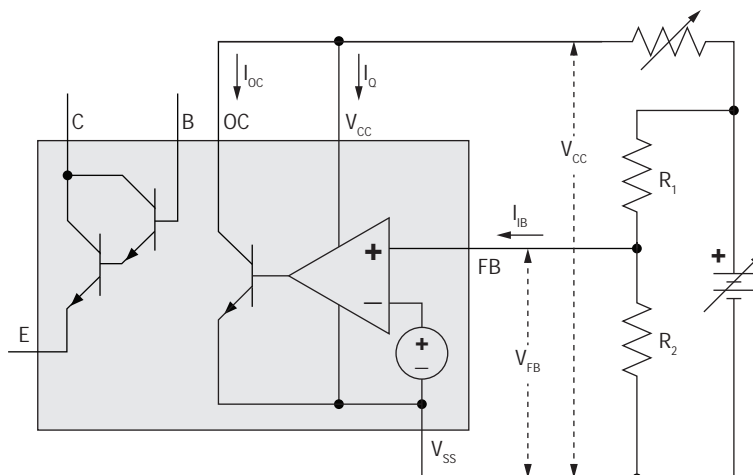
Figure 1:  $V_{REF}, I_{IB}, \Delta V_{REF}/\Delta V_{CC}, g_m$  Test Circuit



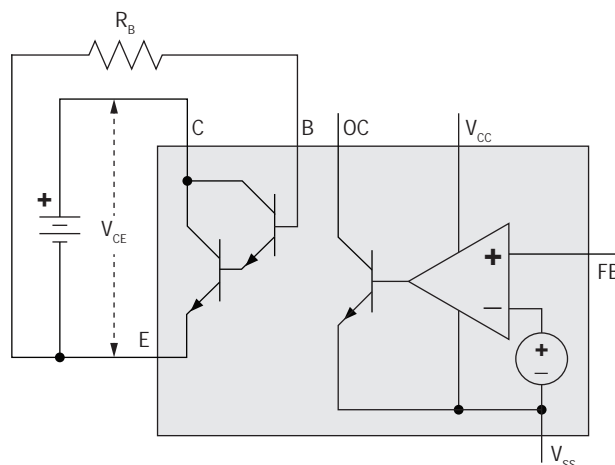
**Figure 2:  $I_{CC(OFF)}$  Test Circuit**



**Figure 3:  $I_Q$  Test Circuit**

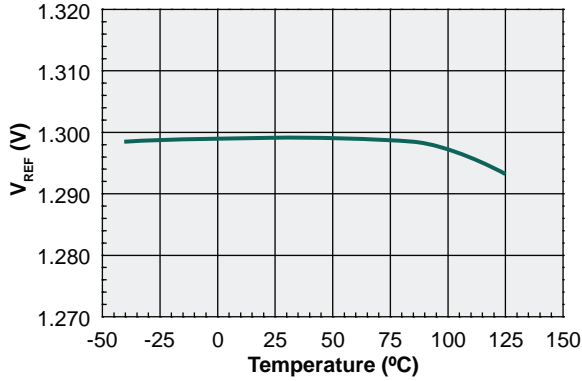


**Figure 4:  $I_{CE}$  Test Circuit**

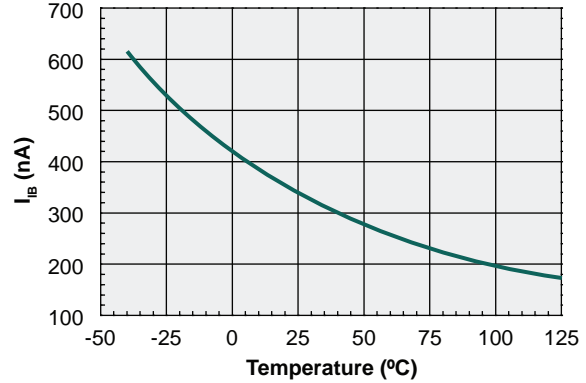


1.6 Performance Data

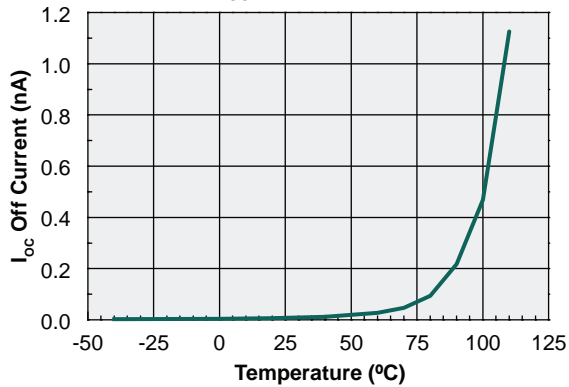
**$V_{REF}$  vs. Temperature**



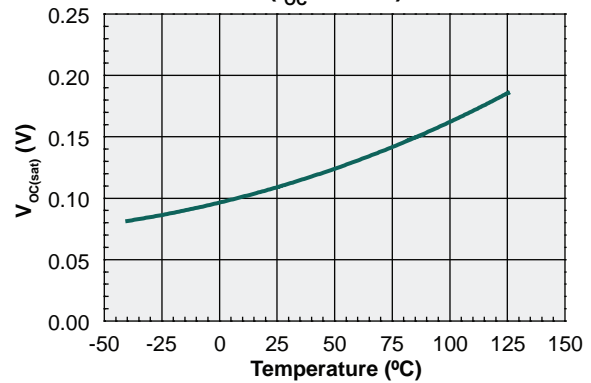
**FB Input Bias Current vs. Temperature  
( $I_{OC}=10mA$ )**



**Off-State Current vs. Temperature  
( $V_{OC}=13.2V, V_{FB}=0V$ )**



**Saturation Voltage vs. Temperature  
( $I_{OC}=10mA$ )**





always into pin FB). This error causes the regulated output voltage to increase which increases the current through  $R_1$  by an amount equal to  $I_{IB}$ , thereby restoring the current through  $R_2$  to its original value. Reducing the  $V_{REG}$  error created by the input bias current to less than 1% is accomplished by setting the value of  $R_1$  using the following formula:

$$R_1 < \frac{V_{REG}}{50\mu A}$$

Where:

$$50\mu A = 100 \cdot I_{IB(MAX)}$$

## 2.2 Compensation

The dominate pole of the error amplifier is around 13kHz. In a typical system with a low-bandwidth requirement, it doesn't need any external compensation. Frequency response of the system can be optimized for the specific application by placing a compensation network between the OC and FB pins of the IX9915. For designs with more critical bandwidth requirements, measurement of the loop response must be made and compensation adjusted as necessary.

## 2.3 Design Example

A design example for the bleeder circuitry in LED lamp exhibits the detailed steps. In this example, it will target the predetermined voltage  $V_{LINE-TH}=25V$  and maximum bleeding current  $I_{H-MAX}=25mA$ .

In order to flow the maximum bleeding current  $I_{H-MAX}$  through the Darlington transistor:

$$V_{REG} = I_{H-MAX} \cdot R_E + V_{BE} \quad (1)$$

If taking  $R_E=100\Omega$ :

$$\begin{aligned} V_{REG} &= I_{H-MAX} \cdot R_E + V_{BE} \\ &= 25mA \cdot 100\Omega + 1.5V \\ &= 4V \end{aligned}$$

In fact, the components in the dashed rectangle function as a comparator, its gain:

$$\begin{aligned} A &= \frac{R_0 \cdot R_2 \cdot g_m}{R_1 + R_2} \\ \frac{R_2}{R_1 + R_2} &= \frac{V_{REF}}{V_{REG}} = \frac{1.299V}{4V} = 0.325 \\ g_m &= 1S \text{ (typical)} \end{aligned}$$

If taking  $R_0=40k\Omega$ , the gain of the comparator is around 82dB. That is to say, once the error amplifier starts to regulate, the Darlington transistor will be shut off by this comparator. So,  $I_{OC}$  can be ignored for affecting the predetermined voltage:

$$V_{LINE-TH} \approx V_{REG} + (I_1 + I_Q) \cdot R_3 \quad (2)$$

Almost full power supply voltage will cross over  $R_3$ , taking  $R_3=100k\Omega$  to minimize its power consumption:

$$P = \frac{(V_{rms})^2}{100k\Omega}$$

Substituting:

- $I_Q=75\mu A$ ,
- $I_1=V_{REF} / R_2$ ,
- $V_{LINE-TH}=25V$

into formula (2):

$$\begin{aligned} R_2 &\approx 9.6k\Omega \\ R_1 &= R_2 \cdot \left( \frac{V_{REG}}{V_{REF}} - 1 \right) \\ R_1 &\approx 20k\Omega \end{aligned}$$



### 3. Manufacturing Information

#### 3.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. IXYS Integrated Circuits Division classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IX9915N	MSL 1

#### 3.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

#### 3.3 Soldering Profile

Provided in the table below is the Classification Temperature ( $T_C$ ) of this product and the maximum dwell time the body temperature of this device may be ( $T_C - 5$ )°C or greater. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through-hole devices, and any other processes, the guidelines of **J-STD-020** must be observed.

Device	Classification Temperature ( $T_C$ )	Dwell Time ( $t_p$ )	Max Reflow Cycles
IX9915N	260°C	30 seconds	3

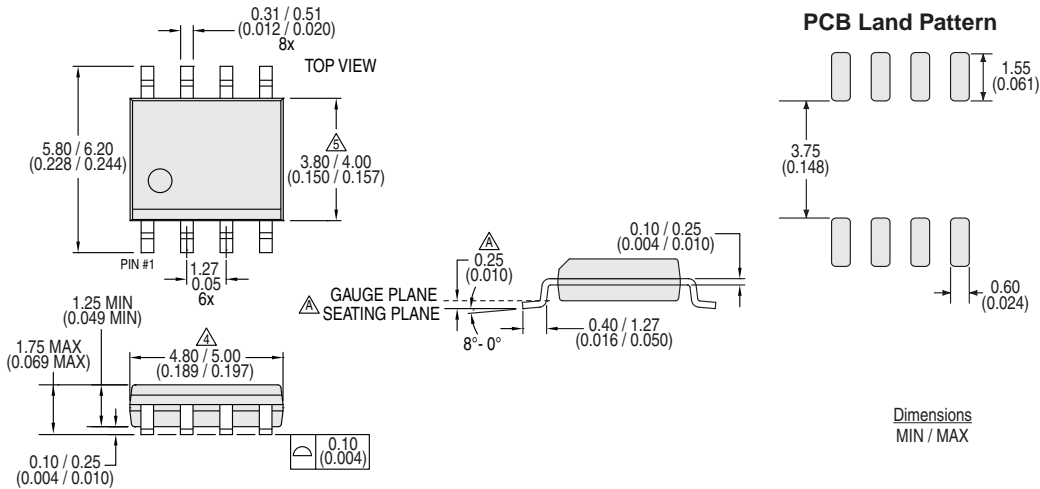
#### 3.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based.



### 3.5 Mechanical Dimensions

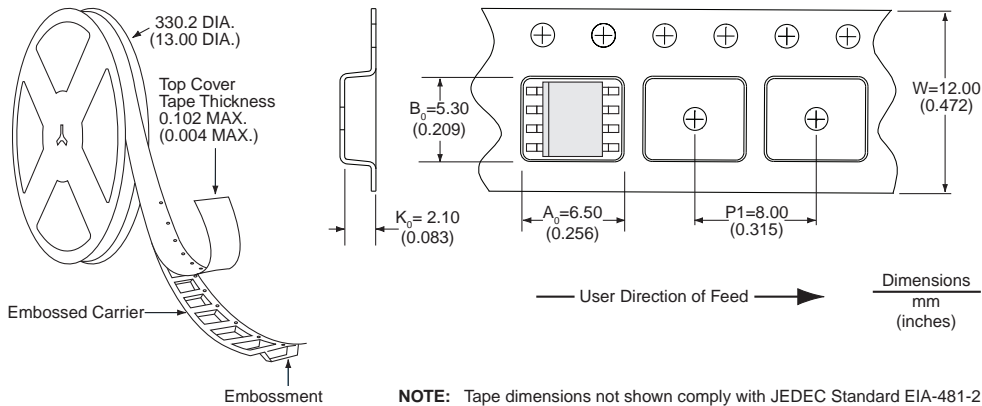
#### 3.5.1 IX9915N 8-Pin SOIC Package



Notes:

1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation AA, Rev. F.
- △ Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per end.
- △ Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
6. Lead thickness includes plating.

#### 3.5.2 IX9915NTR Tape & Reel



NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

For additional information please visit [www.ixysic.com](http://www.ixysic.com)

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