IXYS

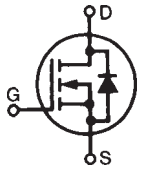
Preliminary Technical Information

Polar3™ HiperFET™ Power MOSFET

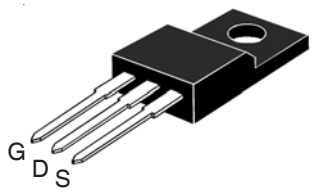
IXFP20N50P3M

V_{DSS} = 500V
I_{D25} = 8A
$R_{DS(on)}$ ≤ 300mΩ

N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Rectifier



OVERMOLDED



G = Gate D = Drain
S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	500	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	500	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	T_C = 25°C	8	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	40	A
I_A	T_C = 25°C	10	A
E_{AS}	T_C = 25°C	300	mJ
dv/dt	$I_S \le I_{DM}$, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$	35	V/ns
P_D	T_C = 25°C	58	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	Plastic Body for 10s	260	°C
M_d	Mounting Torque	1.13 / 10	Nm/lb.in
Weight		2.5	g

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 1mA	500			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 1.5mA	3.0		5.0	V
I_{GSS}	V_{GS} = ±30V, V_{DS} = 0V			±100	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0V			25	μA
	T_J = 125°C			1.25	mA
$R_{DS(on)}$	V_{GS} = 10V, I_D = 10A, Note 1			300	mΩ

Features

- Plastic Overmolded Tab for Electrical Isolation
- Fast Intrinsic Rectifier
- Avalanche Rated
- Low $R_{DS(ON)}$ and Q_G
- Low Package Inductance

Advantages

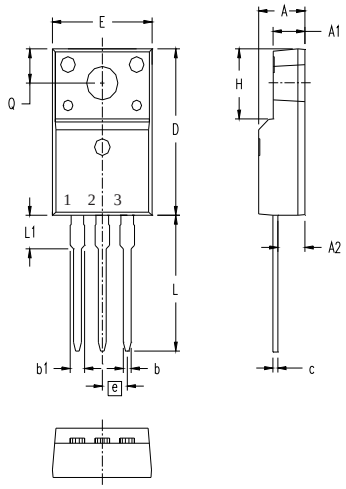
- High Power Density
- Easy to Mount
- Space Savings

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- DC-DC Converters
- Laser Drivers
- AC and DC Motor Drives
- Robotics and Servo Controls

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS} = 20V, I_D = 10A, Note 1	11	18		S
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		1800		pF
C_{oss}			230		pF
C_{rss}			8.3		pF
R_{Gi}	Gate Input Resistance		2.3		Ω
$t_{d(on)}$	**Resistive Switching Times**		10		ns
t_r	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 10A		5		ns
$t_{d(off)}$	R_G = 5Ω (External)		43		ns
t_f			9		ns
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 10A		36		nC
Q_{gs}			7		nC
Q_{gd}			13		nC
R_{thJC}				2.15	°C/W

ISOLATED TO-220 (IXFP...M)



Terminals: 1 - Gate
2 - Drain
3 - Source

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.177	.193	4.50	4.90
A1	.092	.108	2.34	2.74
A2	.101	.117	2.56	2.96
b	.028	.035	0.70	0.90
b1	.050	.058	1.27	1.47
c	.018	.024	0.45	0.60
D	.617	.633	15.67	16.07
E	.392	.408	9.96	10.36
e	.100 BSC		2.54 BSC	
H	.255	.271	6.48	6.88
L	.499	.523	12.68	13.28
L1	.119	.135	3.03	3.43
ØP	.121	.129	3.08	3.28
Q	.126	.134	3.20	3.40

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0V			20	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			80	A
V_{SD}	I_F = I_S, V_{GS} = 0V, Note 1			1.4	V
t_{rr}	I_F = 10A, -di/dt = 100A/μs			250	ns
I_{RM}	V_R = 100V, V_{GS} = 0V		8.0		A
Q_{RM}			0.6		μC

Note 1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

PRELIMANARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

Fig. 1. Output Characteristics @ T_J = 25ºC

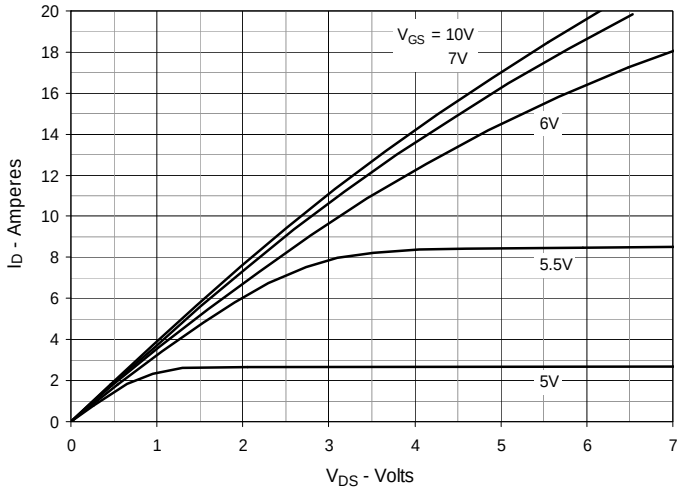


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

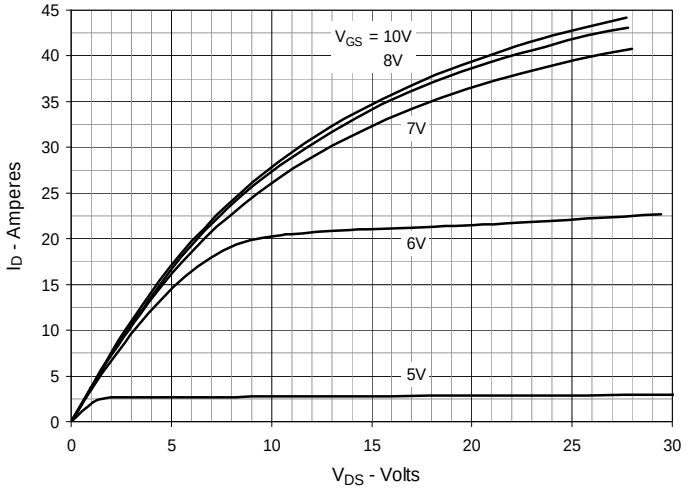


Fig. 3. Output Characteristics @ T_J = 125ºC

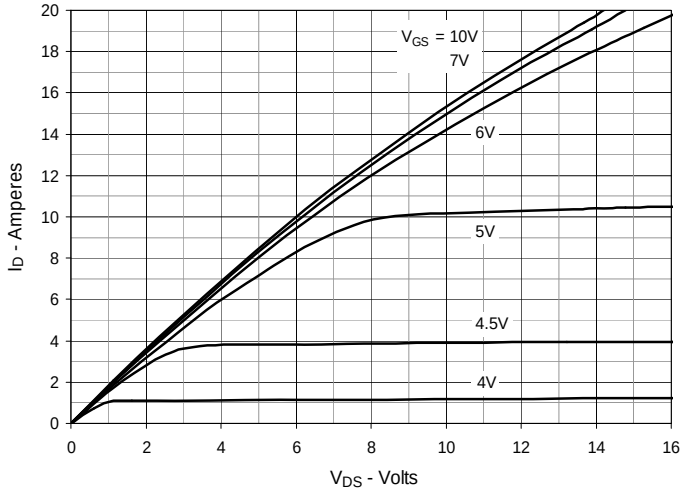


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 10A Value vs. Junction Temperature

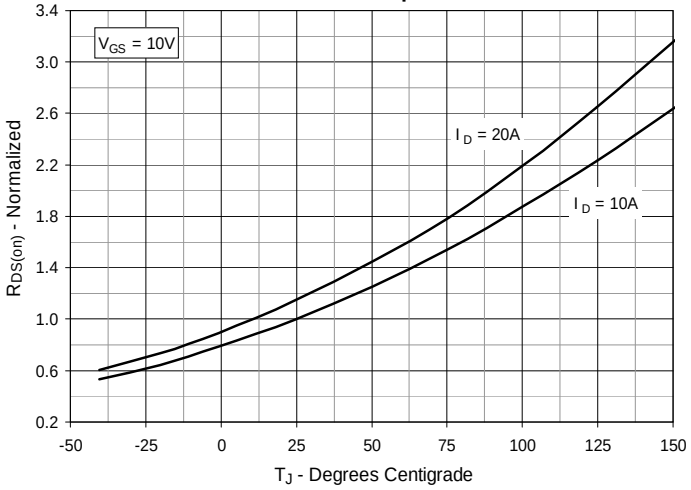


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 10A Value vs. Drain Current

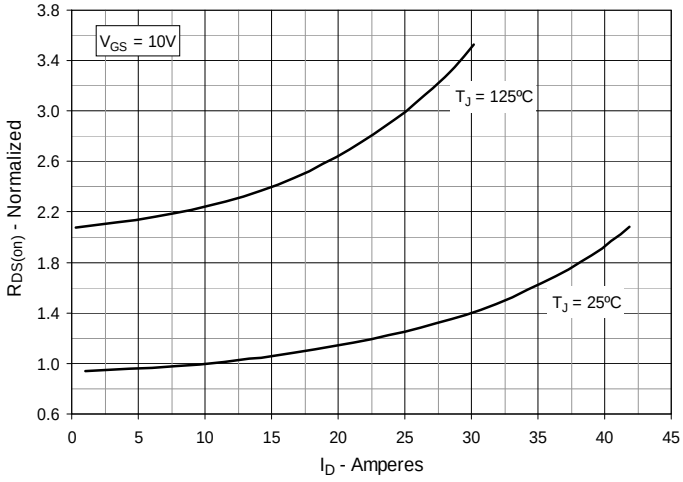


Fig. 6. Maximum Drain Current vs. Case Temperature

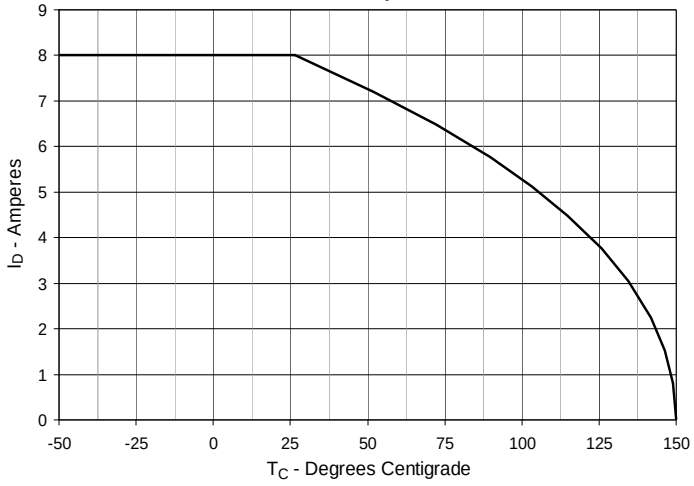


Fig. 7. Input Admittance

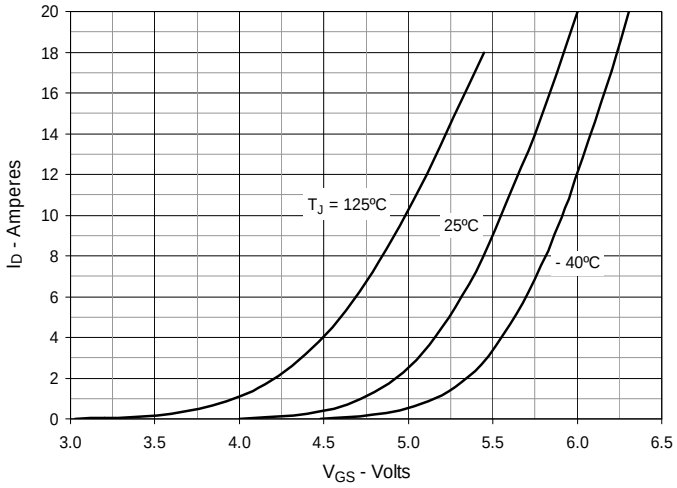


Fig. 8. Transconductance

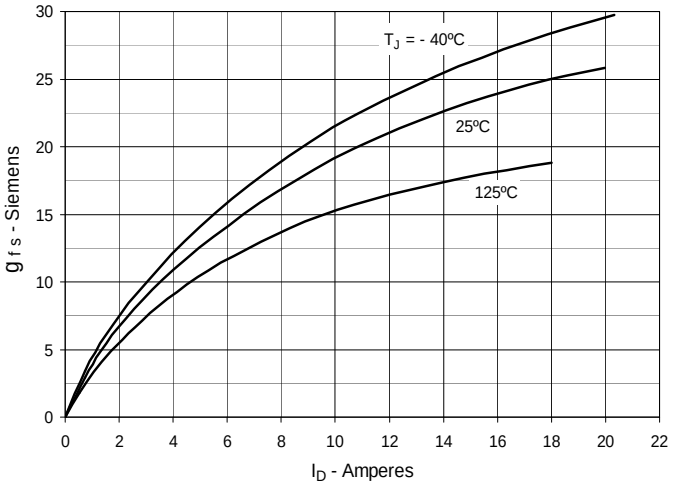


Fig. 9. Forward Voltage Drop of Intrinsic Diode

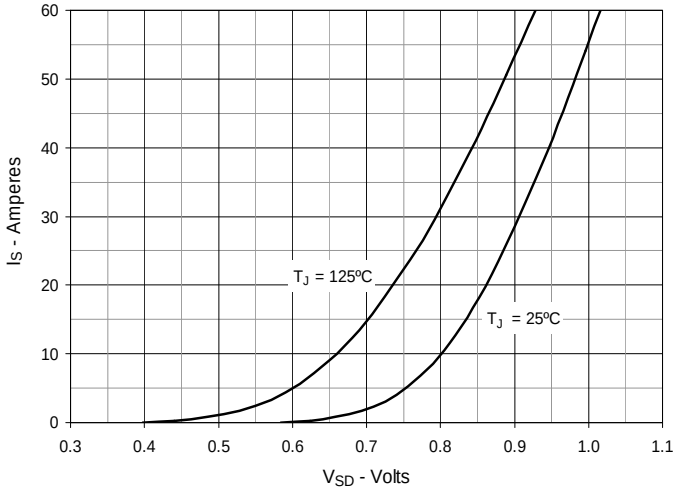


Fig. 10. Gate Charge

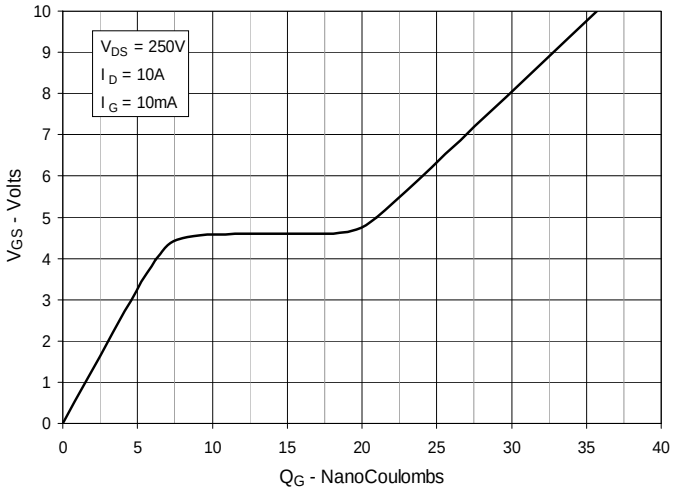


Fig. 11. Capacitance

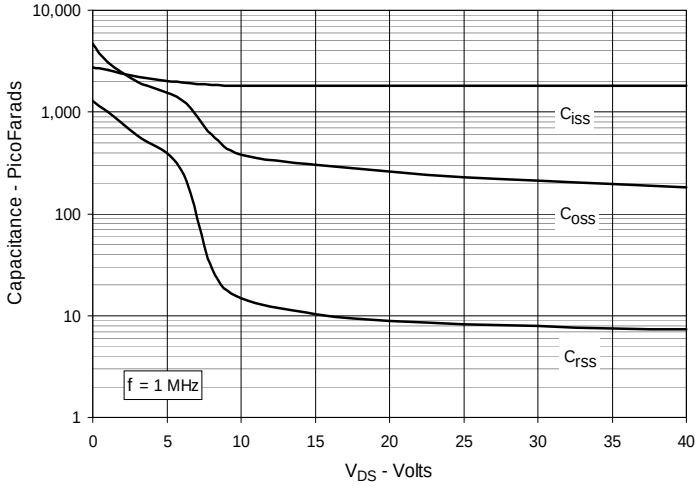


Fig. 12. Forward-Bias Safe Operating Area

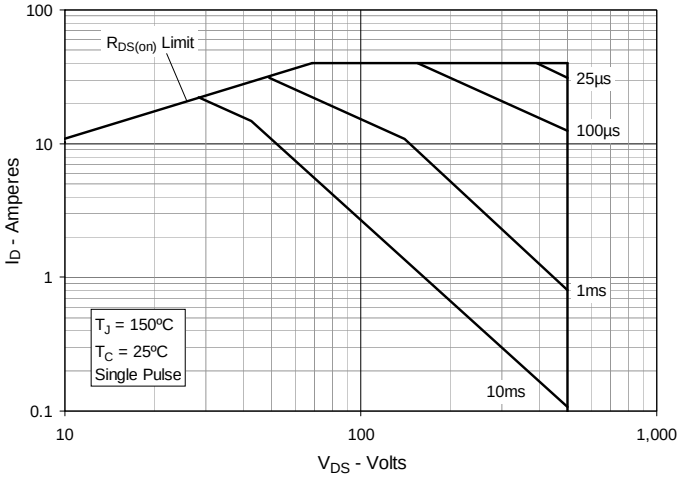
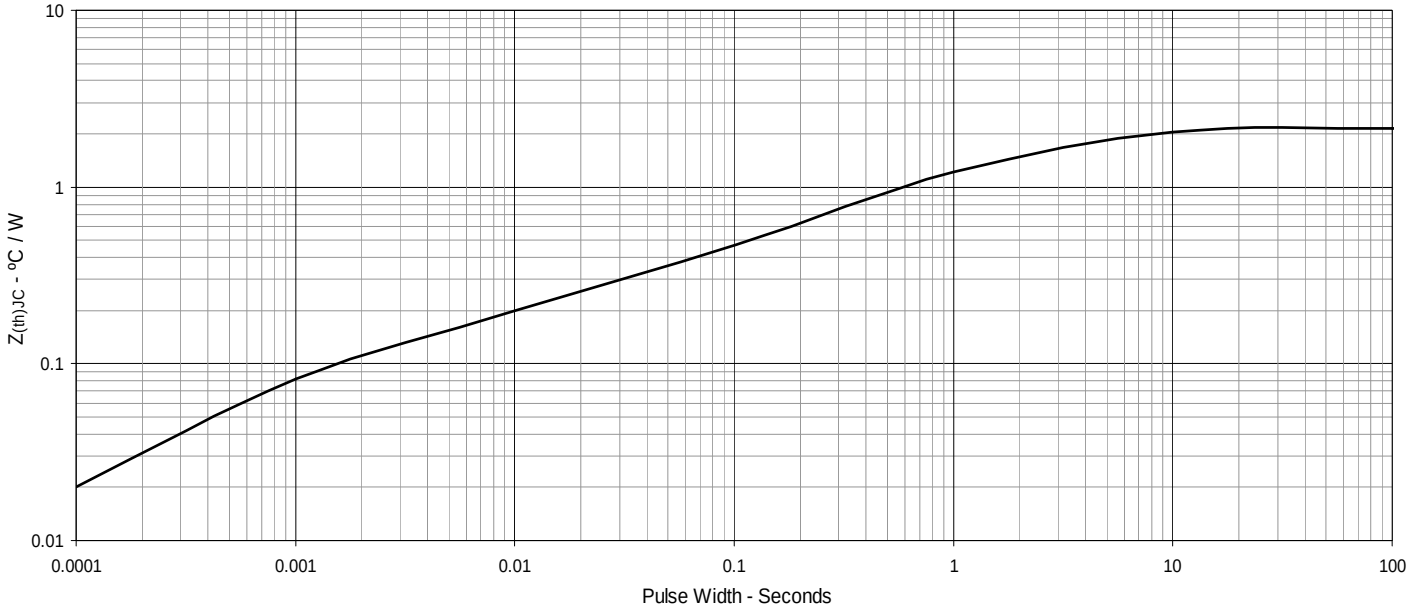


Fig. 13. Maximum Transient Thermal Impedance



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