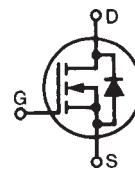


**PolarHV™ HiPerFET
Power MOSFET
ISOPLUS247™
(Electrically Isolated Back Surface)**

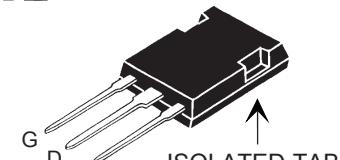
N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode

IXFR 180N15P



V_{DSS} = 150 V
I_{D25} = 100 A
R_{DS(on)} ≤ 13 mΩ
t_{rr} ≤ 200 ns

ISOPLUS247 (IXFR)



G = Gate
S = Source
D = Drain

Symbol	Test Conditions	Maximum Ratings		
V_{DSS}	T _J = 25°C to 175°C	150	V	
V_{DGR}	T _J = 25°C to 175°C; R _{GS} = 1 MΩ	150	V	
V_{GSS}	Continuous	±20	V	
V_{GSM}	Transient	±30	V	
I_{D25}	T _C = 25°C	100	A	
I_{D(RMS)}	External Lead current limit	75	A	
I_{DM}	T _C = 25°C, pulse width limited by T _{JM}	380	A	
I_{AR}	T _C = 25°C	60	A	
E_{AR}	T _C = 25°C	100	mJ	
E_{AS}	T _C = 25°C	4	J	
dv/dt	I _S ≤ I _{DM} , di/dt ≤ 100 A/μs, V _{DD} ≤ V _{DSS} , T _J ≤ 150°C, R _G = 4 Ω	10	V/ns	
P_D	T _C = 25°C	300	W	
T_J		-55 ... +175	°C	
T_{JM}		175	°C	
T_{stg}		-55 ... +150	°C	
T_L	1.6 mm (0.062 in.) from case for 10 s	300	°C	
V_{ISOL}	50/60 Hz, RMS, 1 minute	2500	V~	
F_d	Mounting force	20..120 / 4.5..26	N/lb	
Weight		5	g	

Symbol	Test Conditions (T _J = 25°C, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
V_{DSS}	V _{GS} = 0 V, I _D = 250 μA	150		V
V_{GS(th)}	V _{DS} = V _{GS} , I _D = 4 mA	2.5		5.0 V
I_{GSS}	V _{GS} = ±20 V _{DC} , V _{DS} = 0			±100 nA
I_{DSS}	V _{DS} = V _{DSS} , V _{GS} = 0 V T _J = 150°C			25 μA 1.5 mA
R_{DS(on)}	V _{GS} = 10 V, I _D = I _T , Note 1			13 mΩ

Features

- | International standard isolated package
- | UL recognized package
- | Silicon chip on Direct-Copper-Bond substrate
 - High power dissipation
 - Isolated mounting surface
 - 2500V electrical isolation
- | Unclamped Inductive Switching (UIS) rated
- | Low package inductance
 - easy to drive and to protect
- | Fast intrinsic diode

Advantages

- | Easy to mount
- | Space savings
- | High power density

Symbol **Test Conditions****Characteristic Values**(T_J = 25°C, unless otherwise specified)

Min. | Typ. | Max.

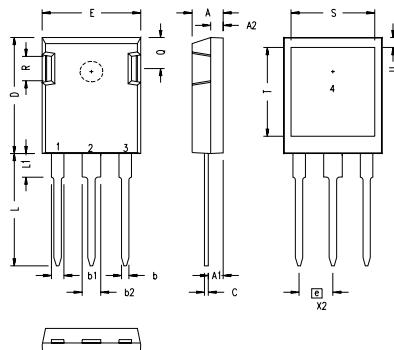
g_{fs}	V _{DS} = 10 V; I _D = I _T , Notes 1, 2	55	86	S
C_{iss} C_{oss} C_{rss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz	7000		pF
		2250		pF
		515		pF
t_{d(on)} t_r t_{d(off)} t_f	V _{GS} = 10 V, V _{DS} = 0.5 V _{DSS} , I _D = 60A R _G = 3.3 Ω (External)	30		ns
		32		ns
		150		ns
		36		ns
Q_{g(on)} Q_{gs} Q_{gd}	V _{GS} = 10 V, V _{DS} = 0.5 V _{DSS} , I _D = I _T	240		nC
		55		nC
		140		nC
R_{thJC}			0.5	°C/W
R_{thCS}		0.15		°C/W

Source-Drain Diode**Characteristic Values**(T_J = 25°C, unless otherwise specified)

Symbol	Test Conditions	min.	typ.	max.
I_s	V _{GS} = 0 V		180	A
I_{SM}	Repetitive		380	A
V_{SD}	I _F = I _S , V _{GS} = 0 V, Note 1		1.5	V
t_{rr} Q_{RM} I_{RM}	I _F = 25A, -di/dt = 100 A/μs V _R = 100V, V _{GS} = 0V		200	ns
		0.6		μC
		6		A

Notes:

1. Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %;
2. Test current I_T = 90 A.

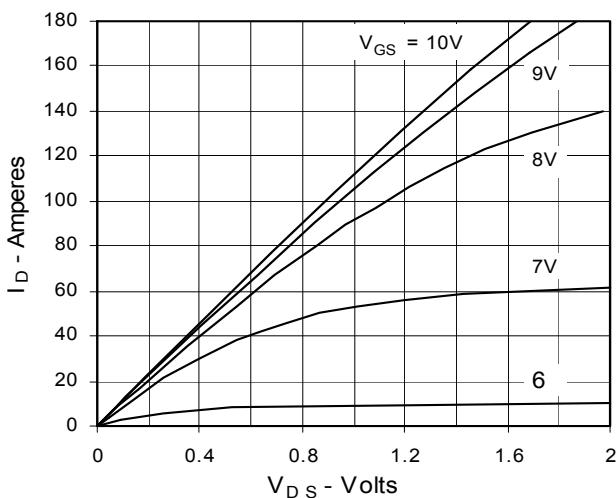
ISOPLUS247 Outline

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215	BSC	5.45	BSC
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

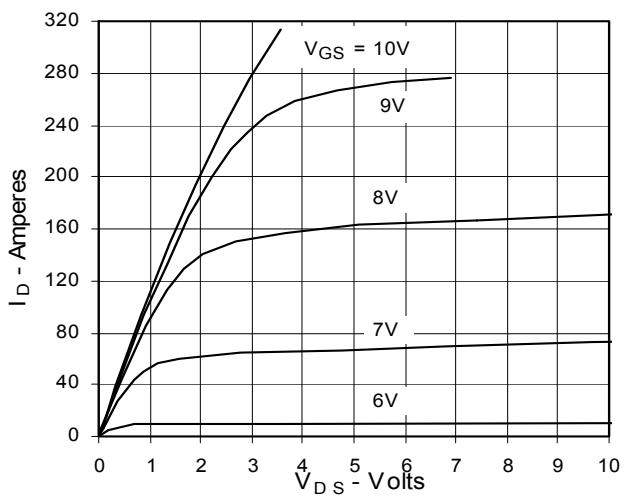
1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

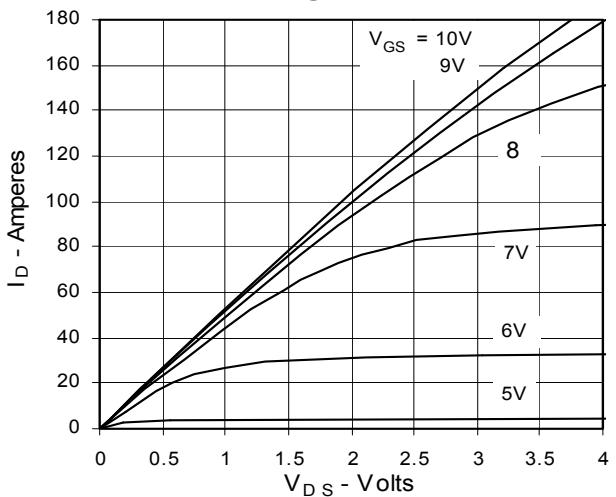
**Fig. 1. Output Characteristics
@ 25°C**



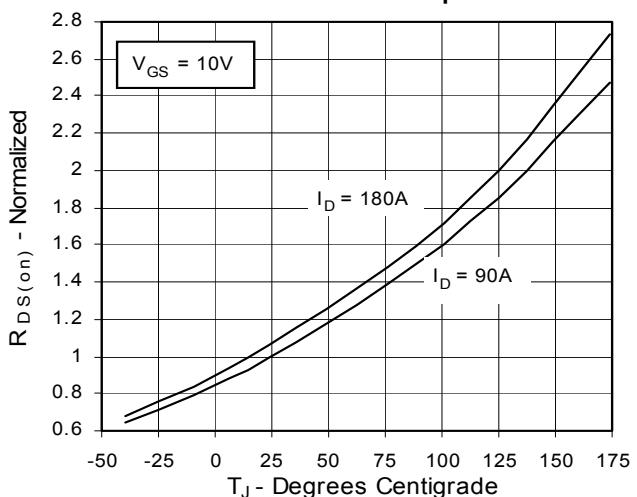
**Fig. 2. Extended Output Characteristics
@ 25°C**



**Fig. 3. Output Characteristics
@ 150°C**



**Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 90A$
Value vs. Junction Temperature**



**Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 90A$
Value vs. Drain Current**

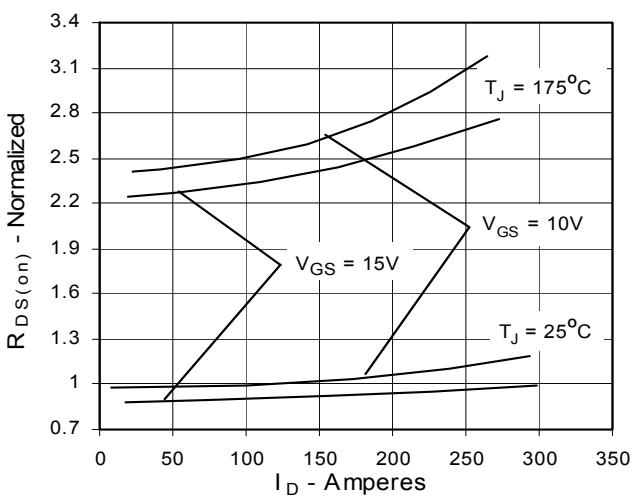


Fig. 6. Drain Current vs. Case Temperature

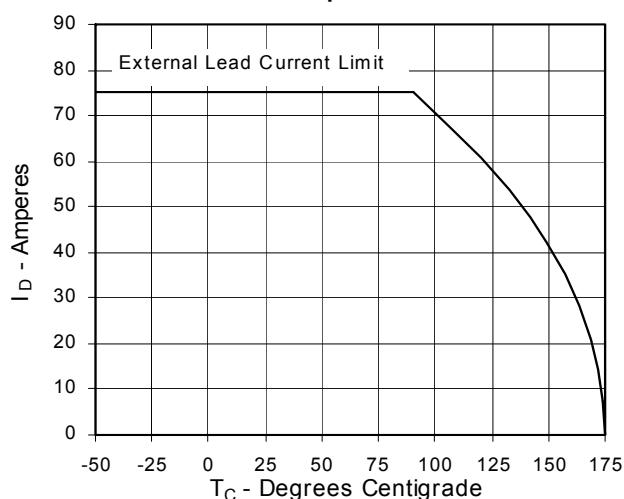


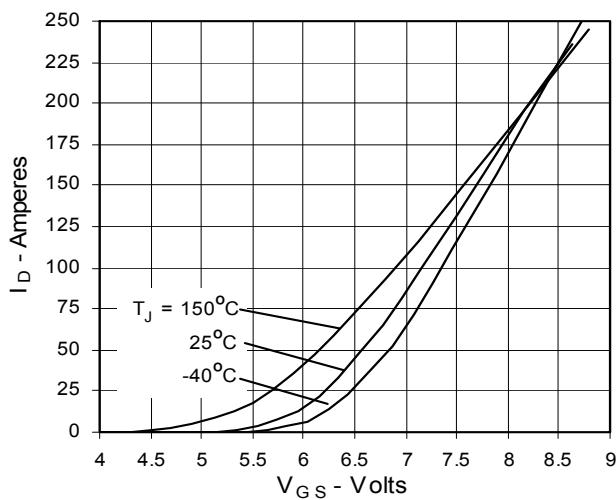
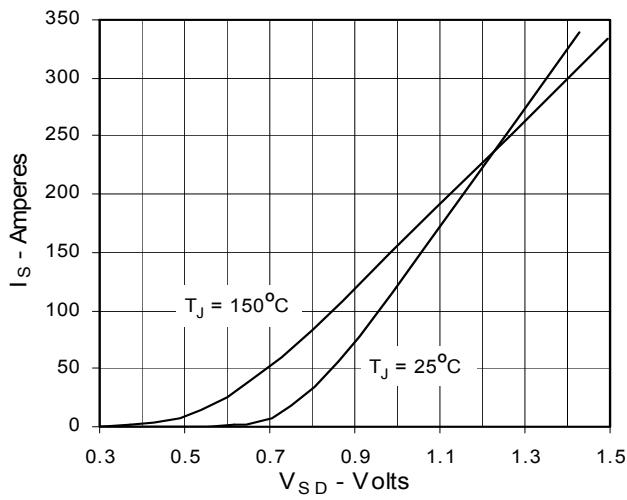
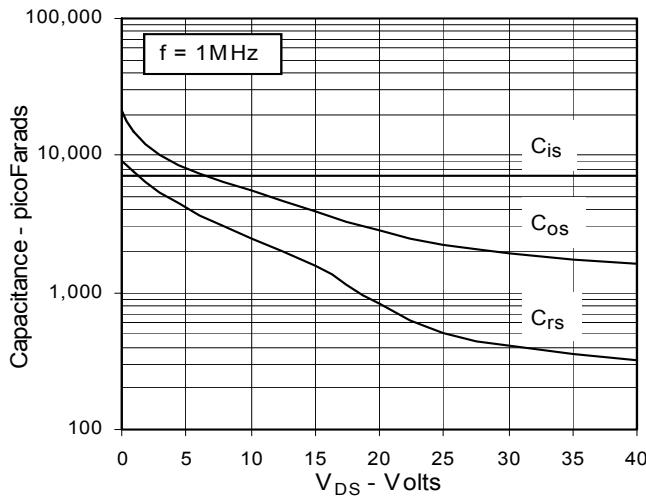
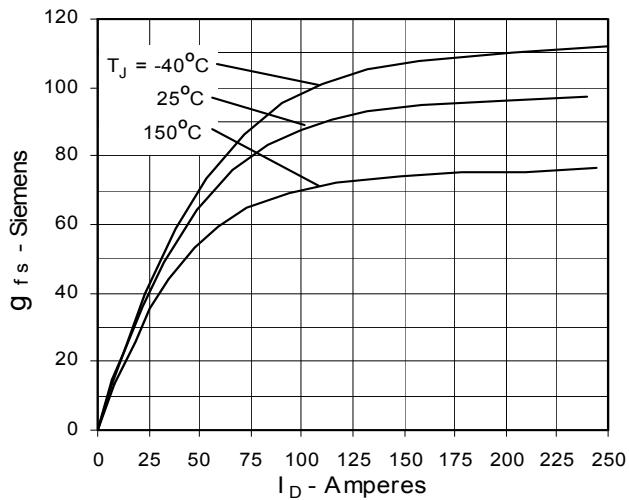
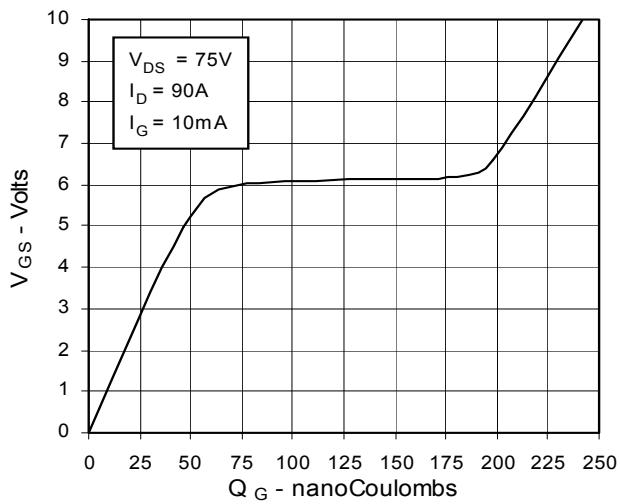
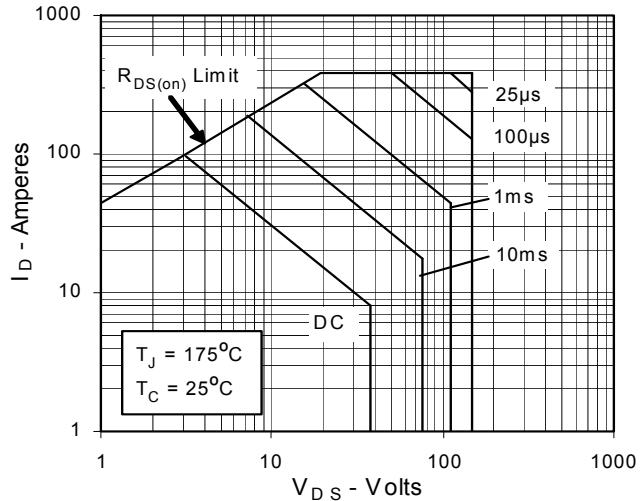
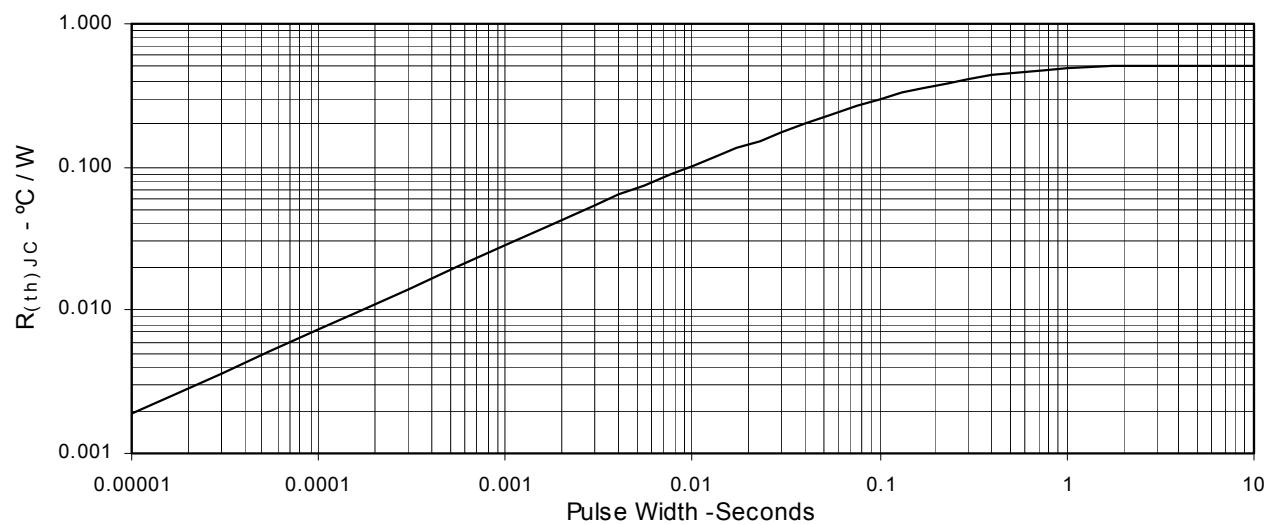
Fig. 7. Input Admittance**Fig. 9. Source Current vs. Source-To-Drain Voltage****Fig. 11. Capacitance****Fig. 8. Transconductance****Fig. 10. Gate Charge****Fig. 12. Forward-Bias Safe Operating Area**

Fig. 13. Maximum Transient Thermal Resistance



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