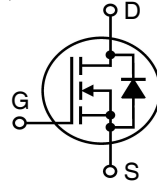


X2-Class HiPerFET™ Power MOSFET

IXFK120N65X2 IXFX120N65X2

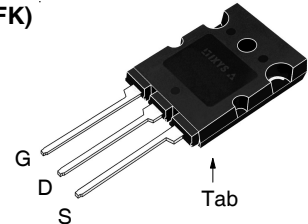
$V_{DSS} = 650V$
 $I_{D25} = 120A$
 $R_{DS(on)} \leq 24m\Omega$

N-Channel Enhancement Mode
 Avalanche Rated
 Fast Intrinsic Diode

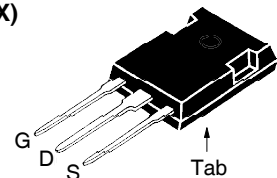


Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $150^\circ C$	650	V
V_{DGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GS} = 1M\Omega$	650	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	$T_C = 25^\circ C$	120	A
I_{DM}	$T_C = 25^\circ C$, Pulse Width Limited by T_{JM}	240	A
I_A	$T_C = 25^\circ C$	15	A
E_{AS}	$T_C = 25^\circ C$	3.5	J
P_D	$T_C = 25^\circ C$	1250	W
dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ C$	50	V/ns
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	$^\circ C$
M_d	Mounting Torque (TO-264)	1.13/10	Nm/lb.in
F_C	Mounting Force (PLUS247)	20..120 / 4.5..27	N/lb
Weight	TO-264	10	g
	PLUS247	6	g

TO-264
(IXFK)



PLUS247
(IXFX)



G = Gate D = Drain
 S = Source Tab = Drain

Features

- International Standard Packages
- Low Q_G
- Avalanche Rated
- Low Package Inductance

Advantages

- High Power Density
- Easy to Mount
- Space Savings

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- DC-DC Converters
- PFC Circuits
- AC and DC Motor Drives
- Robotics and Servo Controls

Symbol	Test Conditions ($T_J = 25^\circ C$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 3mA$	650		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 8mA$	3.5		5.0 V
I_{GSS}	$V_{GS} = \pm 30V$, $V_{DS} = 0V$			± 100 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ C$			50 μA 5 mA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 0.5 \cdot I_{D25}$, Note 1			24 m Ω

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max
g_{fs}	$V_{DS} = 10\text{V}$, $I_D = 0.5 \cdot I_{D25}$, Note 1	46	76	S
R_{Gi}	Gate Input Resistance		0.74	Ω
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		14	nF
C_{oss}			8700	pF
C_{rss}			5.5	pF
Effective Output Capacitance				
$C_{o(er)}$	Energy related	$V_{GS} = 0\text{V}$ $V_{DS} = 0.8 \cdot V_{DSS}$	455	pF
$C_{o(tr)}$	Time related		1930	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$ $R_G = 1\Omega$ (External)		39	ns
t_r			26	ns
$t_{d(off)}$			82	ns
t_f			12	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$		240	nC
Q_{gs}			87	nC
Q_{gd}			65	nC
R_{thJC}				0.10 $^\circ\text{C/W}$
R_{thCS}			0.15	$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			120 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			480 A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{V}$, Note 1			1.4 V
t_{rr}	$I_F = 60\text{A}$, $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}$, $V_{GS} = 0\text{V}$		220	ns
Q_{RM}			2.3	μC
I_{RM}			21.0	A

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
by one or more of the following U.S. patents:	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

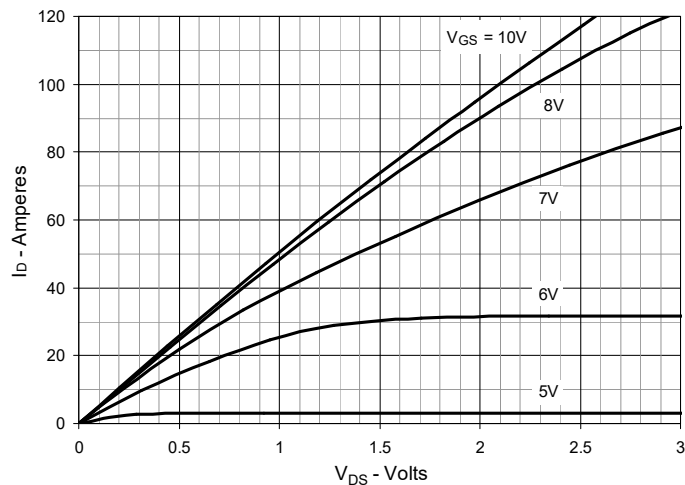


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

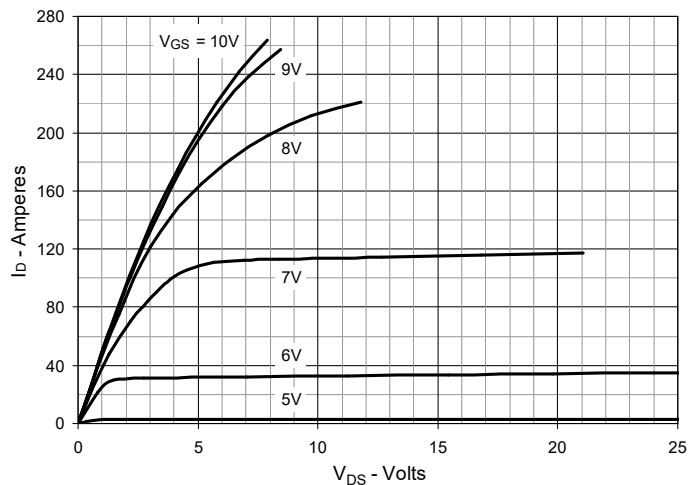


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

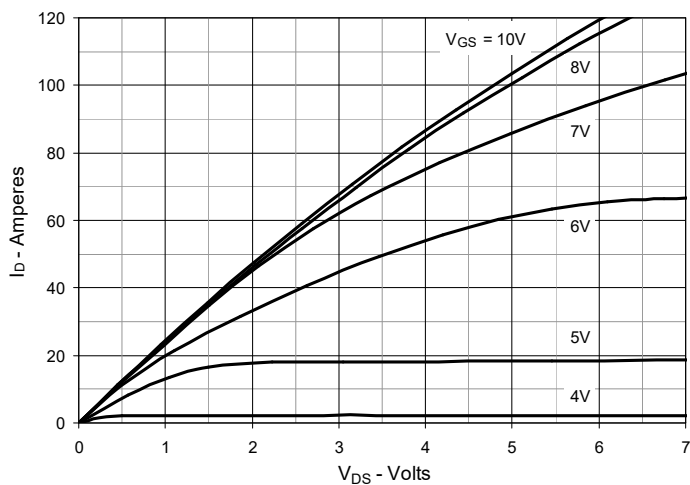


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 60\text{A}$ Value vs. Junction Temperature

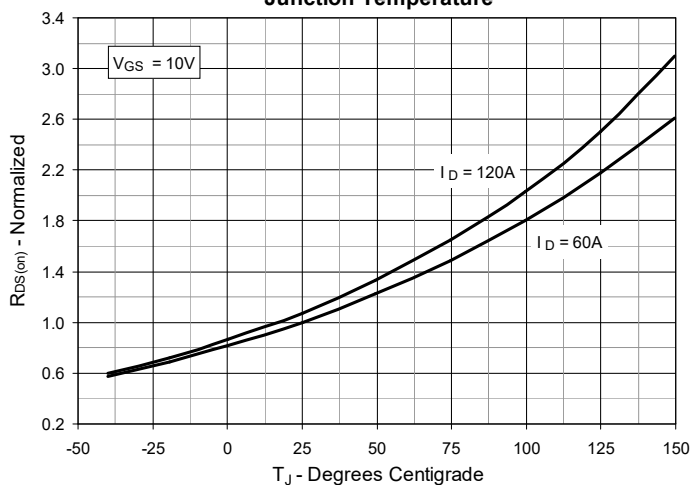


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 60\text{A}$ Value vs. Drain Current

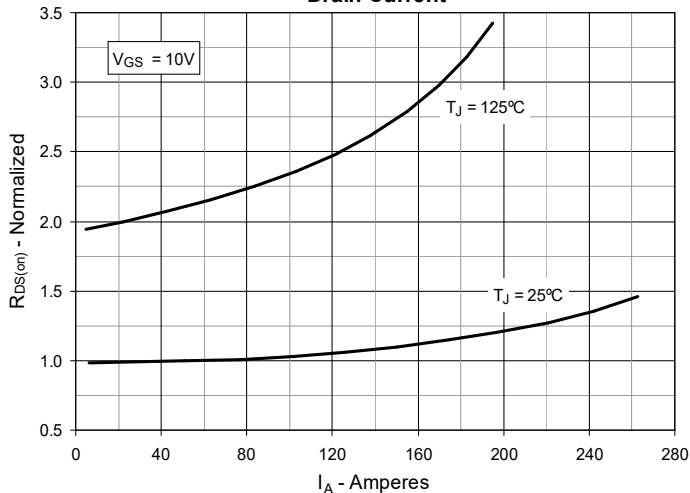


Fig. 6. Normalized Breakdown & Threshold Voltages vs. Junction Temperature

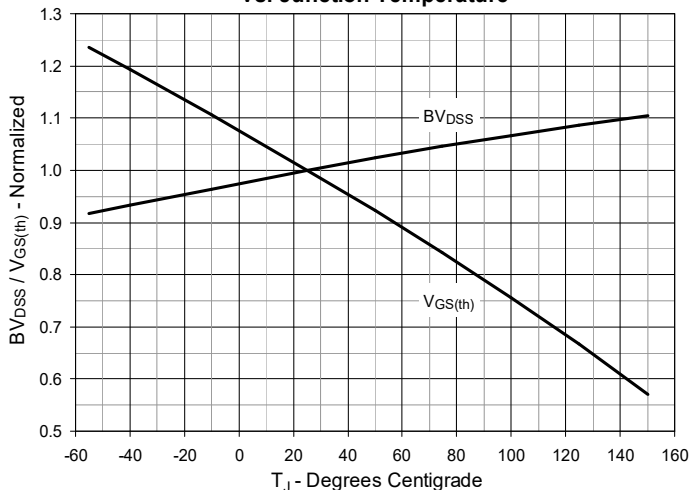


Fig. 7. Maximum Drain Current vs. Case Temperature

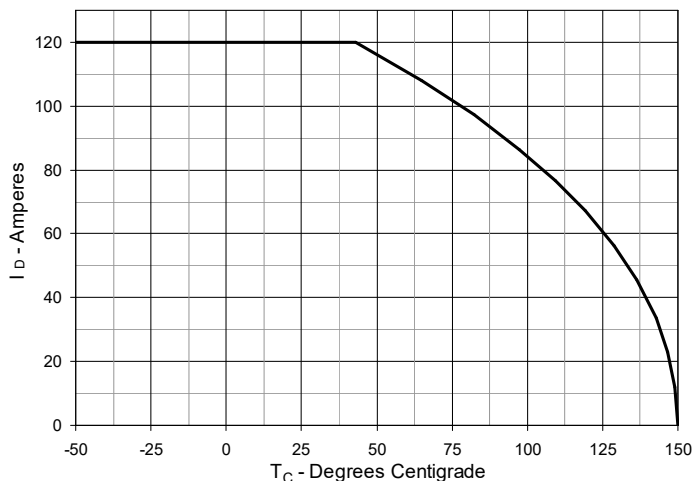


Fig. 8. Input Admittance

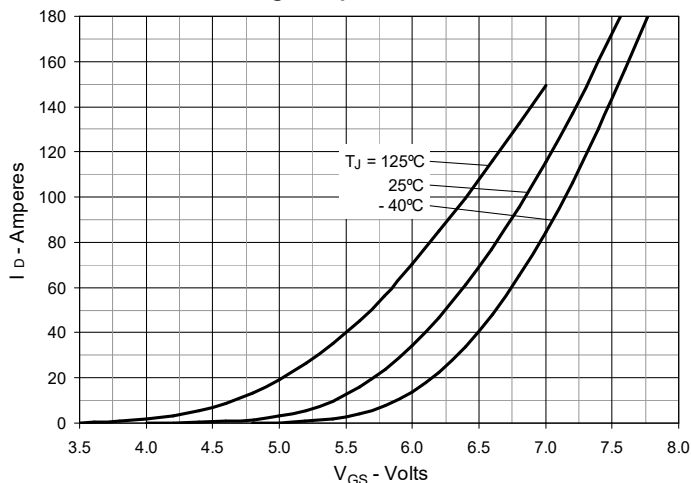


Fig. 9. Transconductance

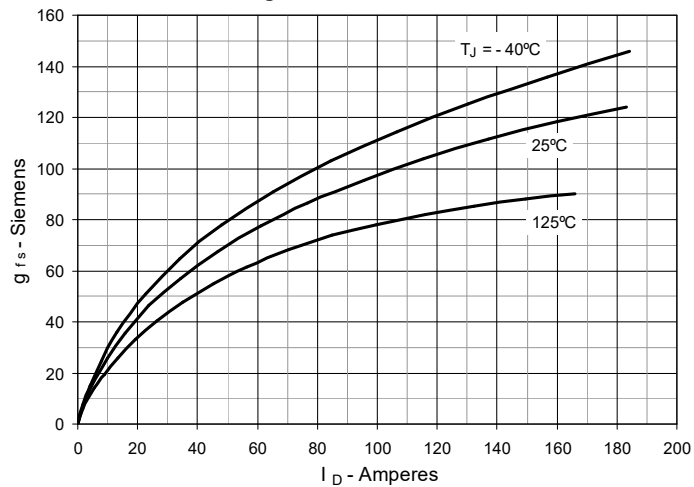


Fig. 10. Forward Voltage Drop of Intrinsic Diode

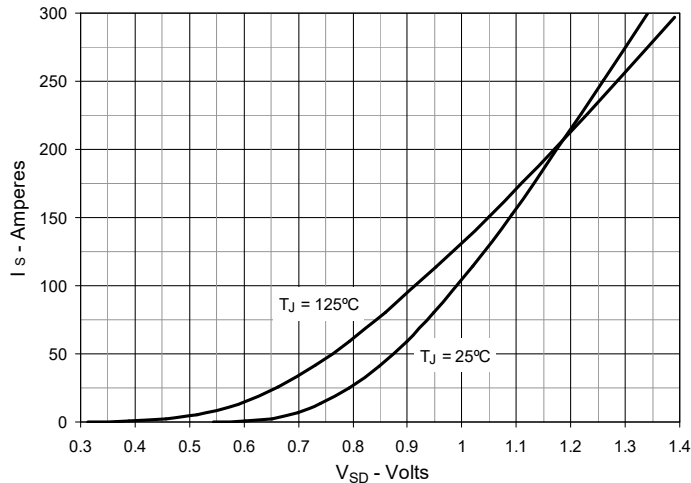


Fig. 11. Gate Charge

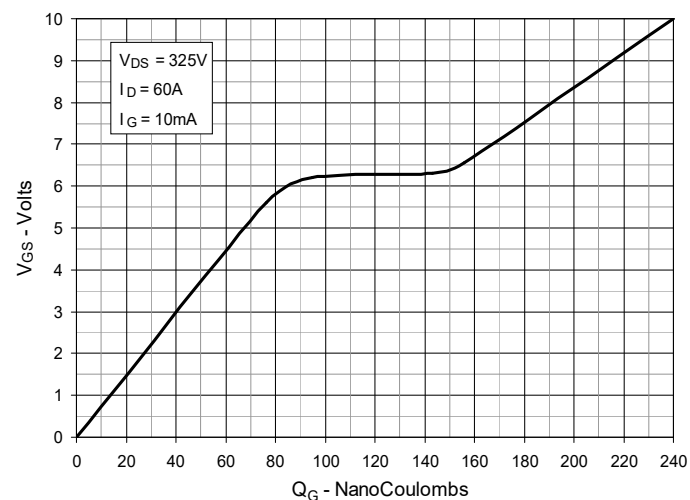


Fig. 12. Capacitance

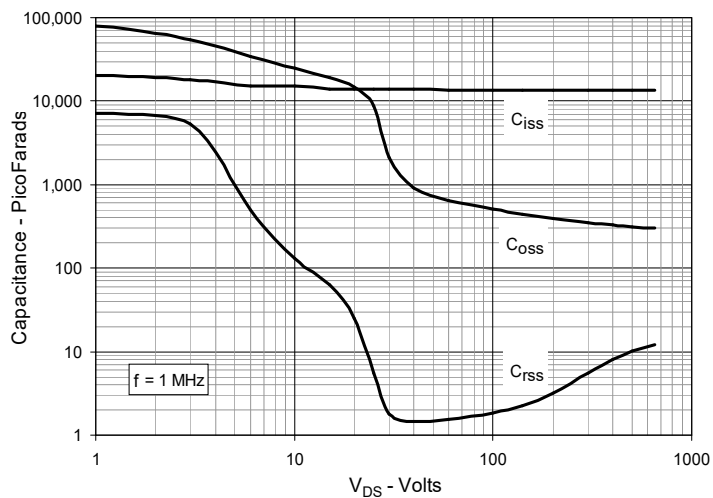


Fig. 13. Output Capacitance Stored Energy

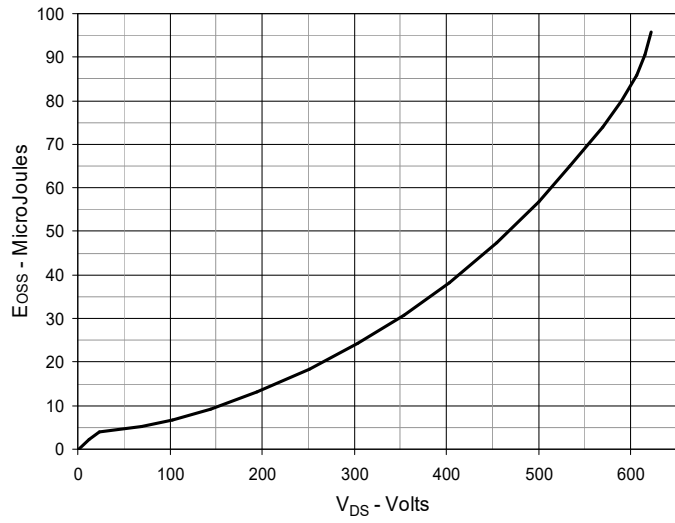


Fig. 14. Forward-Bias Safe Operating Area

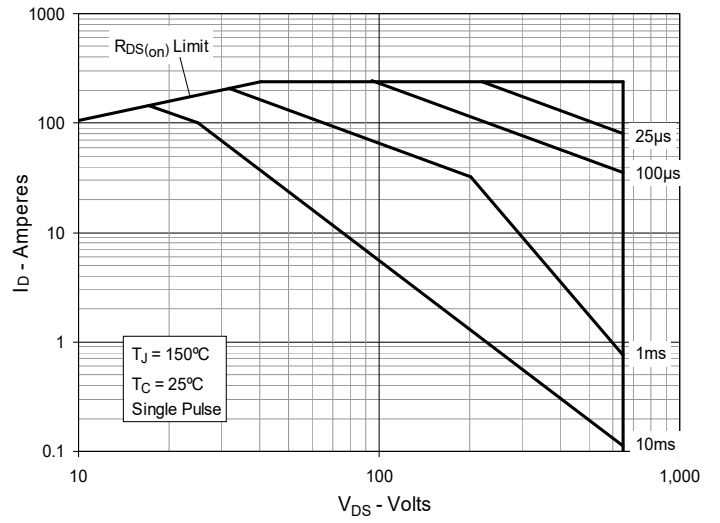
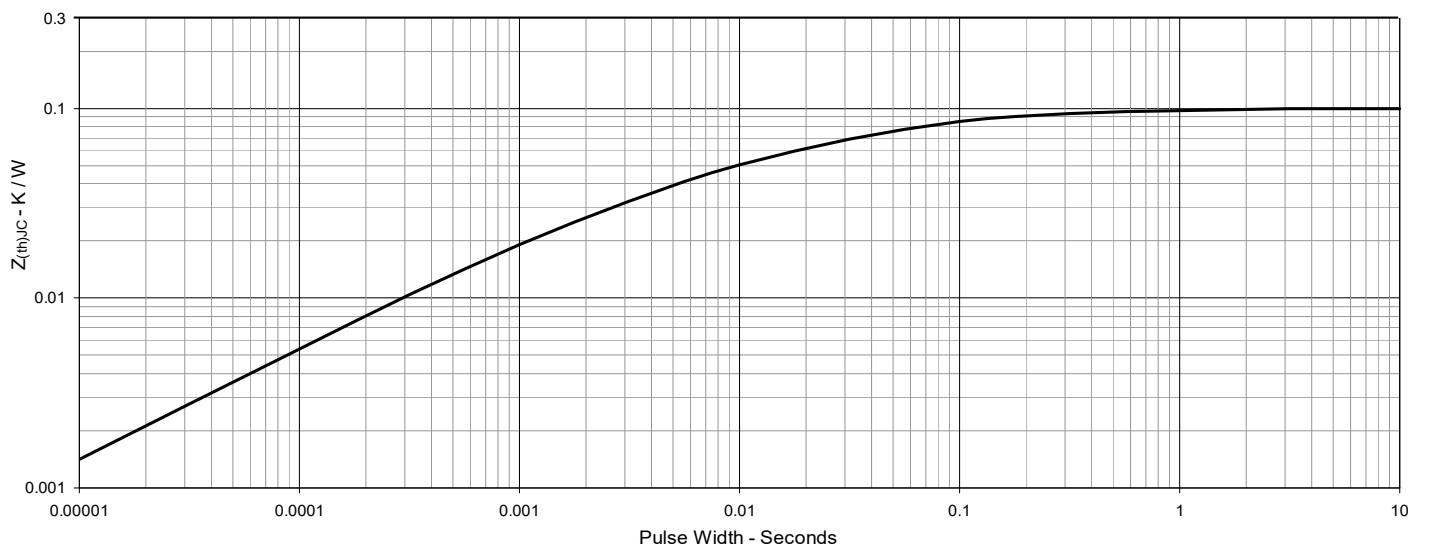
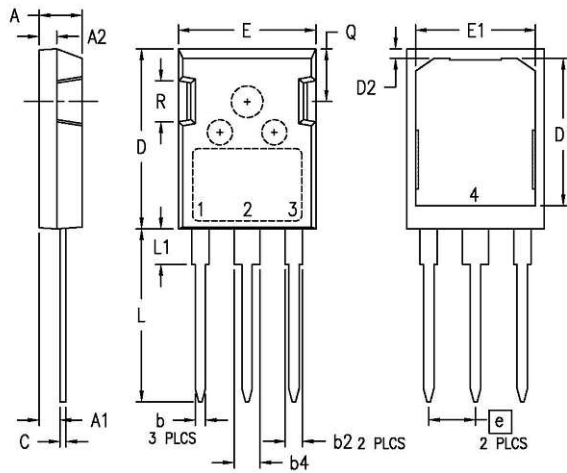


Fig. 15. Maximum Transient Thermal Impedance



PLUS247 Outline

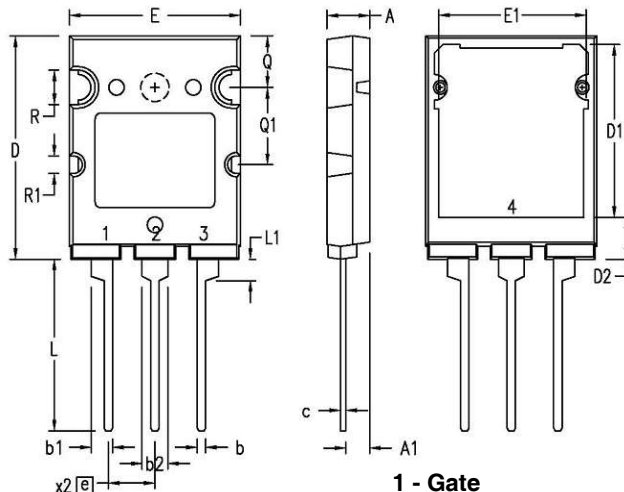


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b2	.075	.087	1.91	2.20
b4	.115	.126	2.92	3.20
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
D1	.650	.690	16.51	17.53
D2	.035	.050	0.89	1.27
E	.620	.635	15.75	16.13
E1	.520	.560	13.08	14.22
e	.215 BSC		5.45 BSC	
L	.780	.810	19.81	20.57
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83

- 1 - Gate
- 2,4 - Drain
- 3 - Source

NOTE: 1. This drawing will meet all dimensions requirement of JEDEC outline TO-247 AD (R-PSIP-F3) except screw mounting hole.
 2. Pin #2 is connected to the bottom heatsink (#4).
 3. Lead finish - One of the following depending on the packaging plants.
 3.1 Matte pure tin plating on the leads and back heatsink.
 3.2 Pb free solder dip on the leads and pre Ni plated back heatsink.

TO-264 Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.209	4.70	5.30
A1	.102	.118	2.60	3.00
b	.035	.049	0.90	1.25
b1	.091	.106	2.30	2.70
b2	.110	.126	2.80	3.20
c	.020	.033	0.50	0.85
D	1.012	1.035	25.70	26.30
D1	.783	.799	19.90	20.30
D2	.185	.205	4.70	5.20
E	.776	.799	19.70	20.30
E1	.661	.677	16.80	17.20
e	.215 BSC		5.46 BSC	
L	.768	.807	19.50	20.50
L1	.091	.106	2.30	2.70
Q	.228	.244	5.80	6.20
Q1	.346	.362	8.80	9.20
øR	.150	.165	3.80	4.20
øR1	.071	.087	1.80	2.20

- 1 - Gate
- 2,4 - Drain
- 3 - Source

NOTE: Leads and back heatsink are Matte Pure Tin plated.



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[DMN1006UCA6-7](#) [DMN16M9UCA6-7](#)