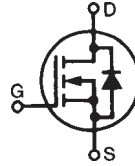


**Linear L2™
Power MOSFETs
w/ Extended FBSOA**

**IXTA15N50L2
IXTP15N50L2
IXTH15N50L2**

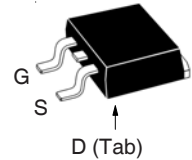
**$V_{DSS} = 500V$
 $I_{D25} = 15A$
 $R_{DS(on)} \leq 480m\Omega$**

N-Channel Enhancement Mode
Avalanche Rated

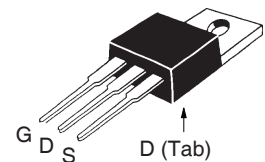


Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $150^\circ C$	500	V
V_{DGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GS} = 1M\Omega$	500	V
V_{GSS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ C$	15	A
I_{DM}	$T_C = 25^\circ C$, Pulse Width Limited by T_{JM}	35	A
I_A	$T_C = 25^\circ C$	15	A
E_{AS}	$T_C = 25^\circ C$	750	mJ
P_D	$T_C = 25^\circ C$	300	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	1.6mm (0.062 in.) from Case for 10s	300	$^\circ C$
T_{SOLD}	Plastic Body for 10s	260	$^\circ C$
M_d	Mounting Torque (TO-220 & TO-247)	1.13/10	Nm/lb.in.
Weight	TO-263	2.5	g
	TO-220	3.0	g
	TO-247	6.0	g

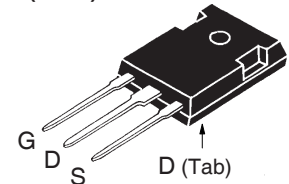
TO-263 AA (IXTA)



TO-220AB (IXTP)



TO-247 (IXTH)



G = Gate D = Drain
S = Source Tab = Drain

Features

- Designed for Linear Operation
- International Standard Packages
- Avalanche Rated
- Molding Epoxies Meet UL 94 V-0 Flammability Classification
- Guaranteed FBSOA at 75°C

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- Solid State Circuit Breakers
- Soft Start Controls
- Linear Amplifiers
- Programmable Loads
- Current Regulators

Symbol	Test Conditions ($T_J = 25^\circ C$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 250\mu A$	500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	2.5		4.5 V
I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$			± 100 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ C$			25 μA 200 μA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 0.5 \cdot I_{D25}$, Note 1			480 m Ω

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values			
		Min.	Typ.	Max.	
g_{fs}	$V_{DS} = 10\text{V}, I_D = 0.5 \cdot I_{D25}$, Note 1	4.5	6.3	8.0	S
C_{iss}	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$		4080		pF
C_{oss}			265		pF
C_{rss}			68		pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}, 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$ $R_G = 10\Omega$ (External)		38		ns
t_r			73		ns
$t_{d(off)}$			110		ns
t_f			65		ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$		123		nC
Q_{gs}			20		nC
Q_{gd}			72		nC
R_{thJC}				0.42	$^\circ\text{C/W}$
R_{thCS}	(TO-220)		0.50		$^\circ\text{C/W}$
	(TO-247)		0.25		$^\circ\text{C/W}$

Safe Operating Area Specification

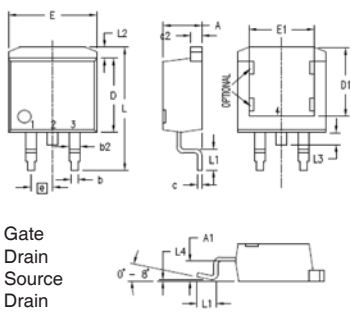
Symbol	Test Conditions	Characteristic Values			
		Min.	Typ.	Max.	
SOA	$V_{DS} = 400\text{V}, I_D = 375\text{mA}, T_C = 75^\circ\text{C}, t_p = 2\text{s}$	150			W

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values			
		Min.	Typ.	Max.	
I_S	$V_{GS} = 0\text{V}$			15	A
I_{SM}	Repetitive, pulse width limited by T_{JM}			60	A
V_{SD}	$I_F = 15\text{A}, V_{GS} = 0\text{V}$, Note 1			1.5	V
t_{rr}	$I_F = 15\text{A}, -di/dt = 100\text{A}/\mu\text{s}, V_R = 100\text{V}, V_{GS} = 0\text{V}$		570		ns

Note 1: Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

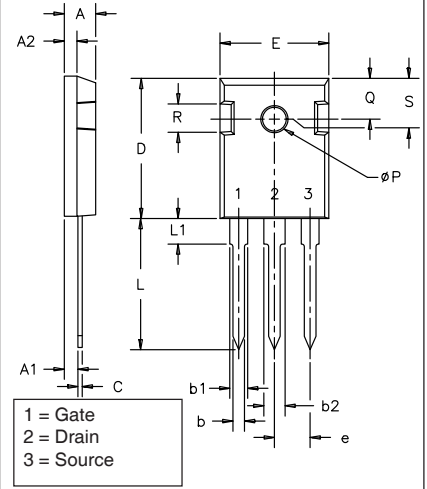
TO-263 Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.160	.190	4.06	4.83
A1	.080	.110	2.03	2.79
b	.020	.039	0.51	0.99
b2	.045	.055	1.14	1.40
c	.016	.029	0.40	0.74
c2	.045	.055	1.14	1.40
D	.340	.380	8.64	9.65
D1	.315	.350	8.00	8.89
E	.380	.410	9.65	10.41
E1	.245	.320	6.22	8.13
e	.100 BSC		2.54 BSC	
L	.575	.625	14.61	15.88
L1	.090	.110	2.29	2.79
L2	.040	.055	1.02	1.40
L3	.050	.070	1.27	1.78
L4	0	.005	0	0.13

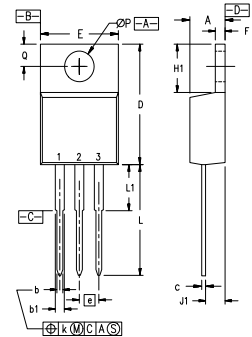
1 = Gate
2 = Drain
3 = Source
4 = Drain

TO-247 Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.209	4.7	5.3
A1	.087	.102	2.2	2.54
A2	.059	.098	2.2	2.6
b	.040	.055	1.0	1.4
b1	.065	.084	1.65	2.13
b2	.113	.123	2.87	3.12
C	.016	.031	.4	.8
D	.819	.845	20.80	21.46
E	.610	.640	15.75	16.26
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1		.177		4.50
ϕP	.140	.144	3.55	3.65
Q	.212	.244	5.4	6.2
R	.170	.216	4.32	5.49
S	.242 BSC		6.15 BSC	

TO-220 Outline



Pins: 1 - Gate 2 - Drain
3 - Source

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.170	.190	4.32	4.83
b	.025	.040	0.64	1.02
b1	.045	.065	1.15	1.65
c	.014	.022	0.35	0.56
D	.580	.630	14.73	16.00
E	.390	.420	9.91	10.66
e	.100 BSC		2.54 BSC	
F	.045	.055	1.14	1.40
H1	.230	.270	5.85	6.85
J1	.090	.110	2.29	2.79
k	0	.015	0	0.38
L	.500	.550	12.70	13.97
L1	.110	.230	2.79	5.84
ϕP	.139	.161	3.53	4.08
Q	.100	.125	2.54	3.18

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

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4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

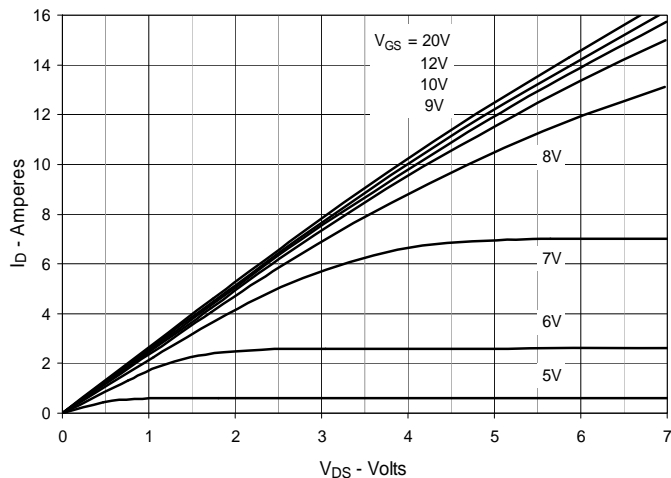


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

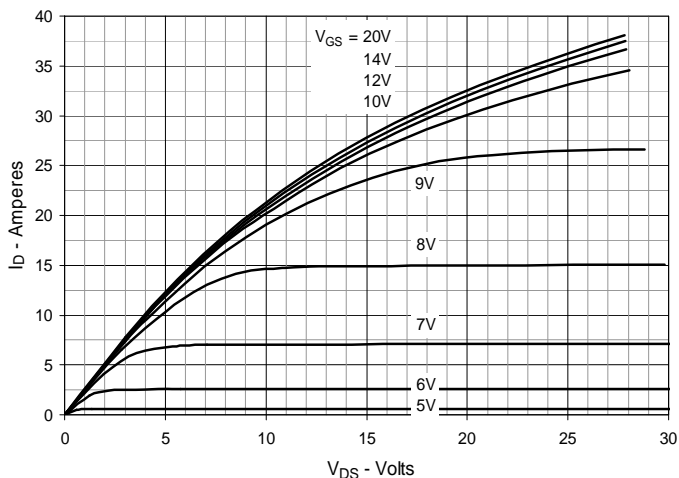


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

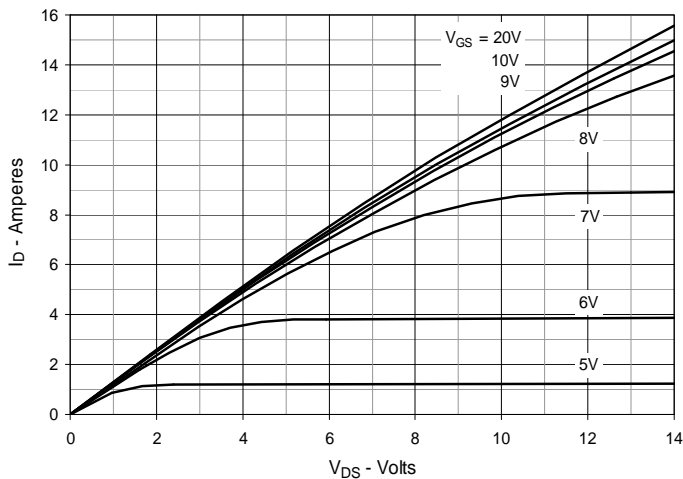


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 7.5\text{A}$ Value vs. Junction Temperature

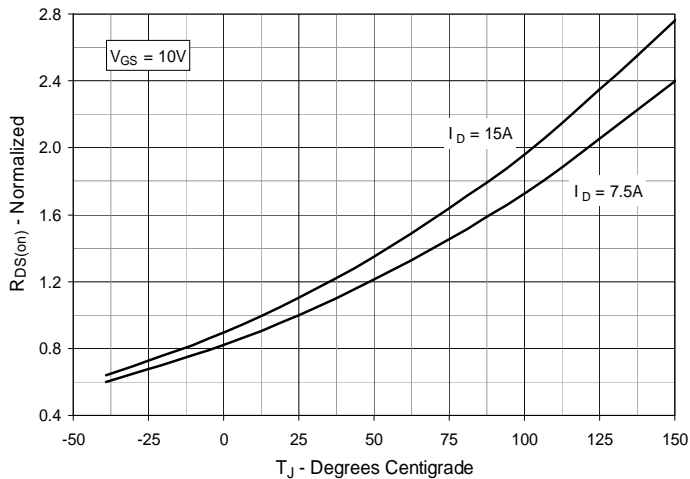


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 7.5\text{A}$ Value vs. Drain Current

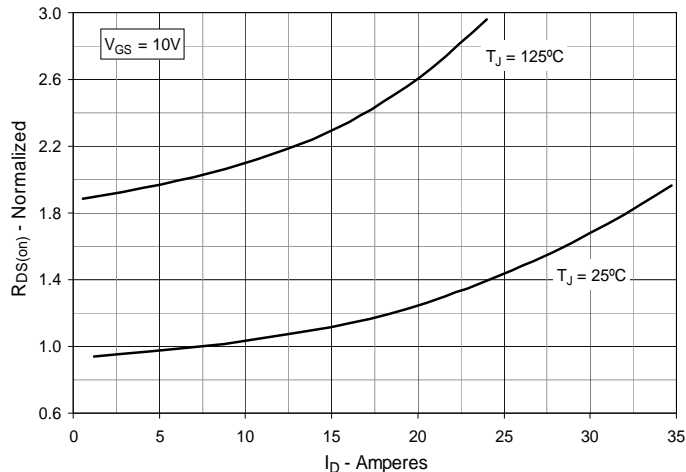


Fig. 6. Maximum Drain Current vs. Case Temperature

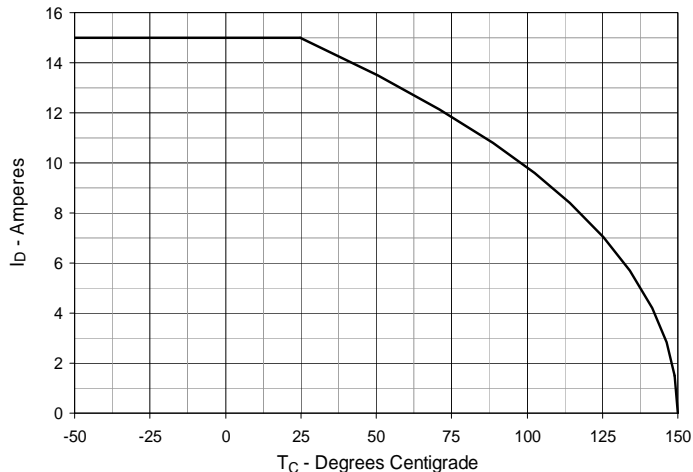


Fig. 7. Input Admittance

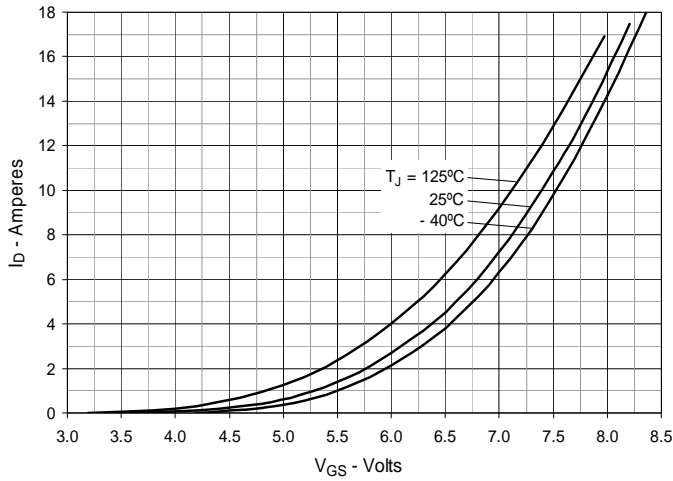


Fig. 8. Transconductance

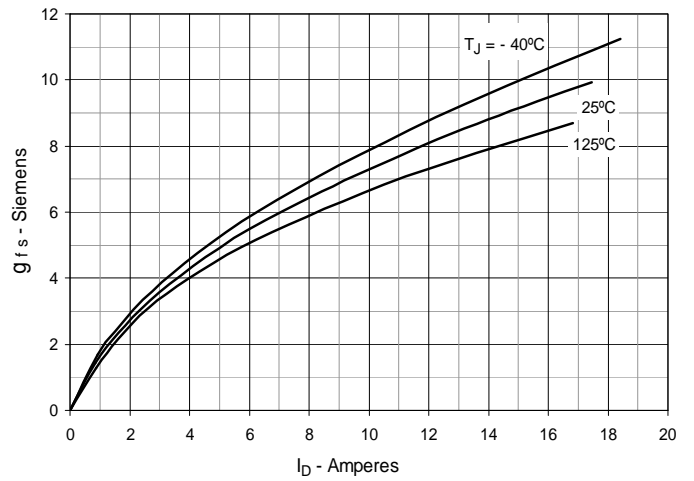


Fig. 9. Forward Voltage Drop of Intrinsic Diode

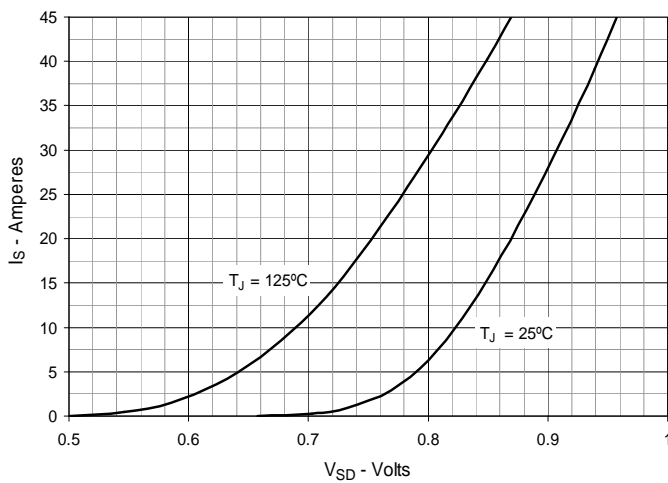


Fig. 10. Gate Charge

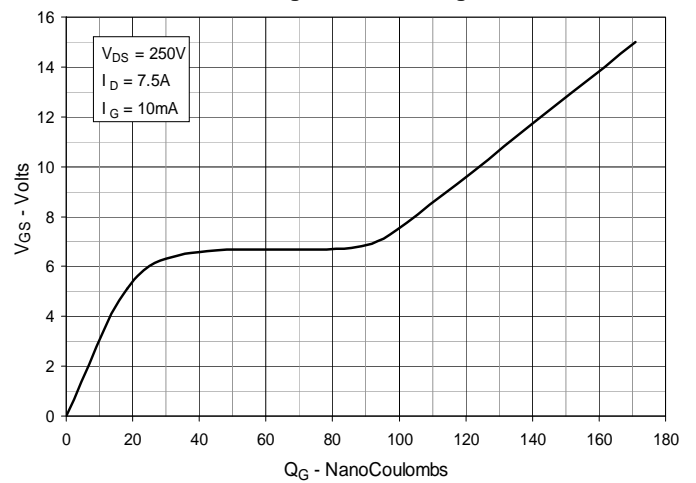


Fig. 11. Capacitance

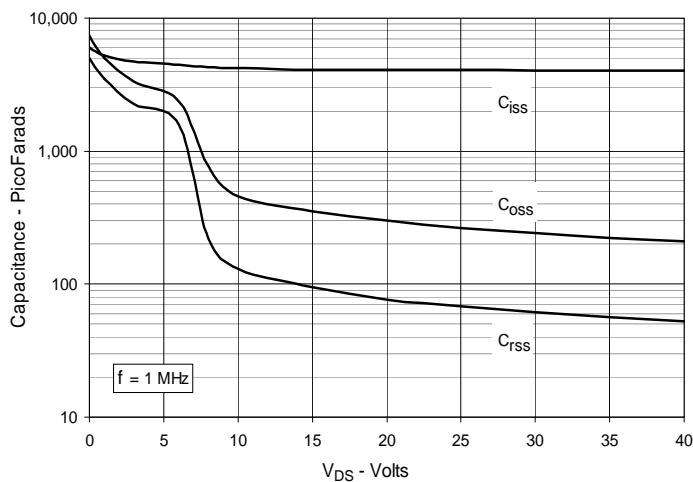


Fig. 12. Maximum Transient Thermal Impedance

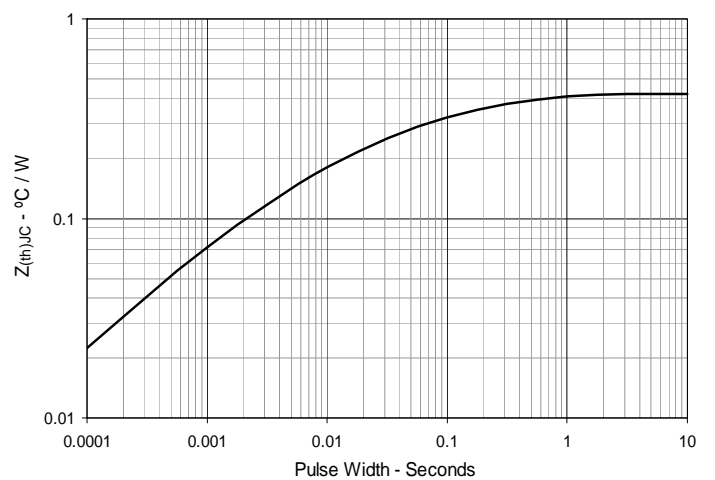


Fig. 13. Forward-Bias Safe Operating Area
@ $T_C = 25^\circ\text{C}$

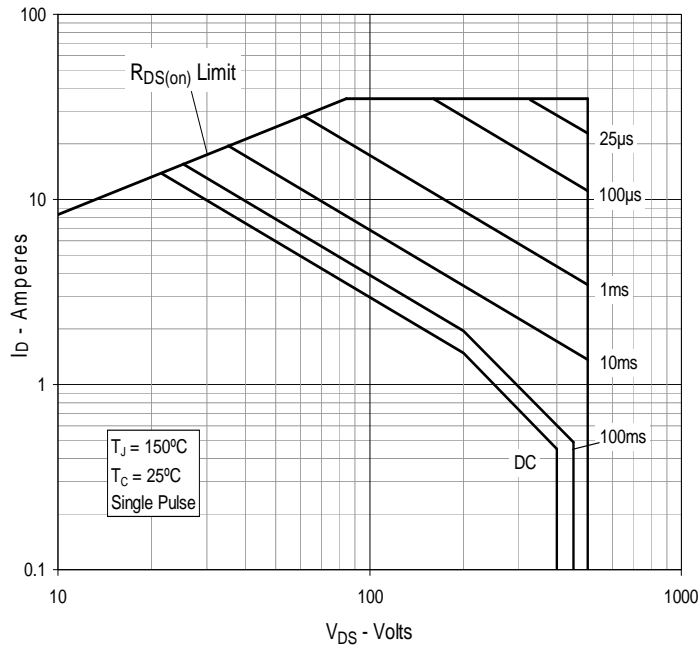
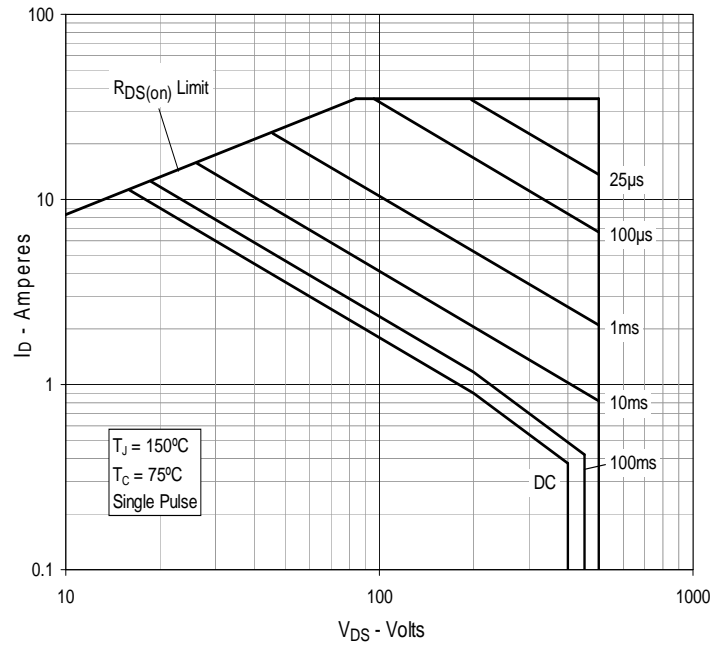


Fig. 14. Forward-Bias Safe Operating Area
@ $T_C = 75^\circ\text{C}$



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