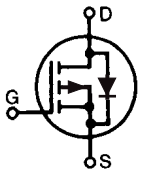
IXYS

Standard Power MOSFET

IXTH 24P20
IXTT 24P20

V_{DSS} = - 200 V
I_{D25} = - 24 A
$R_{DS(on)}$ ≤ 0.15 Ω

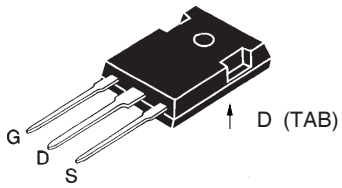
P-Channel Enhancement Mode
Avalanche Rated



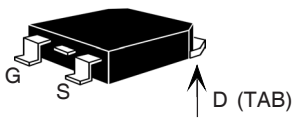
Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	-200	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	-200	V
V_{GS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	-24	A
I_{DM}	T_C = 25°C, pulse width limited by T_J	-96	A
I_{AR}	T_C = 25°C	-24	A
E_{AR}	T_C = 25°C	30	mJ
P_D	T_C = 25°C	300	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
	Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s	400	°C
	Plastic Body for 10s	250	°C
M_d	Mounting torque (TO-247)	1.13/10	Nm/lb.in.
Weight	TO-247	6	g
	TO-268	5	g

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = -250 μA		-200			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = -250 μA		-3.0		-5.0	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0				±100	nA
I_{DSS}	V_{DS} = 0.8 • V_{DSS} V_{GS} = 0 V	T_J = 25°C T_J = 125°C			-25 -1	μA mA
$R_{DS(on)}$	V_{GS} = -10 V, I_D = 0.5 • I_{D25}				0.15	Ω

TO-247 (IXTH)



TO-268 (IXTT)



G = Gate, D = Drain,
S = Source, TAB = Drain

Features

- International standard packages
- Low $R_{DS\ (on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance (<5 nH) - easy to drive and to protect

Applications

- High side switching
- Push-pull amplifiers
- DC choppers
- Automatic test equipment

Advantages

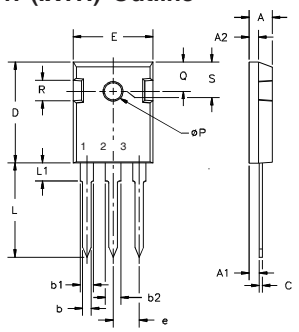
- Easy to mount with 1 screw (isolated mounting screw hole)
- Space savings
- High power density

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values min.	typ.	max.	
g_{fs}	V_{DS} = -10 V; I_D = I_{D25}, pulse test	10	15		S
C_{iss}	V_{GS} = 0 V, V_{DS} = -25 V, f = 1 MHz		4200		pF
C_{oss}			830		pF
C_{rss}			350		pF
$t_{d(on)}$	V_{GS} = -10 V, V_{DS} = 0.5 V_{DSS}, I_D = 0.5 I_{D25} R_G = 4.7 Ω (External)		36		ns
t_r			29		ns
$t_{d(off)}$			68		ns
t_f			28		ns
$Q_{g(on)}$	V_{GS} = -10 V, V_{DS} = 0.5 V_{DSS}, I_D = 0.5 I_{D25}		150		nC
Q_{gs}			40		nC
Q_{gd}			70		nC
R_{thJC}				0.42	K/W
R_{thCS}	(TO-247)		0.25		K/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values min.	typ.	max.	
I_S	V_{GS} = 0			-24	A
I_{SM}	Repetitive; pulse width limited by T_{JM}			-96	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %			-3	V
t_{rr}	I_F = I_S, di/dt = 100 A/µs, V_R = -50 V		250		ns

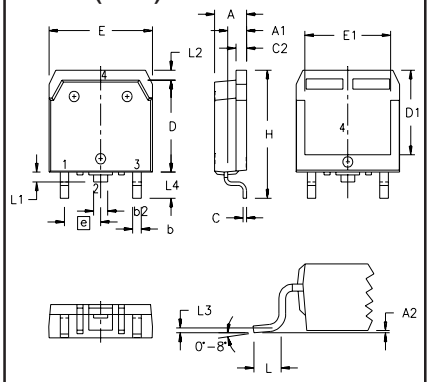
TO-247 (IXTH) Outline



Terminals: 1 - Gate 2 - Drain
3 - Source Tab - Drain

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.7	5.3	.185	.209
A_1	2.2	2.54	.087	.102
A_2	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b_1	1.65	2.13	.065	.084
b_2	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
ØP	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15	BSC	242	BSC

TO-268 (IXTT) Outline



SYM	INCHES MIN	MAX	MILLIMETERS MIN	MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.001	.010	0.02	0.25
b	.045	.057	1.15	1.45
b2	.075	.083	1.90	2.10
C	.016	.026	0.40	0.65
C2	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D1	.488	.500	12.40	12.70
E	.624	.632	15.85	16.05
E1	.524	.535	13.30	13.60
e	.215 BSC		5.45 BSC	
H	.736	.752	18.70	19.10
L	.094	.106	2.40	2.70
L1	.047	.055	1.20	1.40
L2	.039	.045	1.00	1.15
L3	.010 BSC		0.25 BSC	
L4	.150	.161	3.80	4.10

Fig. 1. Output Characteristics @ 25ºC

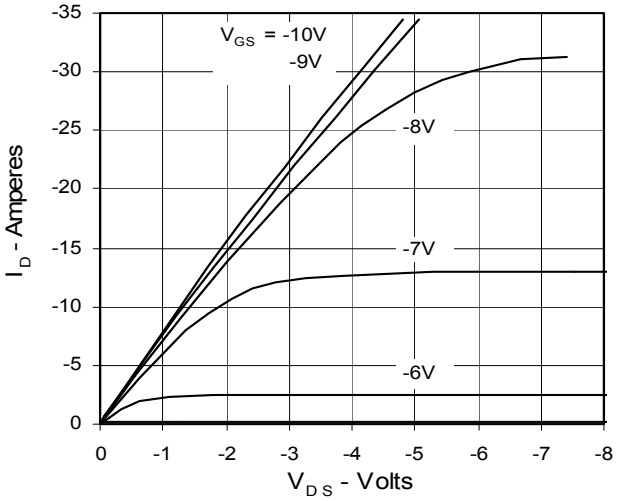


Fig. 2. Output Characteristics @ 125ºC

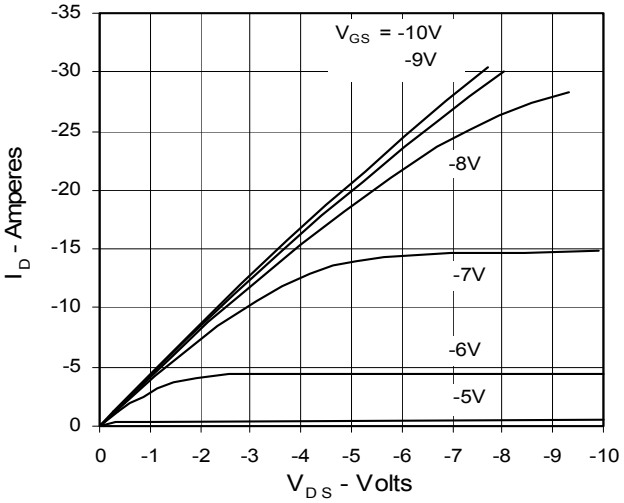


Fig. 3. $R_{DS(on)}$ Normalized to I_{D25} Value vs. Junction Temperature

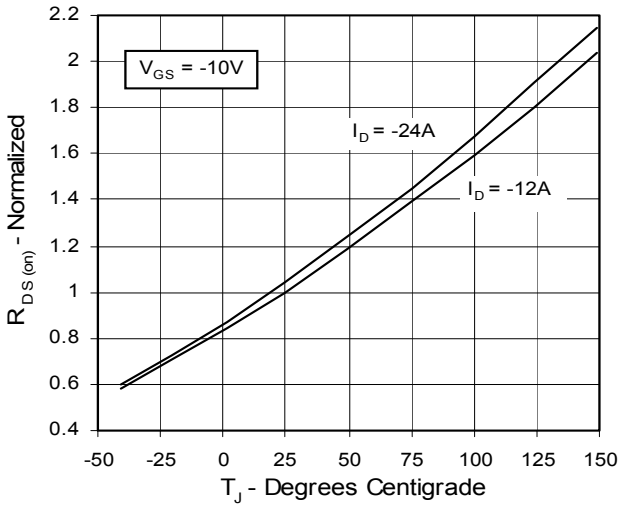


Fig. 4. $R_{DS(on)}$ Normalized to I_{D25} Value vs. I_D

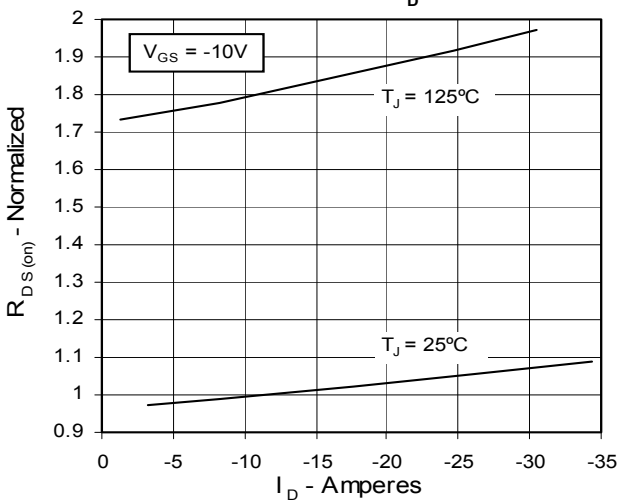


Fig. 5. Drain Current vs. Case Temperature

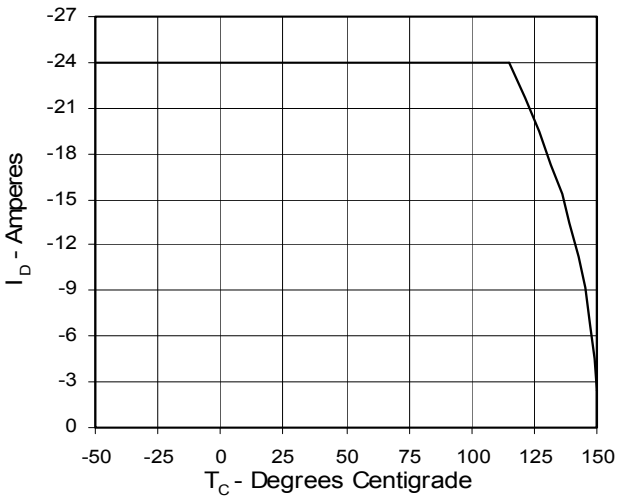


Fig. 6. Input Admittance

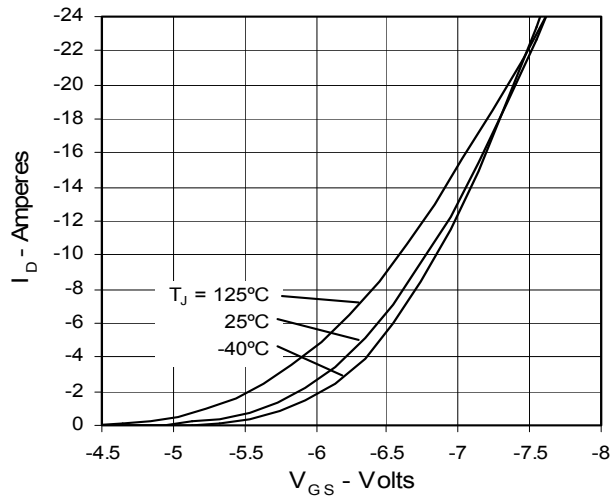


Fig. 7. Transconductance

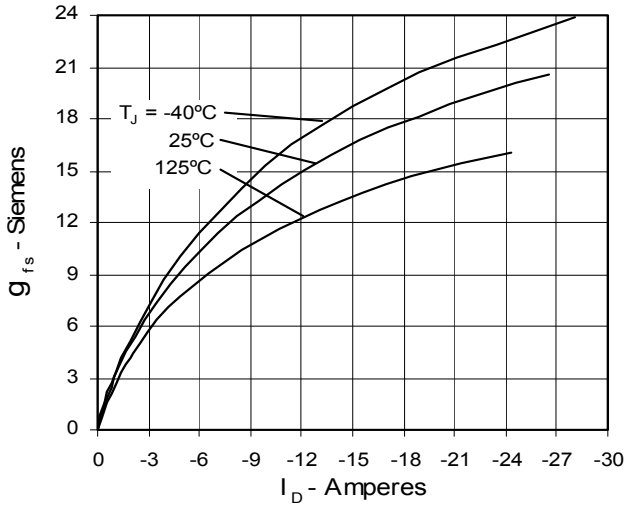


Fig. 8. Source Current vs. Source-To-Drain Voltage

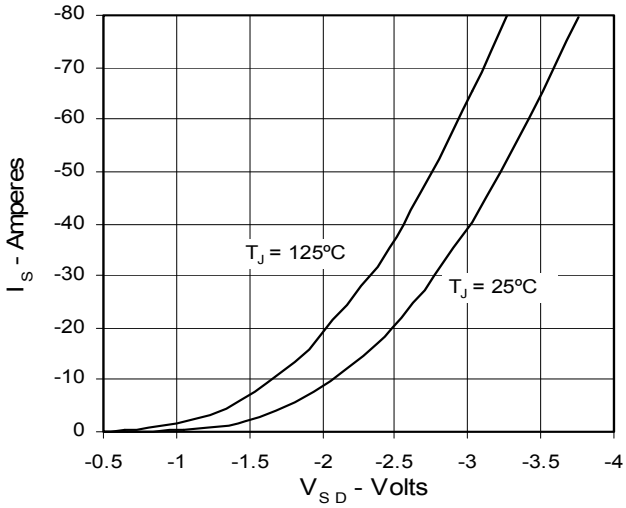


Fig. 9. Gate Charge

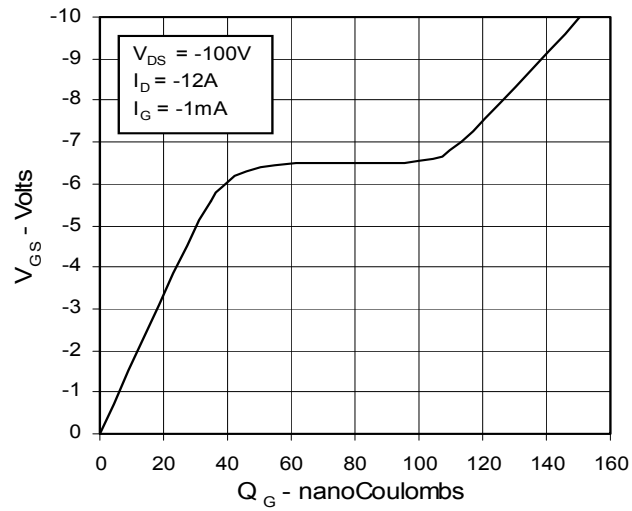


Fig. 10. Temperature dependence of Breakdown and Threshole Voltage

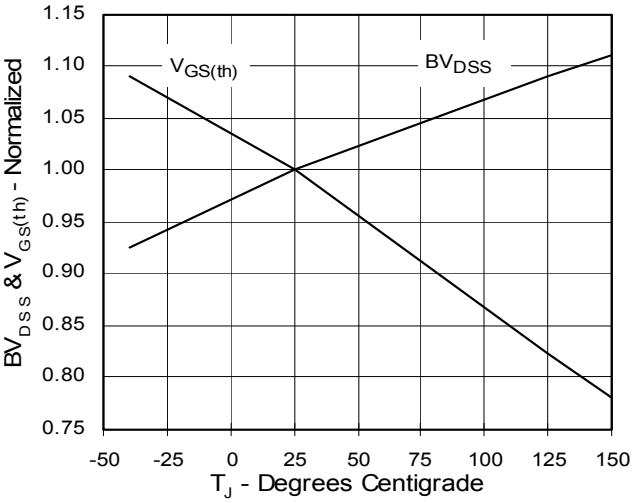


Fig. 11. Capacitance

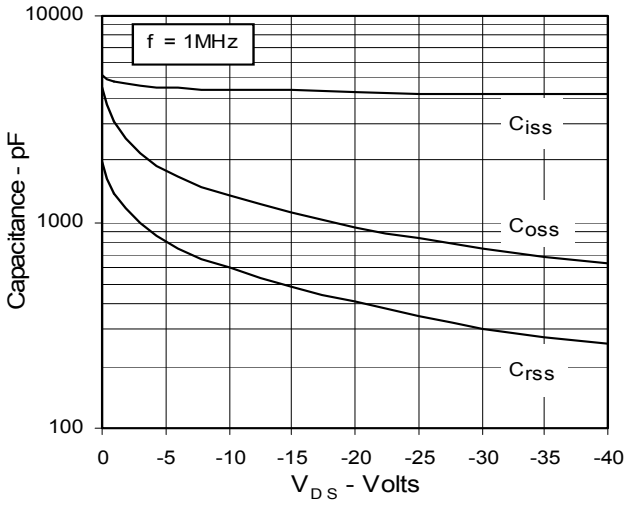


Fig. 12. Forward-Bias Safe Operating Area

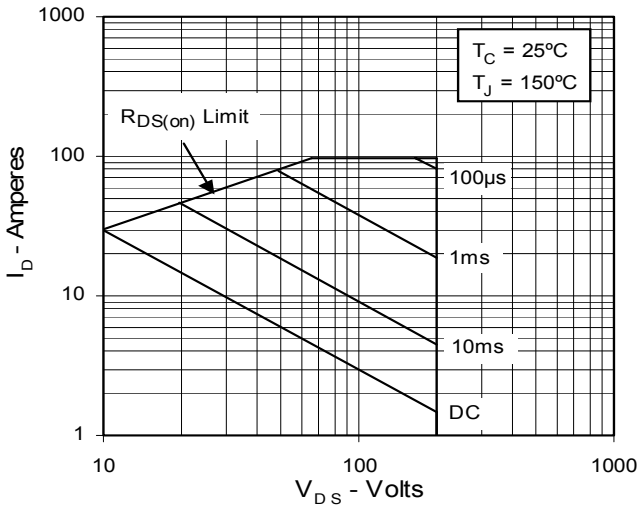
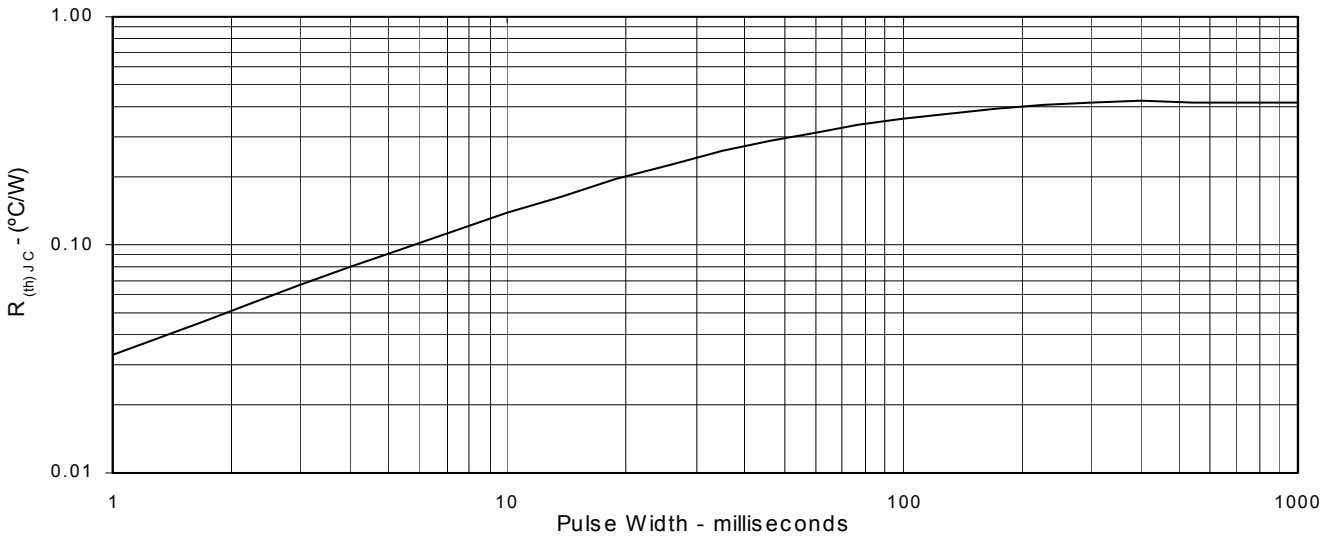


Fig. 13. Maximum Transient Thermal Resistance



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