

# TrenchT4™ Power MOSFET

## IXTP230N04T4M

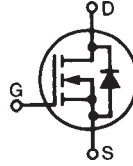
$$V_{DSS} = 40V$$

$$I_{D25} = 230A$$

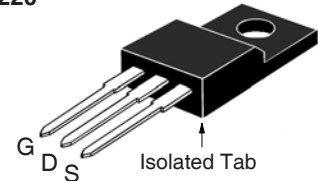
$$R_{DS(on)} \leq 2.9m\Omega$$

(Electrically Isolated Tab)

N-Channel Enhancement Mode  
Avalanche Rated



OVERMOLDED  
TO-220



G = Gate      D = Drain  
S = Source

Symbol	Test Conditions	Maximum Ratings	
$V_{DSS}$	$T_J = 25^\circ\text{C}$ to $175^\circ\text{C}$	40	V
$V_{DGR}$	$T_J = 25^\circ\text{C}$ to $175^\circ\text{C}$ , $R_{GS} = 1M\Omega$	40	V
$V_{GSM}$	Transient	$\pm 15$	V
$I_{D25}$	$T_C = 25^\circ\text{C}$ , Limited by $T_{JM}$	230	A
$I_{LRMS}$	Lead Current Limit, RMS	120	A
$I_{DM}$	$T_C = 25^\circ\text{C}$ , Pulse Width Limited by $T_{JM}$	700	A
$I_A$	$T_C = 25^\circ\text{C}$	100	A
$E_{AS}$	$T_C = 25^\circ\text{C}$	600	mJ
$P_D$	$T_C = 25^\circ\text{C}$	40	W
$T_J$		-55 ... +175	$^\circ\text{C}$
$T_{JM}$		175	$^\circ\text{C}$
$T_{stg}$		-55 ... +175	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering	300	$^\circ\text{C}$
$T_{SOLD}$	1.6 mm (0.062in.) from Case for 10s	260	$^\circ\text{C}$
$V_{ISOL}$	50/60 Hz, 1 Minute	2500	V~
$M_d$	Mounting Torque	1.13 / 10	Nm/lb.in
<b>Weight</b>		2.5	g

### Features

- Plastic Overmolded Tab
- International Standard Package
- $175^\circ\text{C}$  Operating Temperature
- High Current Handling Capability
- Avalanche Rated
- 2500V~ Electrical Isolation
- Low  $R_{DS(on)}$

### Advantages

- Easy to Mount
- Space Savings
- High Power Density

### Applications

- Synchronous Buck Converters
- High Current Switching Power Supplies
- Battery Powered Electric Motors
- Resonant-Mode Power Supplies
- Electronics Ballast Application
- Class D Audio Amplifiers

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$BV_{DSS}$	$V_{GS} = 0V$ , $I_D = 250\mu\text{A}$	40		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$	2.0		4.0 V
$I_{GSS}$	$V_{GS} = \pm 15V$ , $V_{DS} = 0V$			$\pm 200$ nA
$I_{DSS}$	$V_{DS} = V_{DSS}$ , $V_{GS} = 0V$ $T_J = 150^\circ\text{C}$			5 $\mu\text{A}$ 250 $\mu\text{A}$
$R_{DS(on)}$	$V_{GS} = 10V$ , $I_D = 0.5 \cdot I_{D25}$ , Notes 1,2			2.9 m $\Omega$

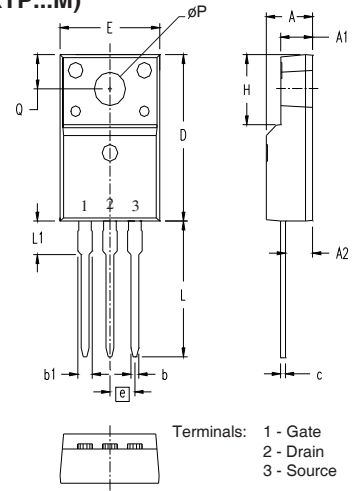
Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$g_{fs}$	$V_{DS} = 10\text{V}, I_D = 60\text{A}$ , Note 1	100	170	S
$R_{Gi}$	Gate Input Resistance		1.2	$\Omega$
$C_{iss}$	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$		7400	pF
$C_{oss}$			1115	pF
$C_{rss}$			760	pF
$t_{d(on)}$	<b>Resistive Switching Times</b> $V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$ $R_G = 10\Omega$ (External)		40	ns
$t_r$			143	ns
$t_{d(off)}$			85	ns
$t_f$			82	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$		140	nC
$Q_{gs}$			35	nC
$Q_{gd}$			53	nC
$R_{thJC}$			0.50	$3.75^\circ\text{C/W}$
$R_{thCS}$				$^\circ\text{C/W}$

### Source-Drain Diode

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$I_S$	$V_{GS} = 0\text{V}$			230 A
$I_{SM}$	Repetitive, Pulse width limited by $T_{JM}$			920 A
$V_{SD}$	$I_F = 100\text{A}, V_{GS} = 0\text{V}$ , Note 1			1.4 V
$t_{rr}$	$I_F = 115\text{A}, V_{GS} = 0\text{V}$ $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 30\text{V}$		32	ns
$I_{RM}$			1.6	A
$Q_{RM}$			25.6	nC

- Notes: 1. Pulse test,  $t \leq 300\mu\text{s}$ , duty cycle,  $d \leq 2\%$ .  
 2. On through-hole packages,  $R_{DS(on)}$  Kelvin test contact location must be 5mm or less from the package body.

### OVERMOLDED TO-220 (IXTP...M)



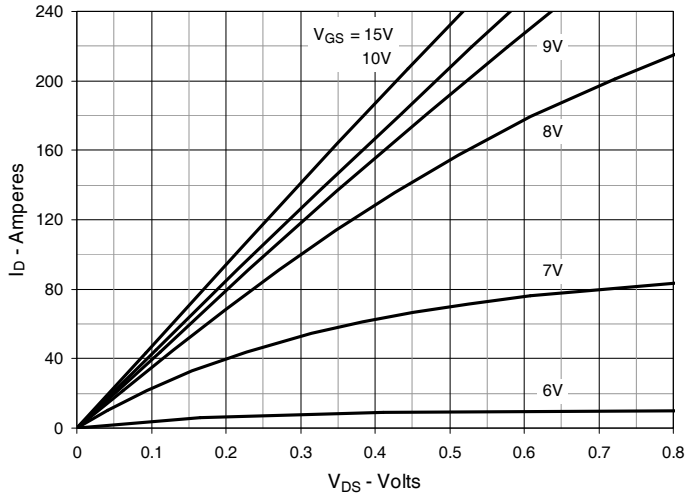
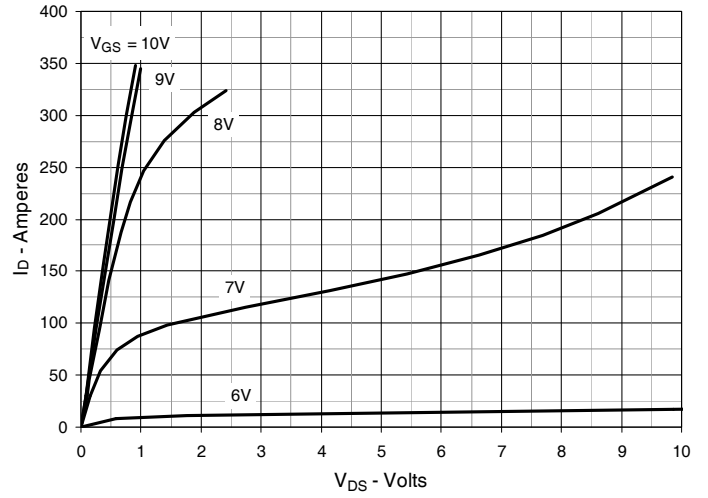
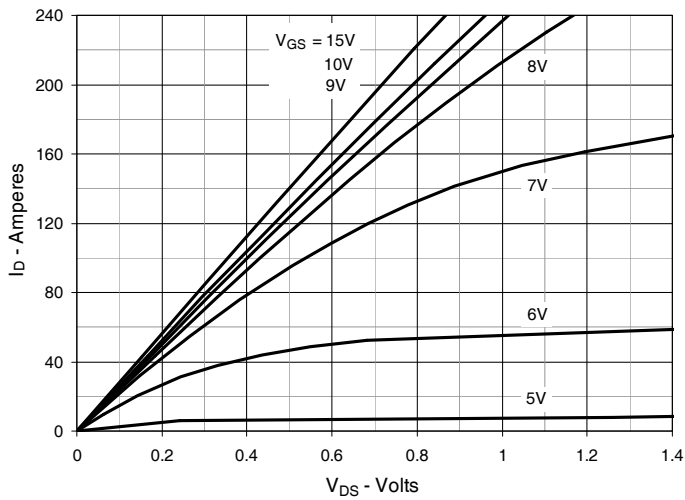
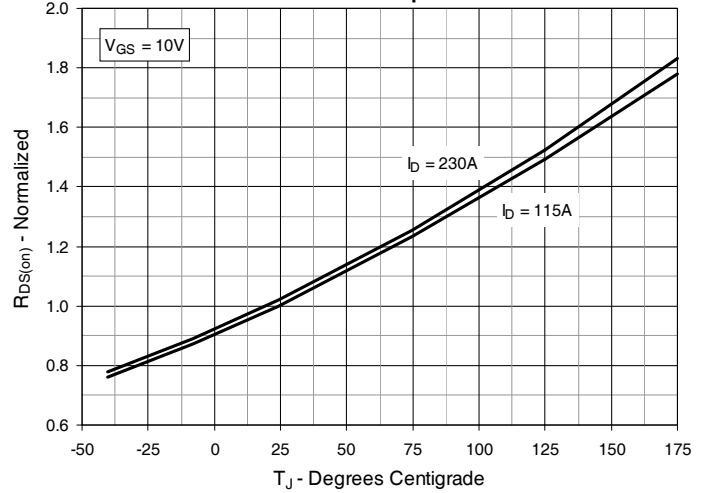
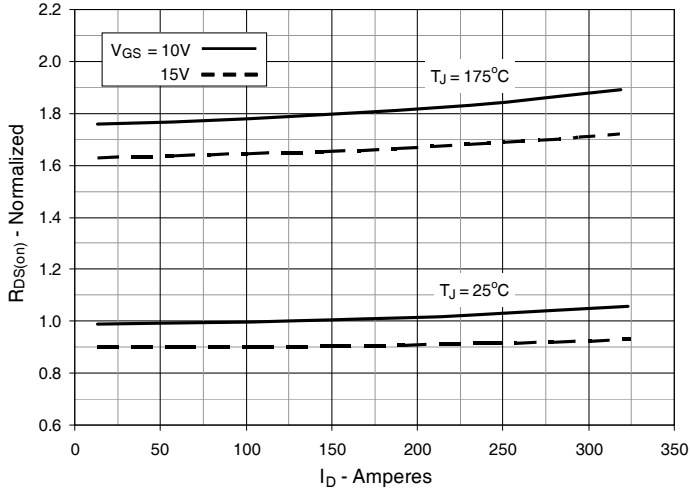
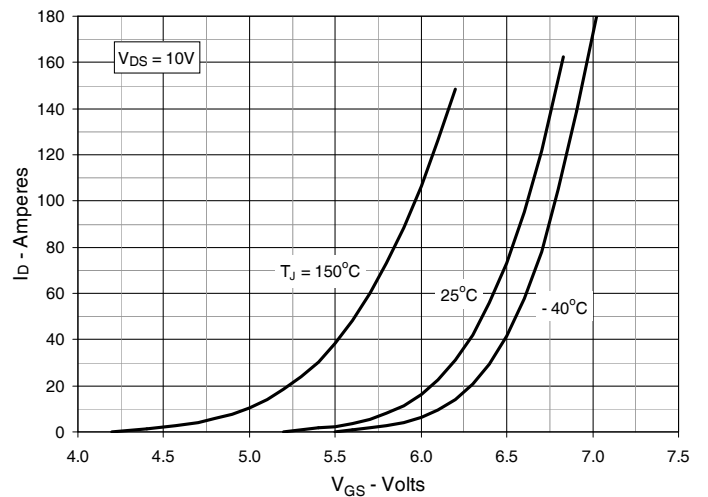
SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.177	.193	4.50	4.90
A1	.092	.108	2.34	2.74
A2	.101	.117	2.56	2.96
b	.028	.035	0.70	0.90
b1	.050	.058	1.27	1.47
c	.018	.024	0.45	0.60
D	.617	.633	15.67	16.07
E	.392	.408	9.96	10.36
e	.100 BSC		2.54 BSC	
H	.255	.271	6.48	6.88
L	.499	.523	12.68	13.28
L1	.119	.135	3.03	3.43
ØP	.121	.129	3.08	3.28
Q	.126	.134	3.20	3.40

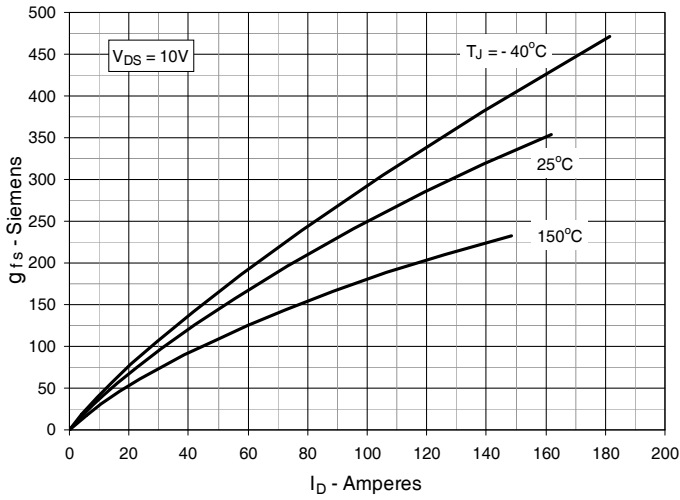
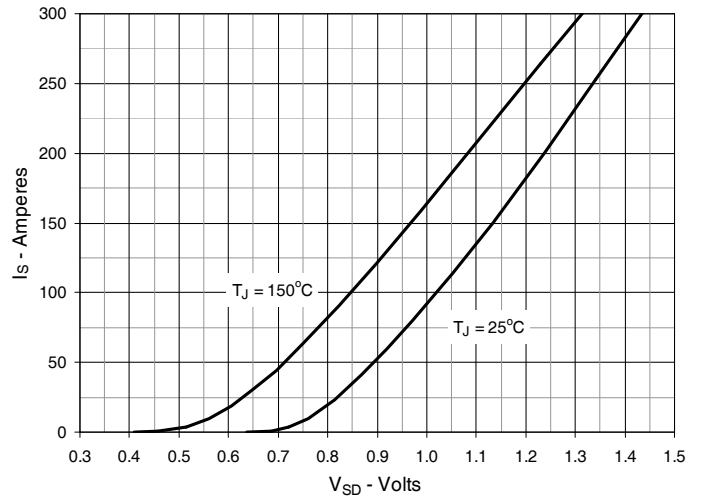
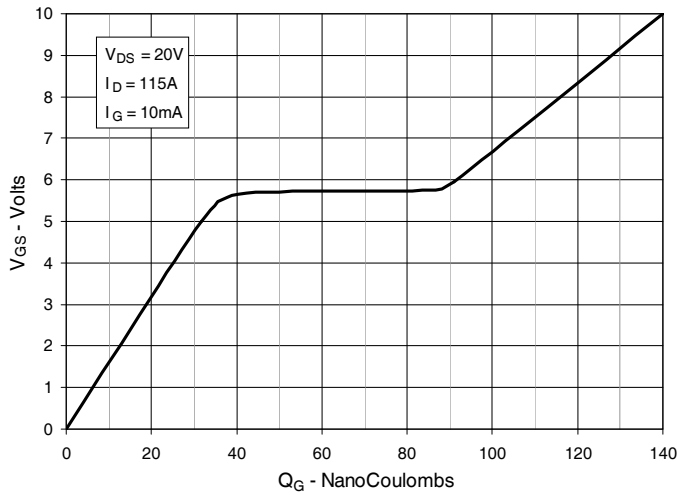
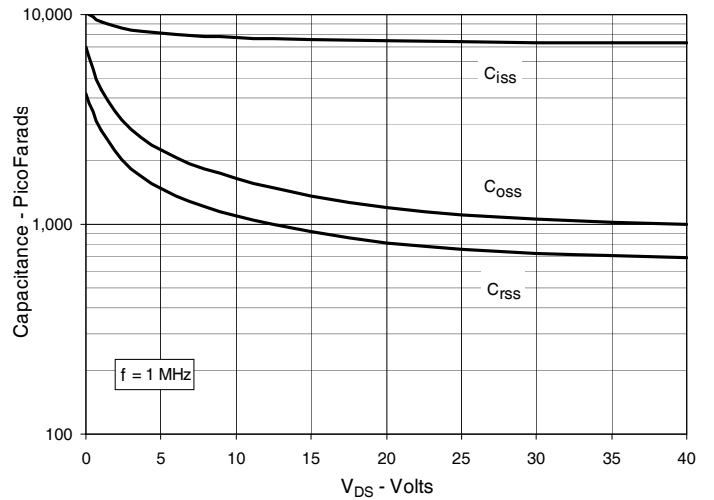
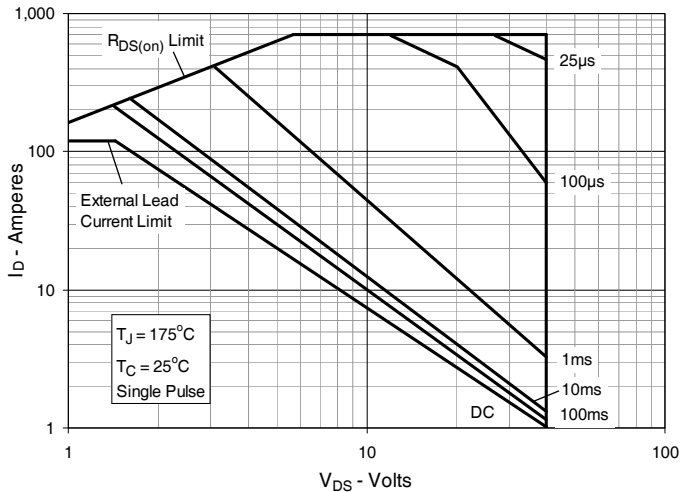
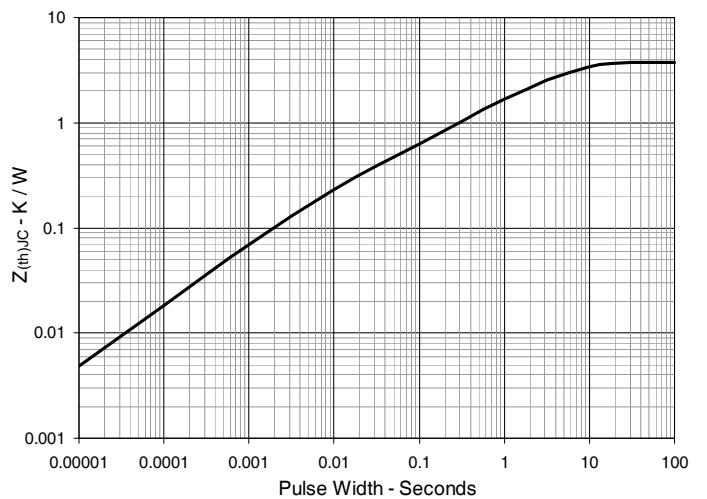
### PRELIMINARY TECHNICAL INFORMATION

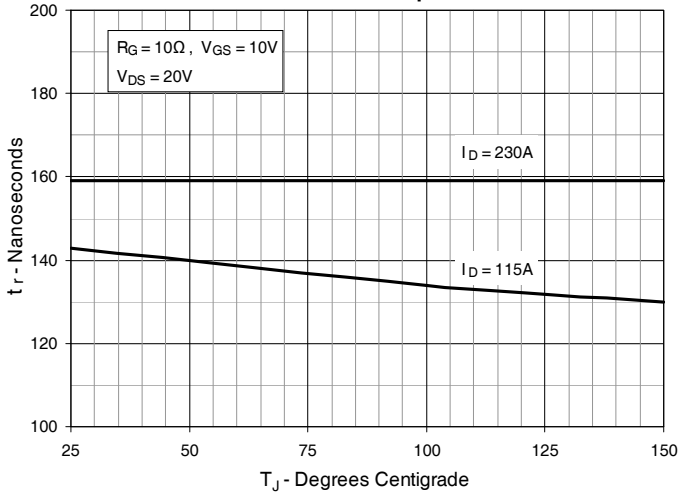
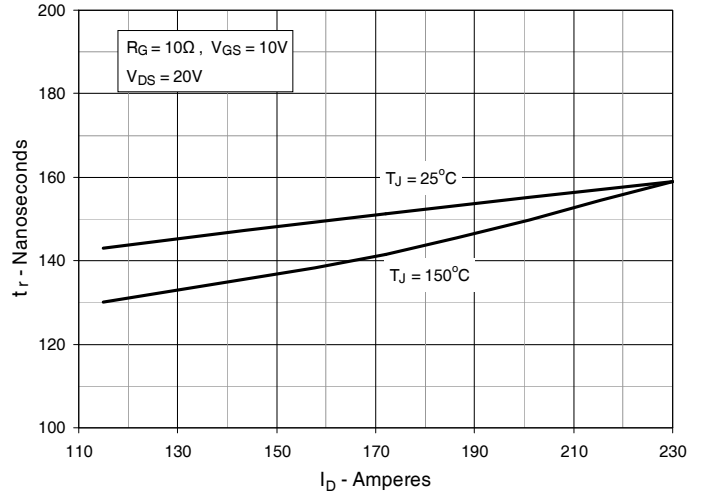
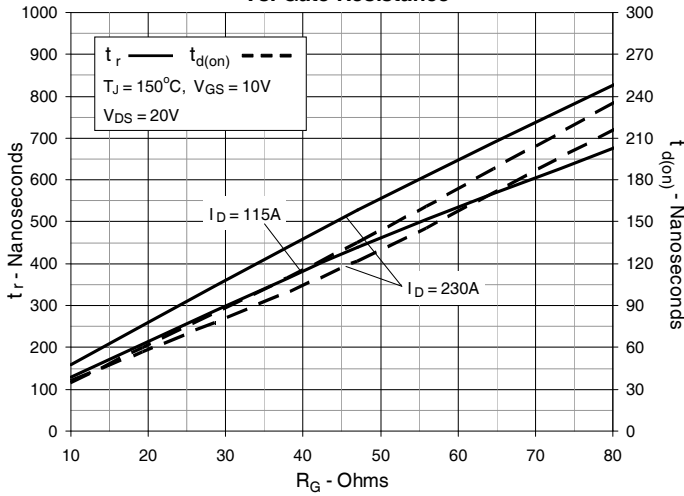
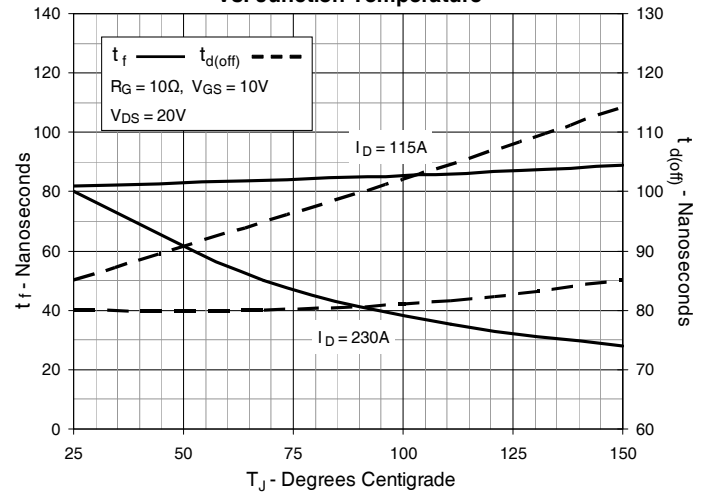
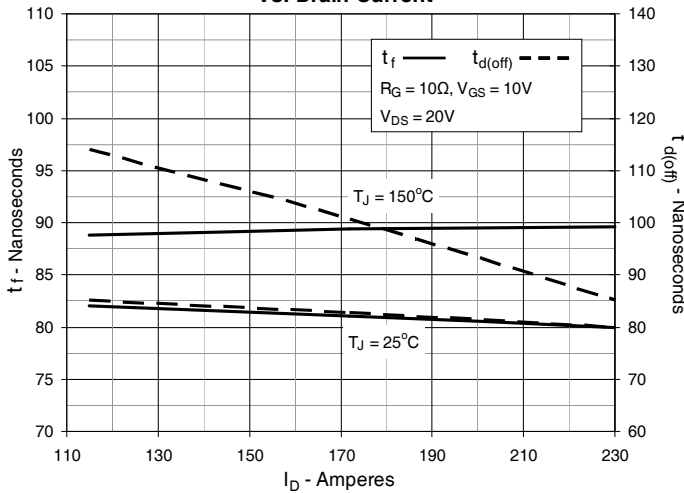
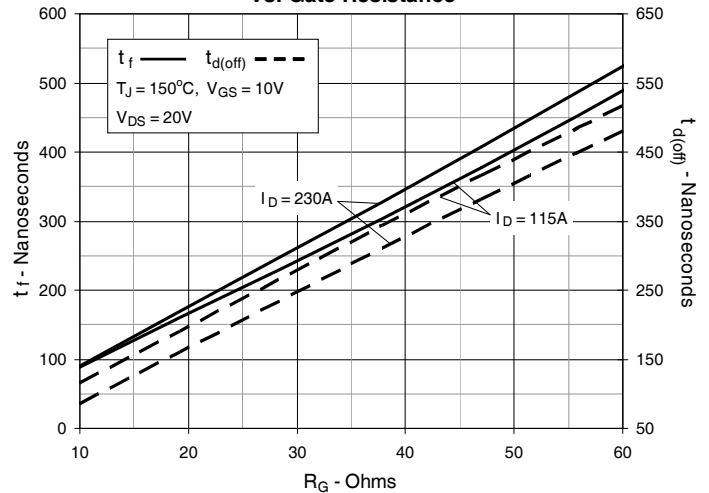
The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves The Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

**Fig. 1. Output Characteristics @  $T_J = 25^\circ\text{C}$** 

**Fig. 2. Extended Output Characteristics @  $T_J = 25^\circ\text{C}$** 

**Fig. 3. Output Characteristics @  $T_J = 150^\circ\text{C}$** 

**Fig. 4. Normalized  $R_{DS(on)}$  to  $I_D = 115\text{A}$  Value vs. Junction Temperature**

**Fig. 5. Normalized  $R_{DS(on)}$  to  $I_D = 115\text{A}$  vs. Drain Current**

**Fig. 6. Input Admittance**


**Fig. 7. Transconductance**

**Fig. 8. Forward Voltage Drop of Intrinsic Diode**

**Fig. 9. Gate Charge**

**Fig. 10. Capacitance**

**Fig. 11. Forward-Bias Safe Operating Area**

**Fig. 12. Maximum Transient Thermal Impedance**


**Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature**

**Fig. 14. Resistive Turn-on Rise Time vs. Drain Current**

**Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance**

**Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature**

**Fig. 17. Resistive Turn-off Switching Times vs. Drain Current**

**Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance**




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