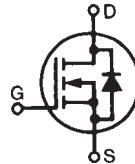


**LinearL2™ Power
MOSFET w/Extended
FBSOA**

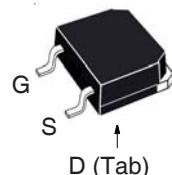
N-Channel Enhancement Mode
Avalanche Rated

IXTT140N075L2HV
IXTH140N075L2

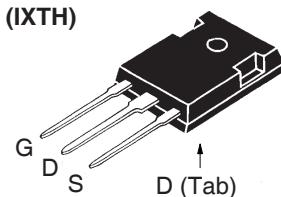
V_{DSS} = **75V**
I_{D25} = **140A**
R_{DS(on)} ≤ **11mΩ**



TO-268HV (IXTT)



TO-247 (IXTH)



G = Gate D = Drain
S = Source Tab = Drain

Symbol	Test Conditions	Maximum Ratings	
V _{DSS}	T _J = 25°C to 150°C	75	V
V _{DGR}	T _J = 25°C to 150°C, R _{GS} = 1MΩ	75	V
V _{GSS}	Continuous	±20	V
V _{GSM}	Transient	±30	V
I _{D25}	T _C = 25°C	140	A
I _{DM}	T _C = 25°C, Pulse Width Limited by T _{JM}	500	A
I _A	T _C = 25°C	140	A
E _{AS}	T _C = 25°C	1.5	J
P _D	T _C = 25°C	540	W
T _J		-55...+150	°C
T _{JM}		150	°C
T _{stg}		-55...+150	°C
T _L	Maximum Lead Temperature for Soldering	300	°C
T _{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	°C
M _d	Mounting Torque (TO-247)	1.13/10	Nm/lb.in
Weight	TO-268HV	4	g
	TO-247	6	g

Symbol	Test Conditions (T _J = 25°C, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV _{DSS}	V _{GS} = 0V, I _D = 250μA	75		V
V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	2.0		V
I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V		±100	nA
I _{DSS}	V _{DS} = V _{DSS} , V _{GS} = 0V T _J = 125°C		5 25	μA μA
R _{DS(on)}	V _{GS} = 10V, I _D = 0.5 • I _{D25} , Note 1		11	mΩ

Features

- Designed for Linear Operation
- International Standard Packages
- Avalanche Rated
- Guaranteed FBSOA at 75°C

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- Solid State Circuit Breakers
- Soft Start Controls
- Linear Amplifiers
- Programmable Loads
- Current Regulators



IXTT140N075L2HV

IXTH140N075L2

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 10\text{V}$, $I_D = 60\text{A}$, Note 1	50	65	80 S
R_{GI}	Gate Input Resistance		1.24	Ω
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$	9300		pF
C_{oss}		2190		pF
C_{rss}		750		pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$ $R_G = 2\Omega$ (External)	26		ns
t_r		83		ns
$t_{d(off)}$		100		ns
t_f		33		ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$	275		nC
Q_{gs}		40		nC
Q_{gd}		108		nC
R_{thJC}			0.23	$^\circ\text{C}/\text{W}$
R_{thCS}	TO-247	0.21		$^\circ\text{C}/\text{W}$

Safe Operating Area Specification

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
SOA	$V_{DS} = 75\text{V}$, $I_D = 4.35\text{A}$, $T_C = 75^\circ\text{C}$, $T_p = 5\text{s}$	326		W

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_s	$V_{GS} = 0\text{V}$		140	A
I_{SM}	Repetitive, pulse width limited by T_{JM}		560	A
V_{SD}	$I_F = 100\text{A}$, $V_{GS} = 0\text{V}$, Note 1		1.4	V
t_{rr}	$I_F = 70\text{A}$, $-di/dt = 100\text{A}/\mu\text{s}$, $V_R = 37.5\text{V}$, $V_{GS} = 0\text{V}$	200		ns
I_{RM}		14.0		A
Q_{RM}		1.4		μC

Note: 1. Pulse test, $t \leq 300\mu\text{s}$; duty cycle, $d \leq 2\%$.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338B2 4,860,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2 4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

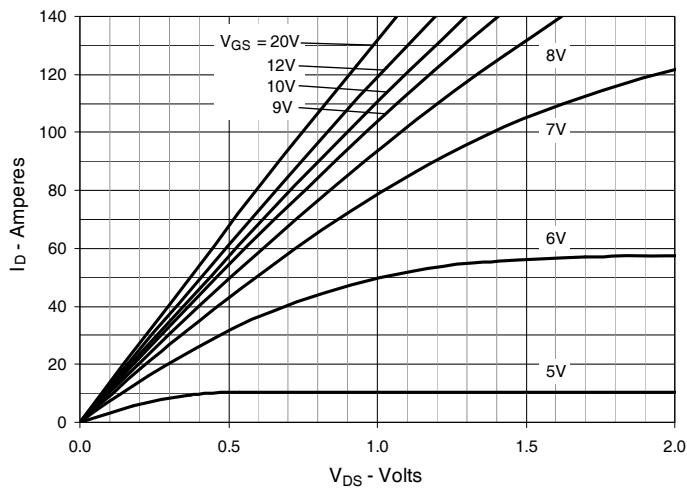
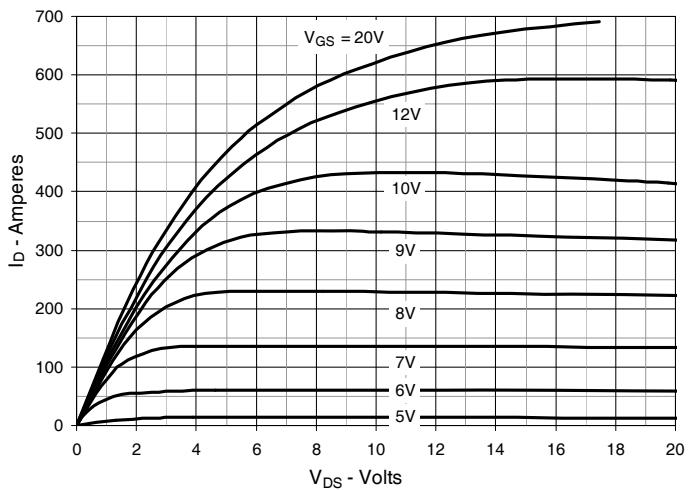
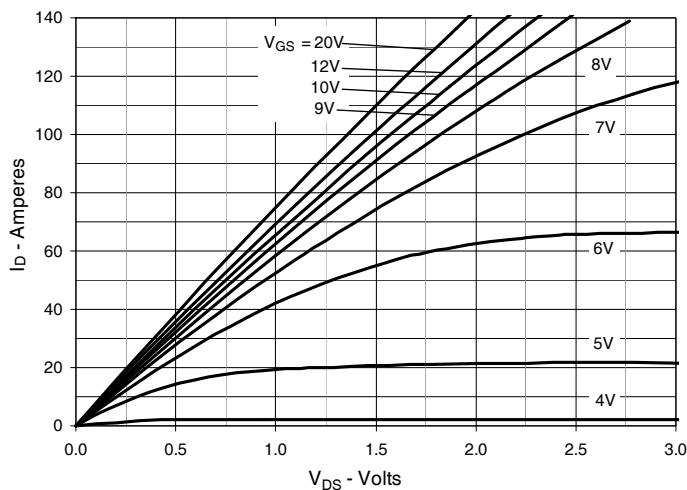
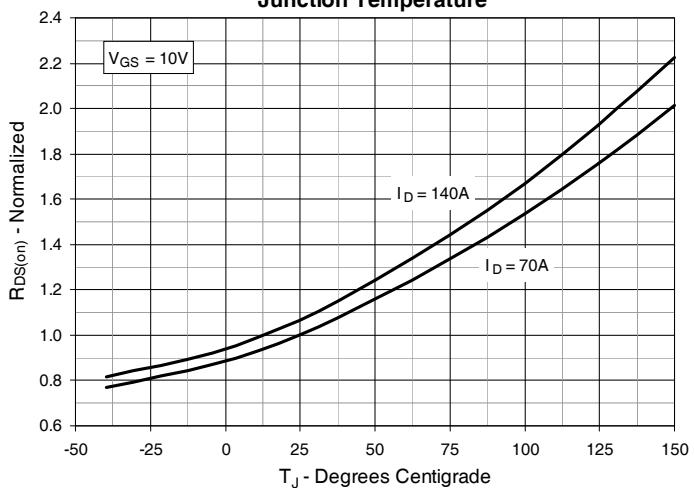
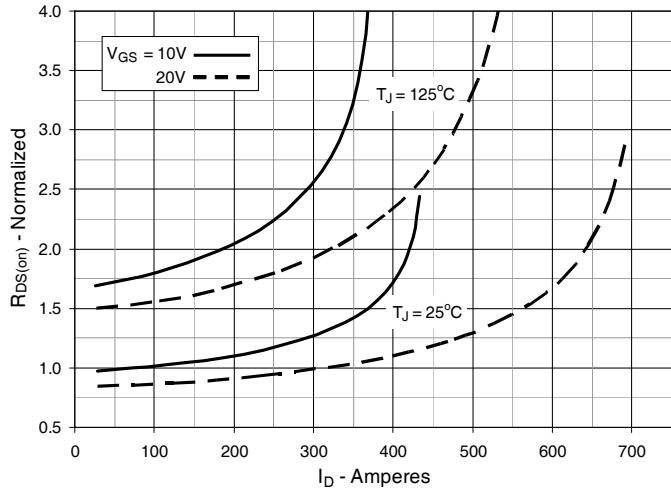
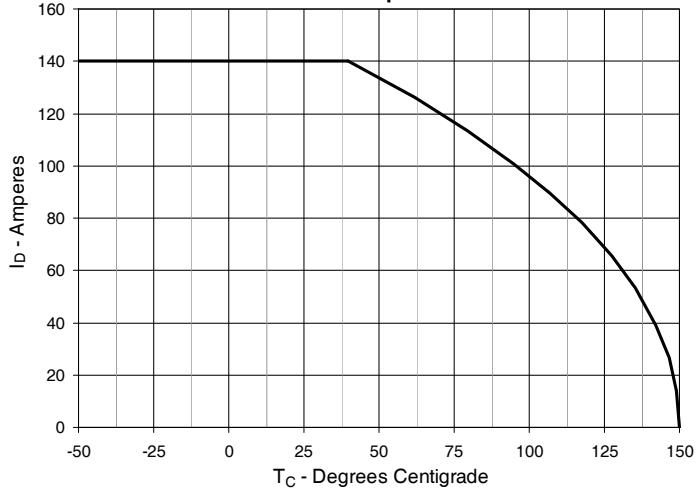
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 70\text{A}$ Value vs. Junction Temperature

Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 70\text{A}$ Value vs. Drain Current

Fig. 6. Maximum Drain Current vs. Case Temperature


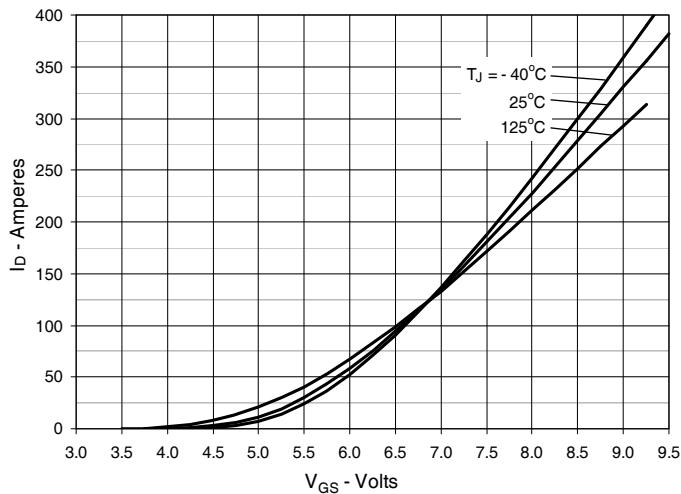
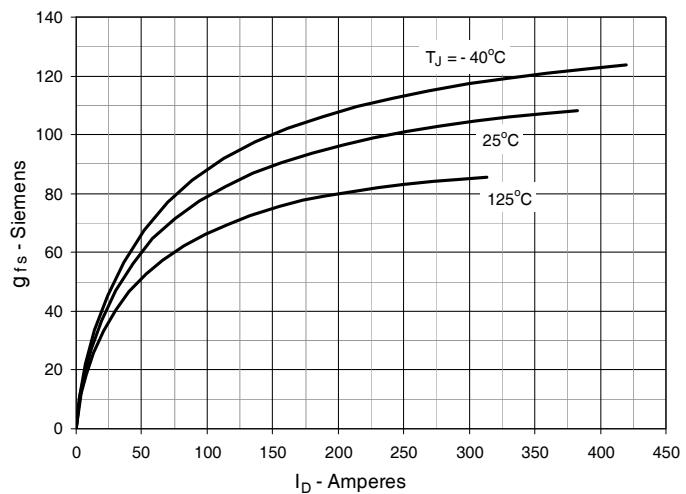
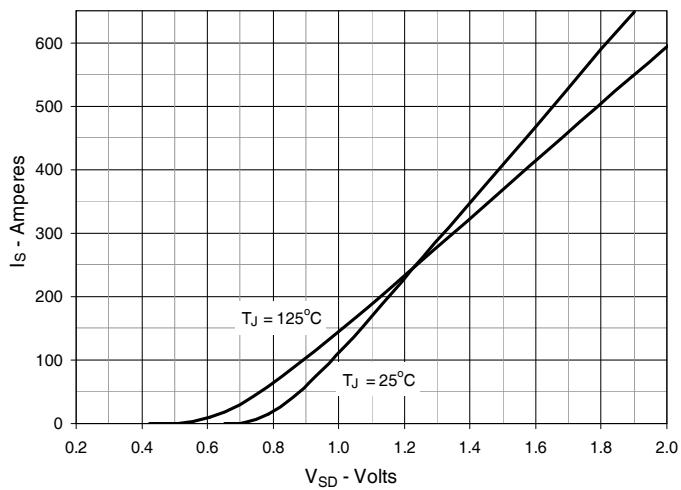
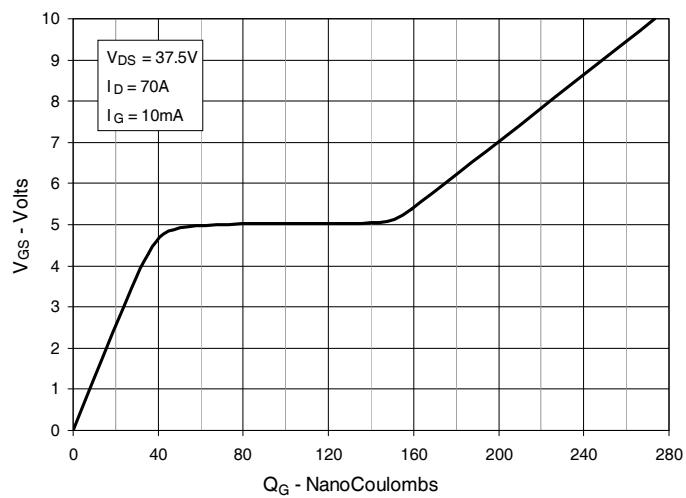
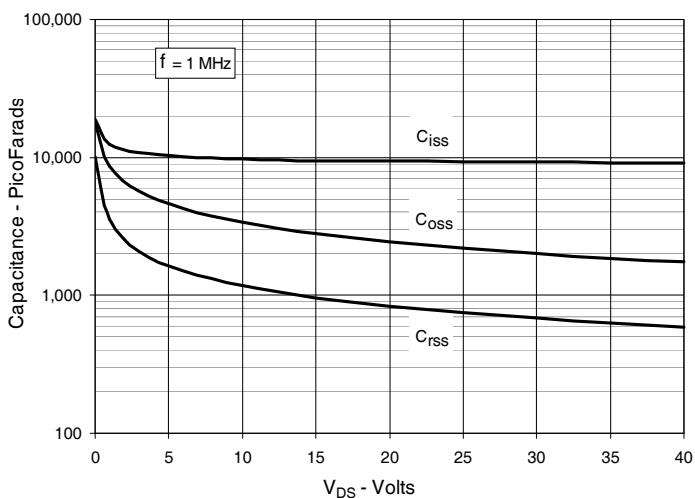
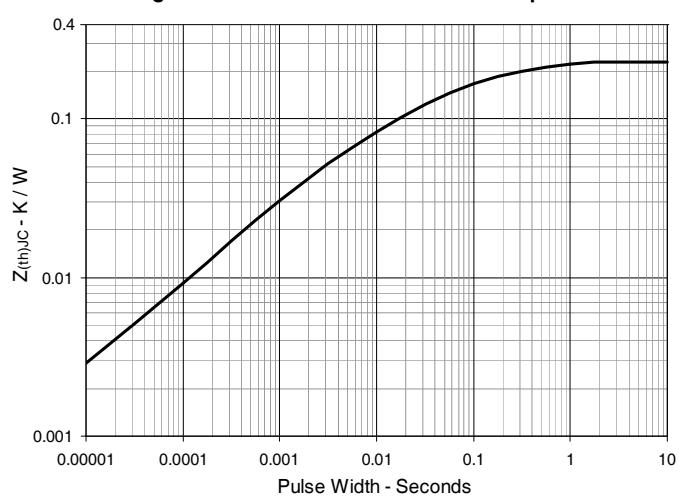
Fig. 7. Input Admittance

Fig. 8. Transconductance

Fig. 9. Forward Voltage Drop of Intrinsic Diode

Fig. 10. Gate Charge

Fig. 11. Capacitance

Fig. 12. Maximum Transient Thermal Impedance


Fig. 13. Forward-Bias Safe Operating Area

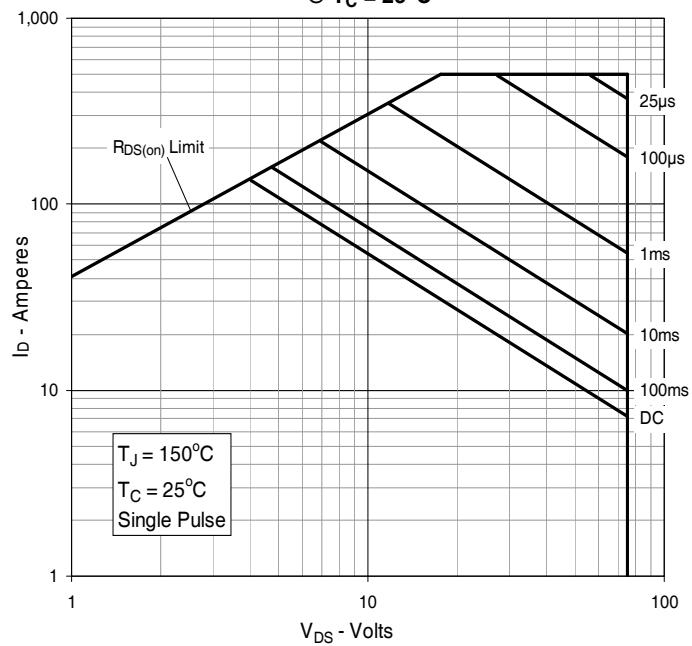
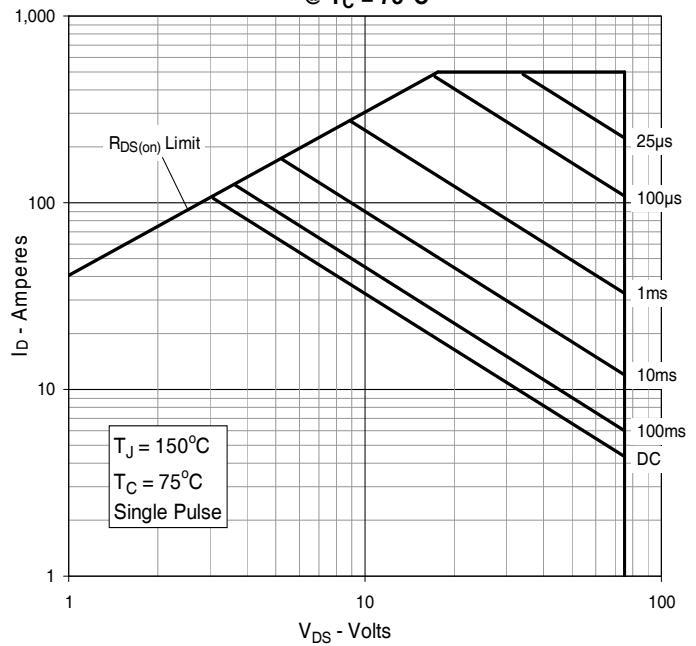
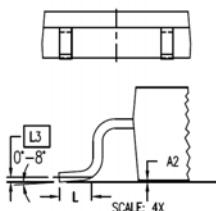
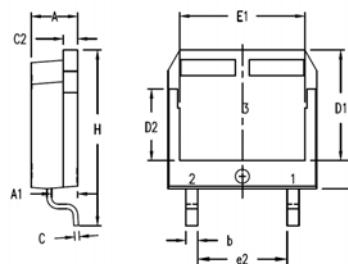
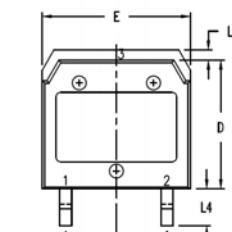
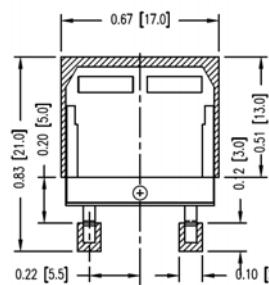
@ $T_C = 25^\circ\text{C}$ 

Fig. 14. Forward-Bias Safe Operating Area

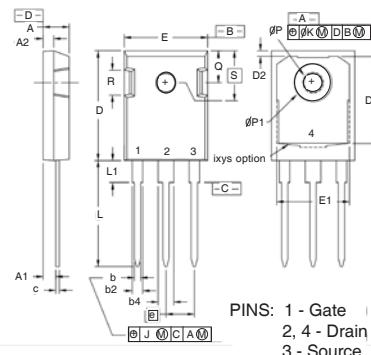
@ $T_C = 75^\circ\text{C}$ 

TO-268HV Outline


PINS:
1 - Gate 2 - Source
3 - Drain



SYM	INCHES		MILLIMETER	
	MIN	MAX	MIN	MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.001	.010	0.02	0.25
b	.045	.057	1.15	1.45
C	.016	.026	0.40	0.65
C2	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D1	.465	.476	11.80	12.10
D2	.295	.307	7.50	7.80
D3	.114	.126	2.90	3.20
E	.624	.632	15.85	16.05
E1	.524	.535	13.30	13.60
e	.215	BSC	5.45	BSC
(e2)	.374	.386	9.50	9.80
H	.736	.752	18.70	19.10
L	.067	.079	1.70	2.00
L2	.039	.045	1.00	1.15
L3	.010	BSC	0.25	BSC
L4	.150	.161	3.80	4.10

TO-247 Outline


PINS: 1 - Gate
2, 4 - Drain
3 - Source

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b2	.075	.087	1.91	2.20
b4	.115	.126	2.92	3.20
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
D1	.650	.690	16.51	17.53
D2	.035	.050	0.89	1.27
E	.620	.635	15.75	16.13
E1	.545	.565	13.84	14.35
e	.215	BSC	5.45	BSC
J	--	.010	--	0.25
K	--	.025	--	0.64
L	.780	.810	19.81	20.57
L1	.150	.170	3.81	4.32
øP	.140	.144	3.55	3.65
øP1	.275	.290	6.99	7.37
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.242	BSC	6.15	BSC

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