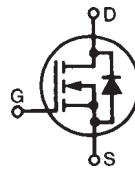


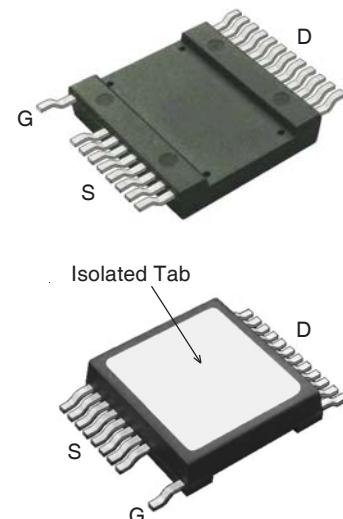
**Polar3™ HiPerFET™
Power MOSFET**
MMIX1F210N30P3

(Electrically Isolated Tab)

N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Rectifier



V_{DSS} = 300V
 I_{D25} = 108A
 $R_{DS(on)}$ ≤ 16mΩ
 t_{rr} ≤ 250ns



G = Gate D = Drain
S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	300	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C , $R_{GS} = 1\text{M}\Omega$	300	V
V_{GSS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	$T_C = 25^\circ\text{C}$	108	A
I_{DM}	$T_C = 25^\circ\text{C}$, Pulse Width Limited by T_{JM}	550	A
I_A	$T_C = 25^\circ\text{C}$	105	A
E_{AS}	$T_C = 25^\circ\text{C}$	4	J
dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$	35	V/ns
P_D	$T_C = 25^\circ\text{C}$	520	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	°C
V_{ISOL}	50/60 Hz, 1 Minute	2500	V~
F_c	Mounting Force	50..200 / 11..45	N/lb
Weight		8	g

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0\text{V}$, $I_D = 3\text{mA}$	300		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 8\text{mA}$	2.5		V
I_{GSS}	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$			$\pm 200 \text{ nA}$
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0\text{V}$ Note 2, $T_J = 125^\circ\text{C}$			$50 \mu\text{A}$ 1.5 mA
$R_{DS(on)}$	$V_{GS} = 10\text{V}$, $I_D = 105\text{A}$, Note 1			$16 \text{ m}\Omega$

Features

- Silicon Chip on Direct-Copper-Bond Substrate
 - High Power Dissipation
 - Isolated Mounting Surface
 - 2500V~ Electrical Isolation
- Dynamic dv/dt Rating
- Avalanche Rated
- Fast Intrinsic Rectifier
- Low $R_{DS(on)}$
- Low Drain-to-Tab Capacitance
- Low Package Inductance

Advantages

- Easy to Mount
- Space Savings

Applications

- DC-DC Converters
- Battery Chargers
- Switch-Mode and Resonant-Mode Power Supplies
- Uninterrupted Power Supplies
- AC Motor Drives
- High Speed Power Switching Applications

Symbol	Test Conditions (T _J = 25°C Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 10V, I_D = 60A$, Note 1	60	100	S
C_{iss}	$V_{GS} = 0V, V_{DS} = 25V, f = 1MHz$	16.2	nF	
C_{oss}		2550	pF	
C_{rss}		42	pF	
R_{GI}	Gate Input Resistance	1.0	Ω	
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10V, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{DSS}$ $R_G = 1\Omega$ (External)	46	ns	
t_r		25	ns	
$t_{d(off)}$		94	ns	
t_f		13	ns	
$Q_{g(on)}$	$V_{GS} = 10V, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{DSS}$	268	nC	
Q_{gs}		80	nC	
Q_{gd}		72	nC	
R_{thJC}			0.24 °C/W	
R_{thCS}		0.05	°C/W	
R_{thJA}		30	°C/W	

Source-Drain Diode

Symbol	Test Conditions (T _J = 25°C Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_s	$V_{GS} = 0V$		210	A
I_{SM}	Repetitive, Pulse Width Limited by T _{JM}		840	A
V_{SD}	$I_F = 100A, V_{GS} = 0V$, Note 1		1.5	V
t_{rr}	$I_F = 105A, -di/dt = 100A/\mu s$ $V_R = 100V, V_{GS} = 0V$	4.1	250	ns
Q_{RM}			28	μC
I_{RM}				A

Notes:

1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.
2. Part must be heatsunk for high-temp I_{DSS} measurement.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

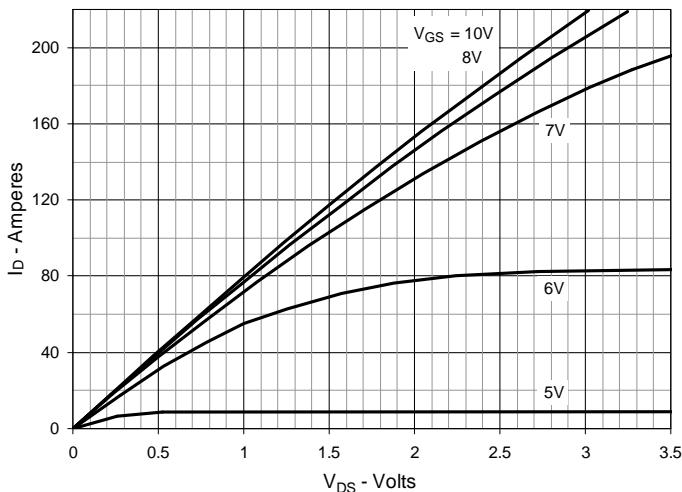
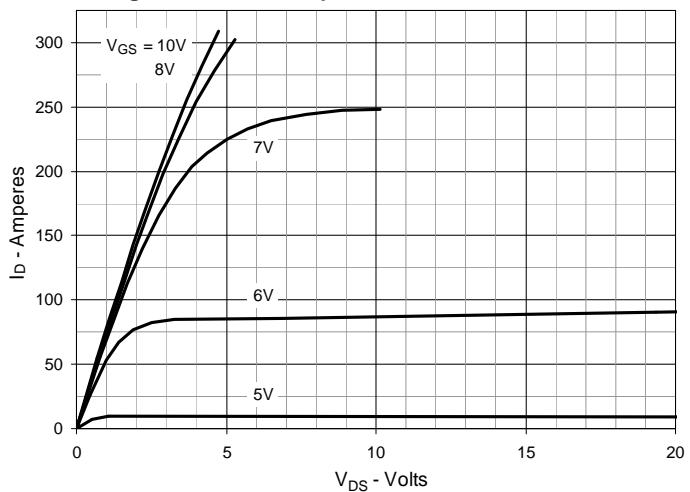
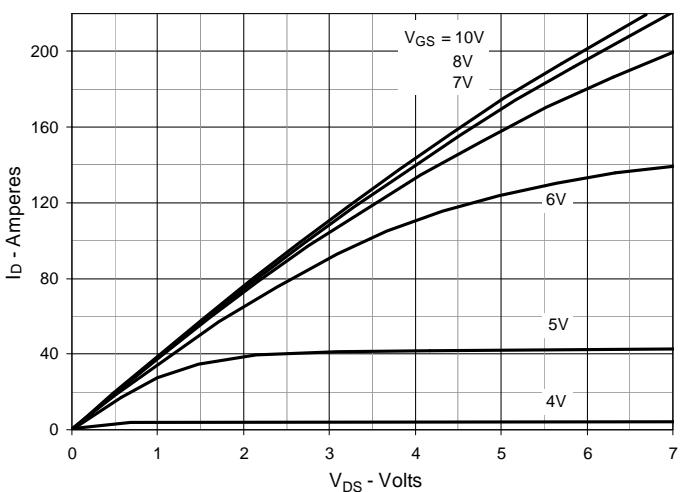
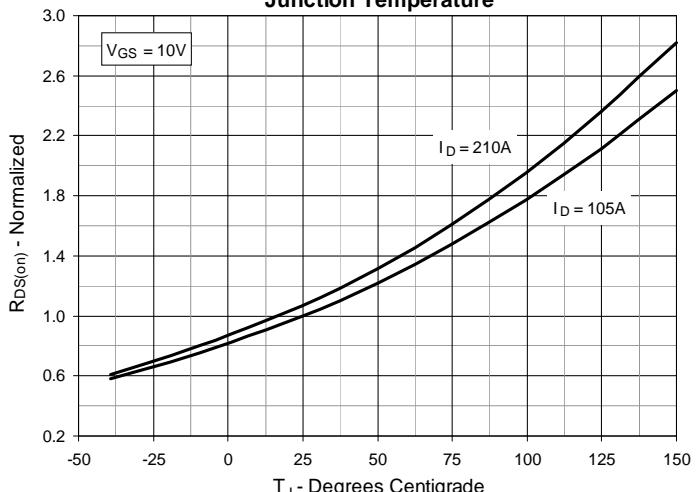
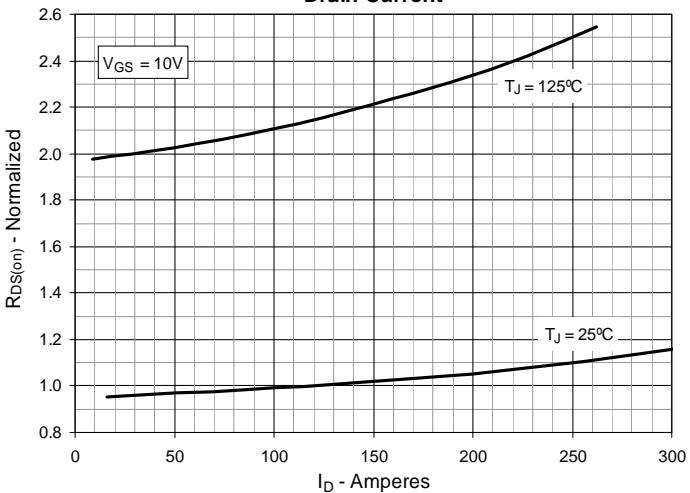
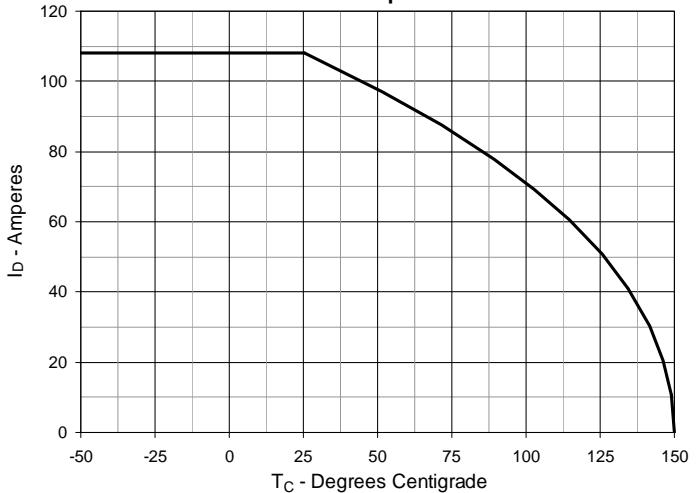
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$ **Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$** **Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$** **Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 105\text{A}$ Value vs. Junction Temperature****Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 105\text{A}$ Value vs. Drain Current****Fig. 6. Maximum Drain Current vs. Case Temperature**

Fig. 7. Input Admittance

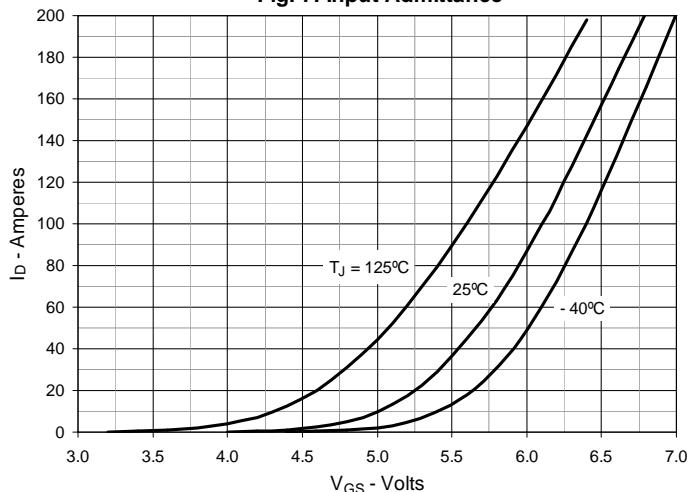


Fig. 8. Transconductance

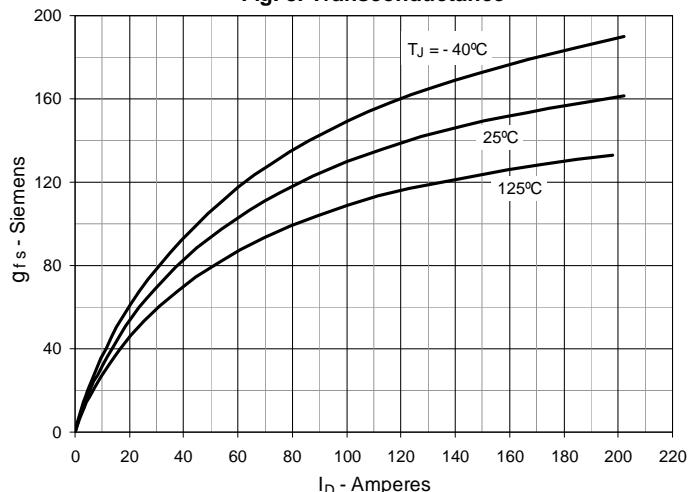


Fig. 9. Forward Voltage Drop of Intrinsic Diode

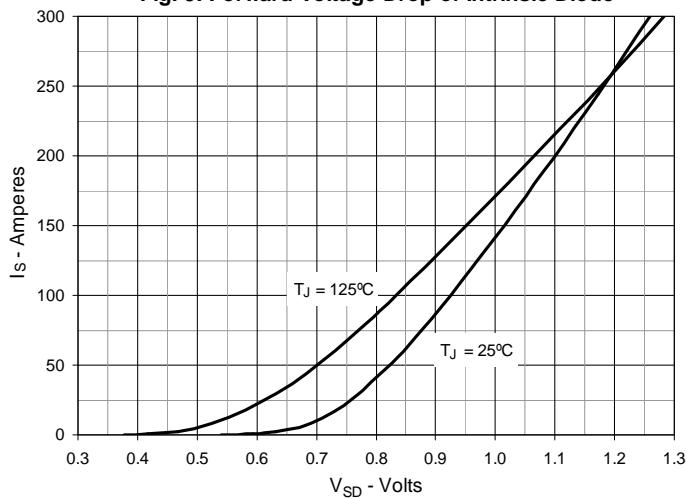


Fig. 10. Gate Charge

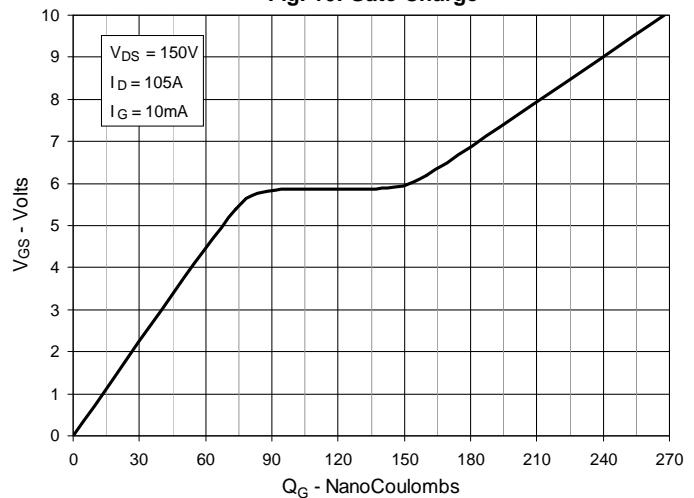


Fig. 11. Capacitance

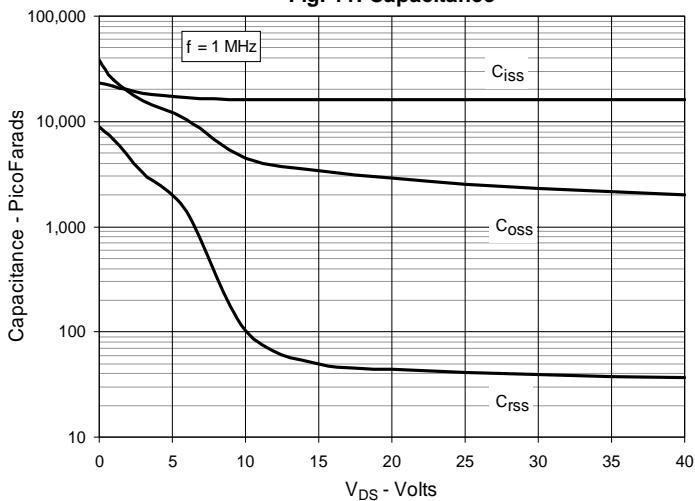


Fig. 12. Forward-Bias Safe Operating Area

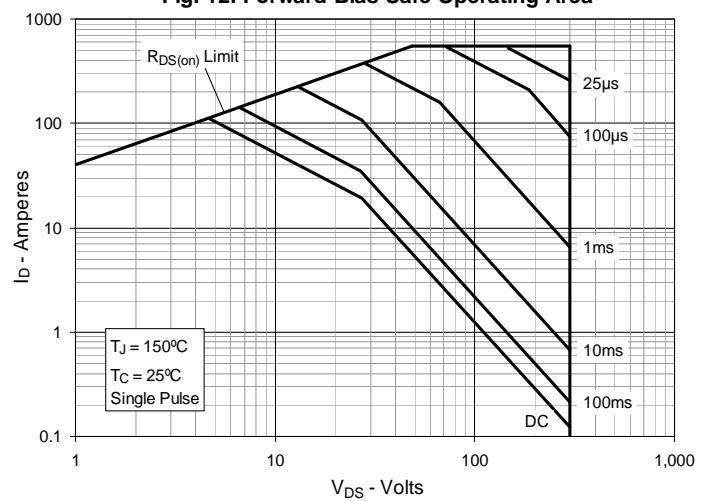
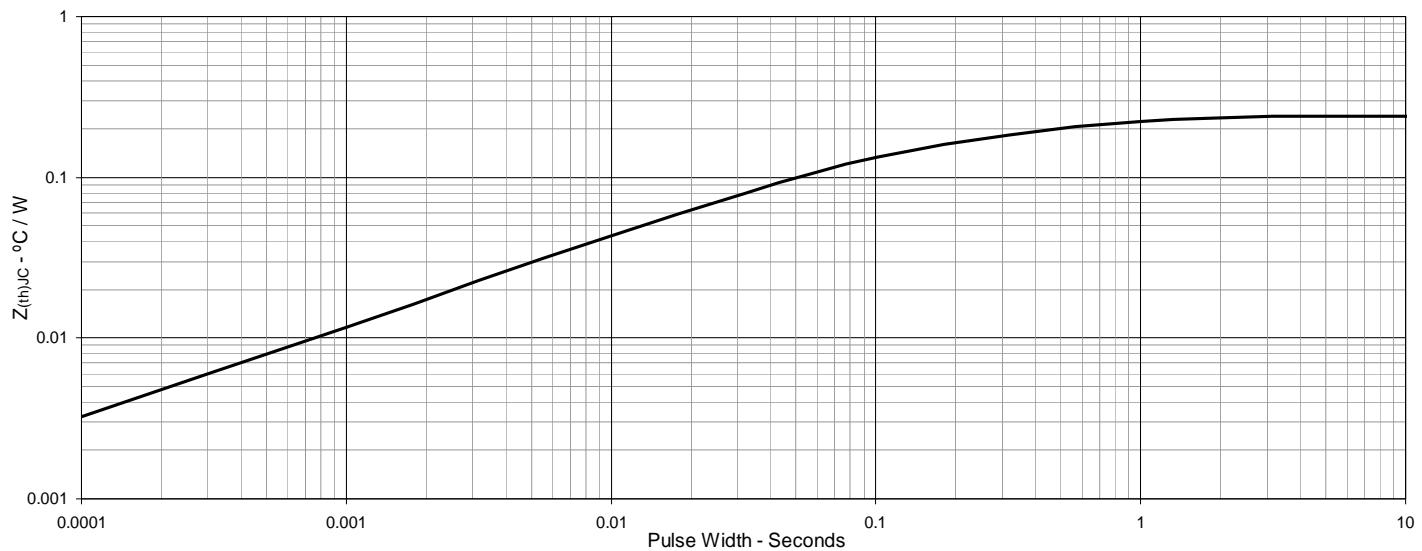
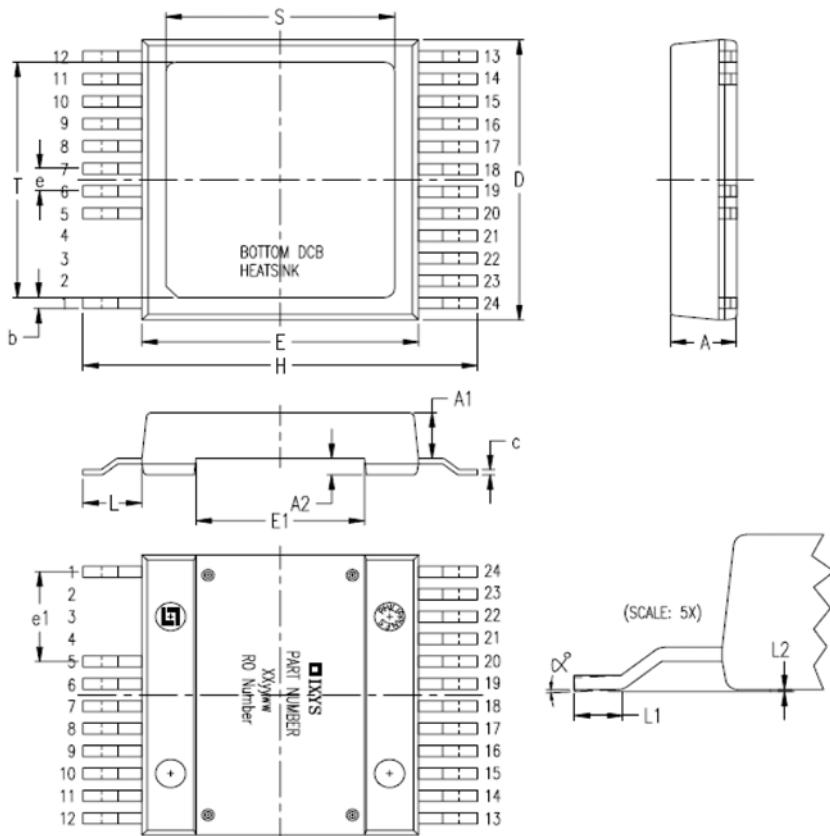


Fig. 13. Maximum Transient Thermal Impedance

Package Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.209	.224	5.30	5.70
A1	.154	.161	3.90	4.10
A2	.055	.063	1.40	1.60
b	.035	.045	0.90	1.15
c	.018	.026	0.45	0.65
D	.976	.994	24.80	25.25
E	.898	.915	22.80	23.25
E1	.543	.559	13.80	14.20
e	.079	BSC	2.00	BSC
e1	.315	BSC	8.00	BSC
H	1.272	1.311	32.30	33.30
L	.181	.209	4.60	5.30
L1	.051	.067	1.30	1.70
L2	.000	.006	0.00	0.15
S	.736	.760	18.70	19.30
T	.815	.839	20.70	21.30
X	0	4°	0	4°

PIN: 1 = Gate
 5-12 = Source
 13-24 = Drain

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