Three phase full Bridge
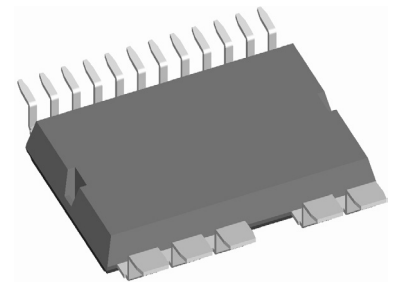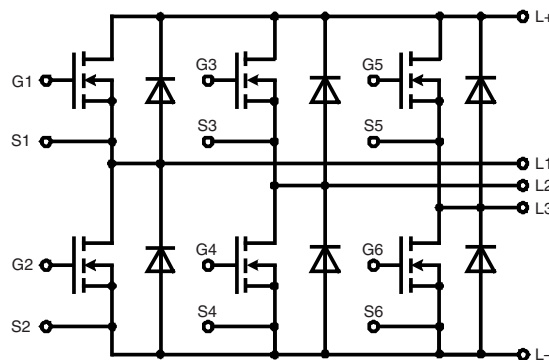## with Trench MOSFETs
in DCB-isolated high-current package

V_{DSS} = 100 V
I_{D25} = 120 A
$R_{DSon\ typ.}$ = 3.2 mΩ

Part number
MTI85W100GC

Surface Mount Device

Features / Advantages:

- MOSFETs in trench technology:
  - low R_{DSon}
  - optimized intrinsic reverse diode
- Package:
  - high level of integration
  - high current capability (300 A max.)
  - aux. terminals for MOSFET control
  - terminals for soldering or welding connections
  - isolated DCB ceramic base plate with optimized heat transfer
- Space and weight savings

Applications:

AC drives
- in automobiles
  - electric power steering
  - starter generator
- in industrial vehicles
  - propulsion drives
  - fork lift drives
- in battery supplied equipment

Package: ISOPLUS-DIL®

- High level of integration
- RoHS compliant
- High current capability
- Aux. Terminals for MOSFET control
- Terminals for soldering or welding connections
- Space and weight savings

IXYS reserves the right to change limits, test conditions and dimensions.

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MOSFETs

Symbol	Definitions	Conditions		min.	typ.	max.	Unit
V_{DSS}	drain source breakdown voltage	T_{VJ} = 25°C to 150°C				100	V
V_{GS}	gate source voltage					±15	V
V_{GSM}	max. transient gate source voltage					±20	V
I_{D25}	continuous drain current	T_C = 25°C				120	A
I_{D90}		T_C = 90°C				90	A
I_{F25}	forward current	T_C = 25°C					A
I_{F90}		T_C = 90°C					A
$R_{DS(on)}$ [1]	static drain source on resistance	on-chip level at I_D = 80 A; V_{GS} = 10 V	T_{VJ} = 25°C		3.2	4	mΩ
			T_{VJ} = 125°C		5.4		mΩ
$V_{GS(th)}$	gate threshold voltage	I_D = 150 µA; V_{DS} = V_{GS}	T_{VJ} = 25°C	2.0		3.5	V
I_{DSS}	drain source leakage current	V_{DS} = V_{DSS}; V_{GS} = 0 V	T_{VJ} = 25°C			1	µA
			T_{VJ} = 125°C		10	100	µA
I_{GSS}	gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V				500	nA
R_G	gate resistance	on-chip level					Ω
Q_g	total gate charge	V_{GS} = 10 V; V_{DS} = 50 V; I_D = 80 A			88		nC
Q_{gs}	gate source charge				30		nC
Q_{gd}	gate drain (Miller) charge				18		nC
$t_{d(on)}$	turn-on delay time	inductive load V_{GS} = 10 V; V_{DS} = 50 V I_D = 80 A; R_G = 39 Ω	T_{VJ} = 125°C		90		ns
t_r	current rise time				55		ns
$t_{d(off)}$	turn-off delay time				480		ns
t_f	current fall time				40		ns
E_{on}	turn-on energy per pulse				130		µJ
E_{off}	turn-off energy per pulse				390		µJ
$E_{rec(off)}$	turn-off reverse recovery losses				10		µJ
R_{thJC}	thermal resistance junction to case					1.2	K/W
R_{thJH}	thermal resistance junction to heatsink	with heat transfer paste (IXYS test setup)			1.5		K/W
		[1] $V_{DS} = I_D \cdot (R_{DS(on)} + 2 \cdot R_{Pin\ to\ Chip})$					

Source-Drain Diode

Symbol	Definitions	Conditions		min.	typ.	max.	Unit
V_{SD}	source drain voltage	I_F = 80 A; V_{GS} = 0 V	T_{VJ} = 25°C		0.9	1.2	V
Q_{RM}	reverse recovery charge	V_R = 50 V; I_F = 80 A; R_G = 39 Ω di/dt = 1500 A/µs	T_{VJ} = 125°C		1.3		µC
I_{RM}	max. reverse recovery current				44		A
t_{rr}	reverse recovery time				45		ns

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Package ISOPLUS-DIL®

Symbol	Definitions	Conditions	min.	typ.	max.	Unit
I_{RMS}	RMS current	per pin in main current paths (P+, N–, L1, L2, L3) may be additionally limited by external connections (PCB tracks)			300	A
T_{stg}	storage temperature		-55		125	°C
T_{op}	operation temperature		-55		150	°C
T_{VJ}	virtual junction temperature		-55		175	°C
V_{ISOL}	isolation voltage	t = 1 second / 50/60 Hz, RMS, $I_{ISOL} \leq 1$ mA	1200			V
		t = 1 minute	1000			V
$R_{pin\text{-}chip}$	resistance terminal to chip	$V_{DS} = I_D \cdot (R_{DS(on)} + 2 \cdot R_{pin\ to\ chip})$		0.6		mΩ
C_P	coupling capacity	between shorted pins and back side metallization		160		pF
F_C	mounting force with clip		50		250	N
Weight				13		g
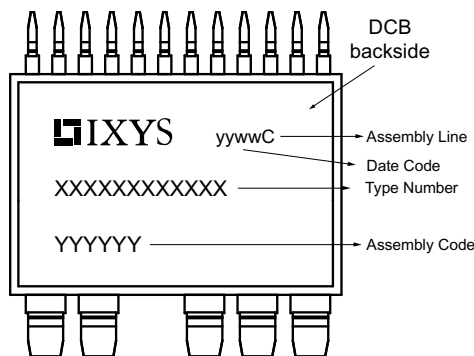
Part number

M = MOSFET
T = Trench
I = Infineon Trench
85 = Current Rating [A]
W = 6-Pack
100 = Reverse Voltage [V]
GC = ISOPLUS-DIL

Ordering	Part Name	Marking on Product	Delivering Mode	Base Qty	Ordering Code
Standard	MTI85W100GC-SMD	MTI85W100GC	Tube	13	516941

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Outlines ISOPLUS-DIL®

Detail A — [A] SEATING PLANE

contact pin:
- galv. tin plating, per pin side: Sn 10...25 µm, undercoating Ni 0,2...1 µm
- stamping edges may be free of tin
- puching burr: ≤ 0,05mm
- Test specification GNP631102

⚠1 Convex bow of substrate, typ. 10–40 µm longitudinal and 5–15 µm transversal

⚠2 Distance between pin and case bottom side.

⚠3 Distance between pin and contact surface.

⚠4 Distance between parallel planes aligned to top and bottom sides of the package

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Fig. 1   Drain source breakdown voltage
V_{DSS} vs. junction temperature T_{VJ}
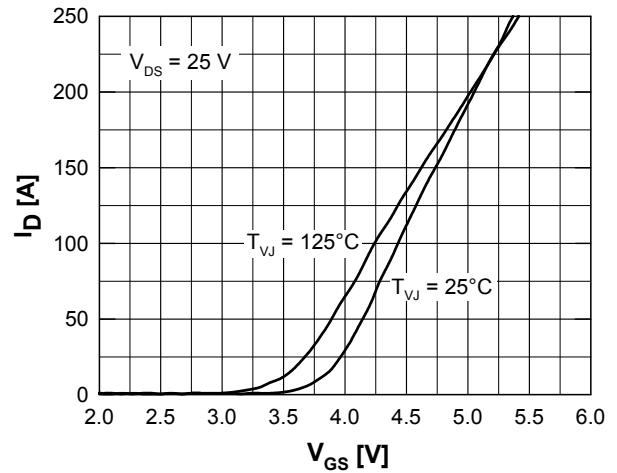
Fig. 2   Typ. transfer characteristics
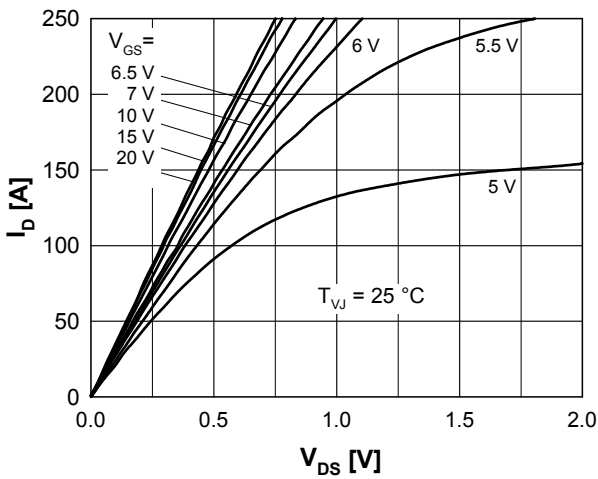
Fig. 3   Typ. output characteristics (25 °C)
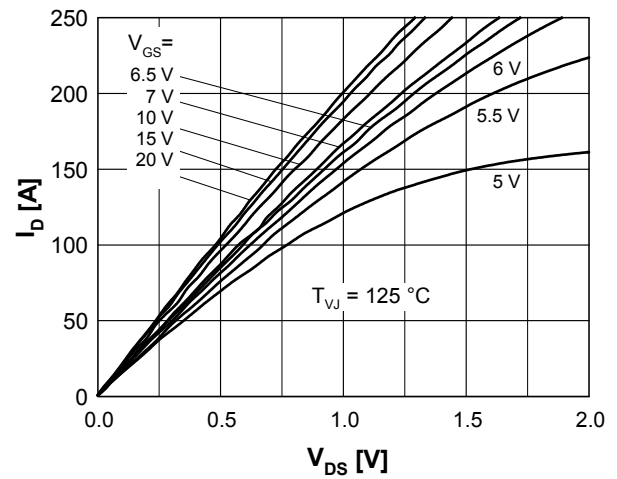
Fig. 4   Typ. output characteristics (125 °C)
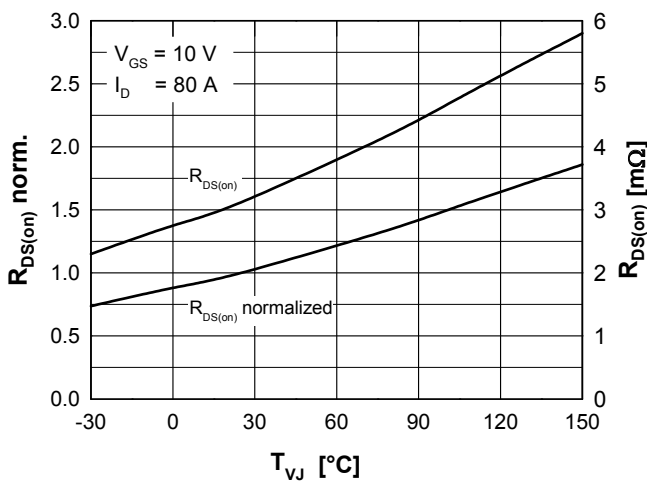
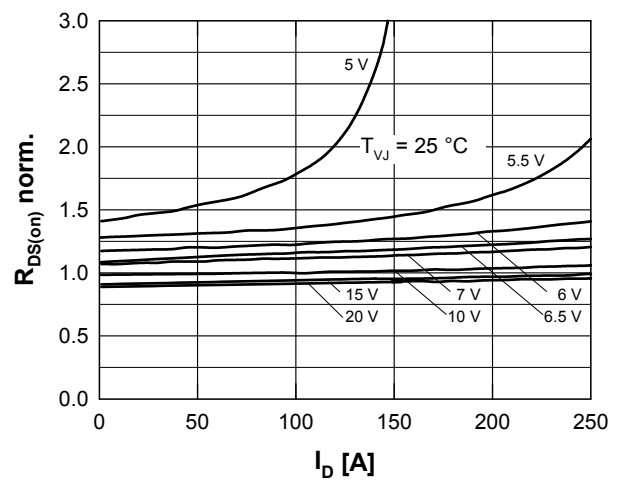Fig. 5   Drain source on-state resistance
versus junction temperature
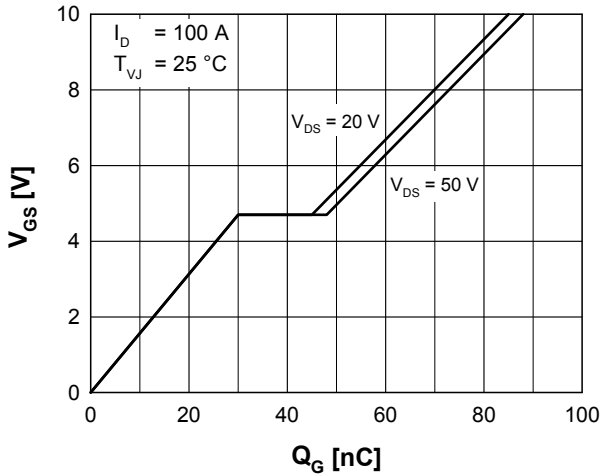

Fig. 6   Drain source on-state resistance
versus I_D

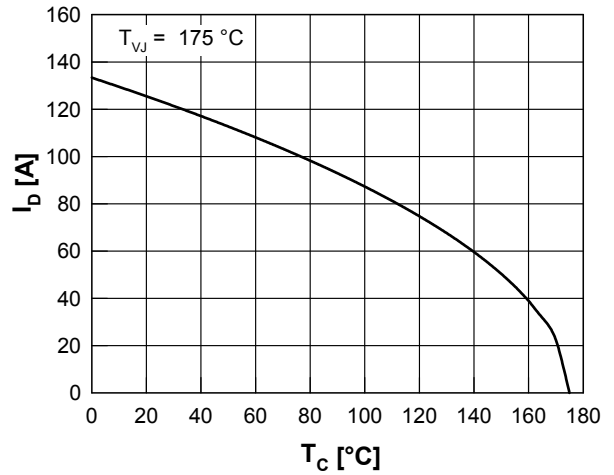IXYS reserves the right to change limits, test conditions and dimensions.

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Fig. 7 Typical turn on gate charge

Fig. 8 Drain current I_D vs. case temperature T_C (chip capability)
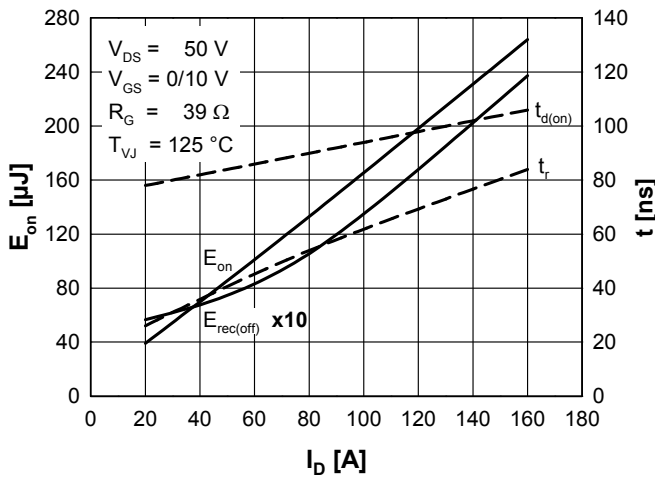
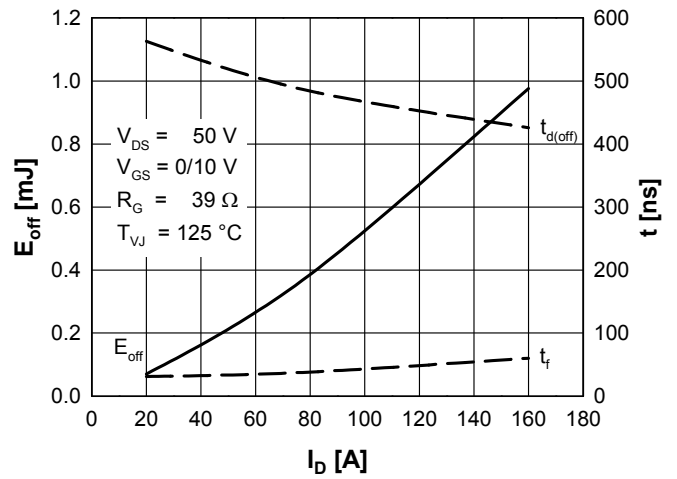Fig. 9 Typ. turn-on energy and switching times versus drain current, inductive switching

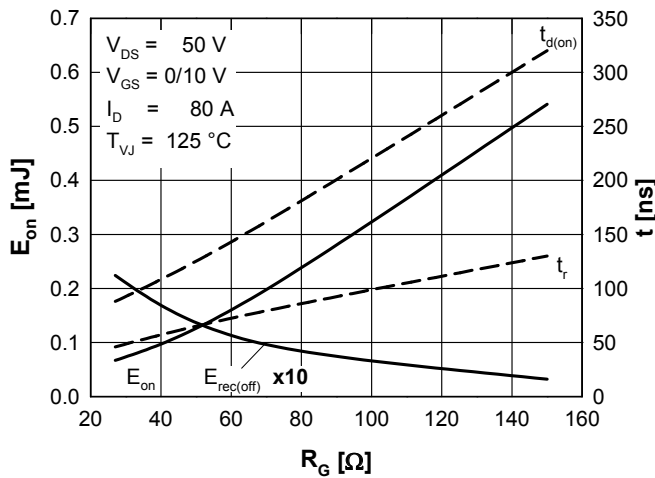Fig. 10 Typ. turn-off energy and switching times versus drain-current, inductive switching

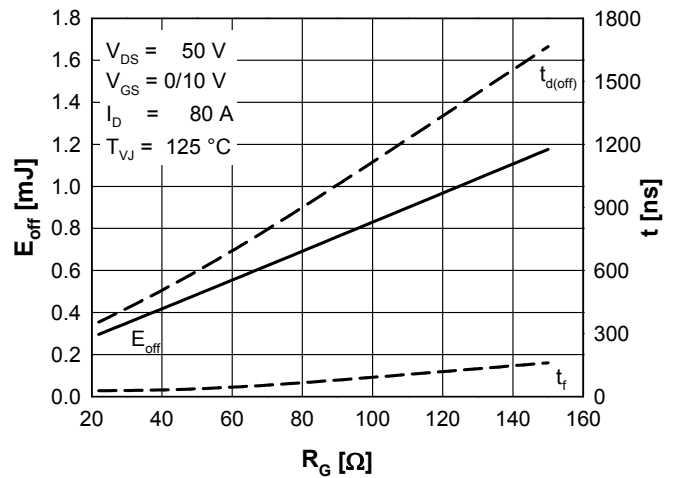Fig. 11 Typ. turn-on energy and switching times versus gate resistor, inductive switching

Fig. 12 Typ. turn-off energy and switching times versus gate resistor, inductive switching
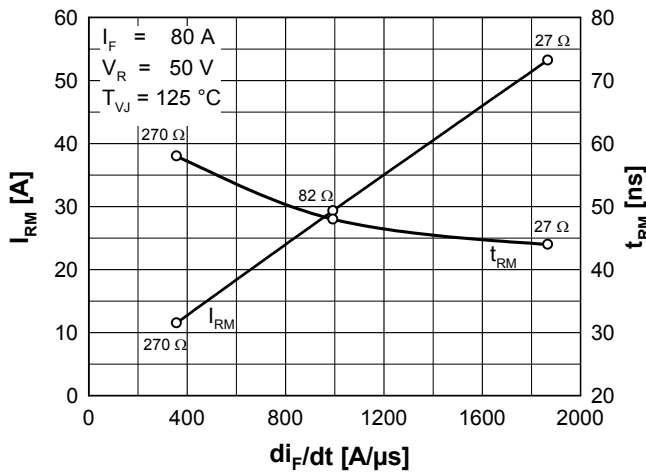
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Fig. 13 Reverse recovery time t_{RM} of the body diode vs. di_F/dt
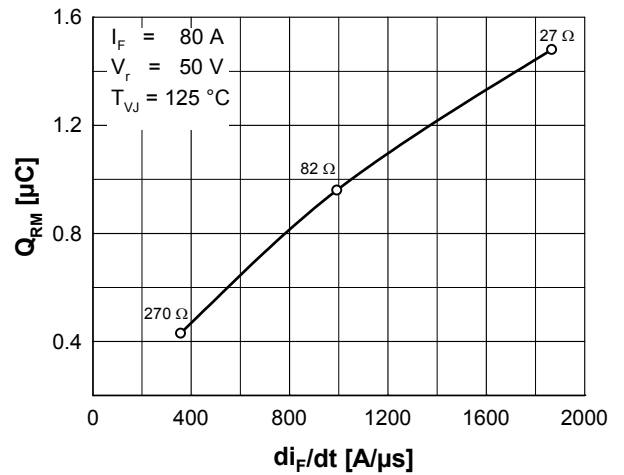

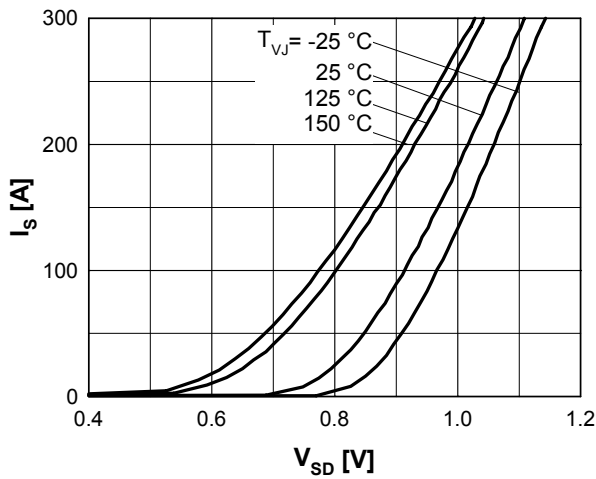Fig. 14 Reverse recovery charge Q_{RM} of the body diode vs. di_F/dt

Fig.15 Source current I_S vs. source drain voltage V_{SD} (body diode)
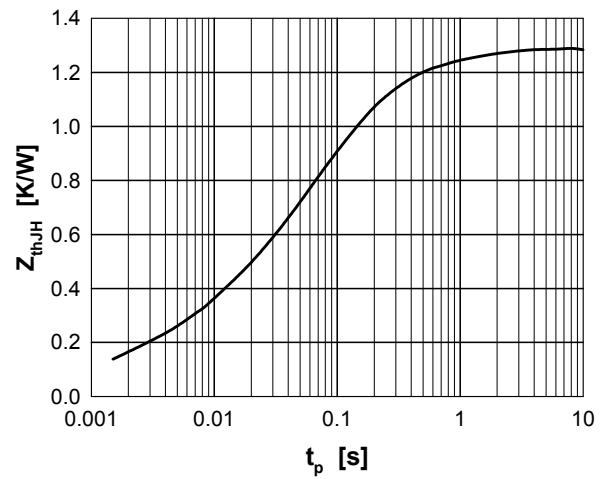

Fig. 16 Typ. thermal impedance junction to heatsink Z_{thJH} with heat transfer paste (IXYS test setup)
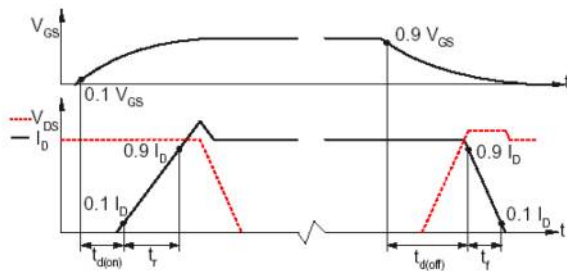

Fig. 17 Definition of switching times

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