



## Description

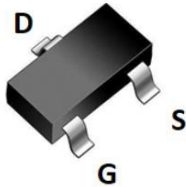
### JMT N-channel MOSFET

#### Features

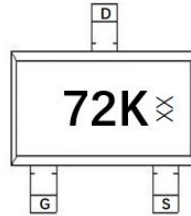
- $V_{DS}=60V$ ,  $I_D=0.25A$   
 $R_{DS(ON)} < 2.2\Omega @ V_{GS} = 10V$   
 $R_{DS(ON)} < 2.87\Omega @ V_{GS} = 5V$
- Advanced Trench Technology
- Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead free product is acquired
- ESD Protected: 2KV

#### Application

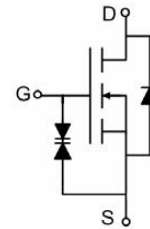
- Battery Operated Systems
- Direct logic-level Interface: TTL/CMOS
- Solid-State Relays



SOT-23 top view



Marking and pin Assignment



Schematic diagram

## Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
72K	JMTL2N7002KS	TAPING	SOT-23	7inch	3000	180000

## Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise specified)

Symbol	Parameter	Max.	Units
$V_{DSS}$	Drain-Source Voltage	60	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current	$T_A = 25^\circ C$	0.25
		$T_A = 100^\circ C$	0.16
$I_{DM}$	Pulsed Drain Current <sup>note1</sup>	1	A
$P_D$	Power Dissipation	$T_A = 25^\circ C$	0.23
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	543	$^\circ C/W$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$



## Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> = 250μA	60	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =60V, V <sub>GS</sub> = 0V,	-	-	1	μA
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V	-	-	±10	uA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1	1.6	2.5	V
R <sub>DS(on)</sub>	Static Drain-Source on-Resistance <small>note2</small>	V <sub>GS</sub> =10V, I <sub>D</sub> =0.3A	-	1.69	2.2	Ω
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =0.2A	-	2.05	2.87	
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1.0MHz	-	28	-	pF
C <sub>oss</sub>	Output Capacitance		-	11	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	4	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 10V, I <sub>D</sub> = 0.3A, V <sub>GS</sub> = 4.5V	-	1.7	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	0.3	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		-	0.6	-	nC
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> = 30V, I <sub>D</sub> =0.2A, R <sub>GEN</sub> = 10Ω, V <sub>GS</sub> =10V,	-	10	-	ns
t <sub>r</sub>	Turn-on Rise Time		-	50	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time		-	17	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	10	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	0.25	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	1	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> =0.25A	-	-	1.2	V

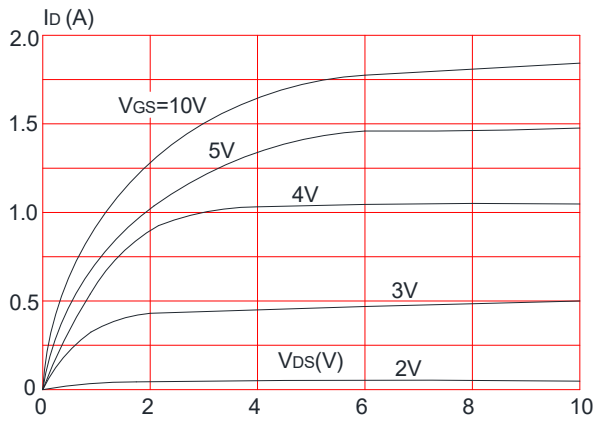
Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%

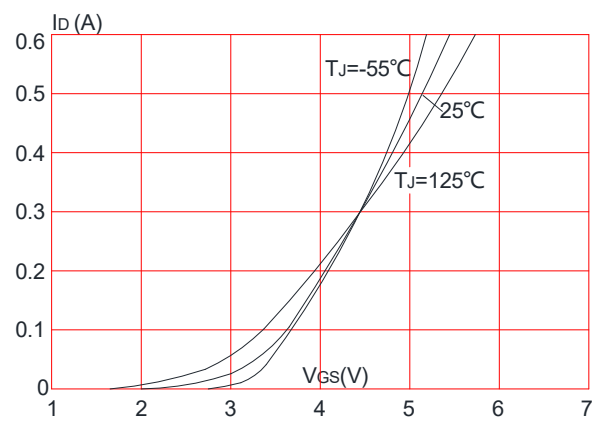


## Typical Performance Characteristics

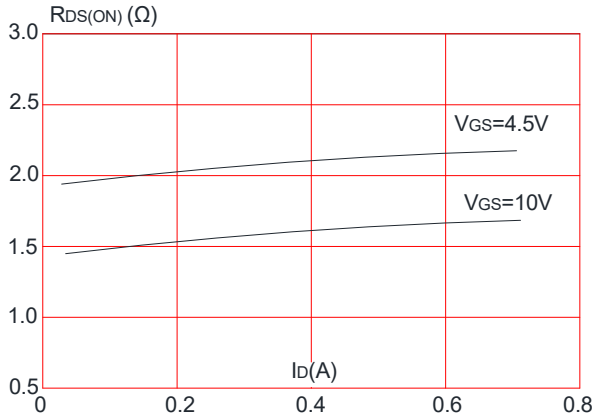
**Figure 1: Output Characteristics**



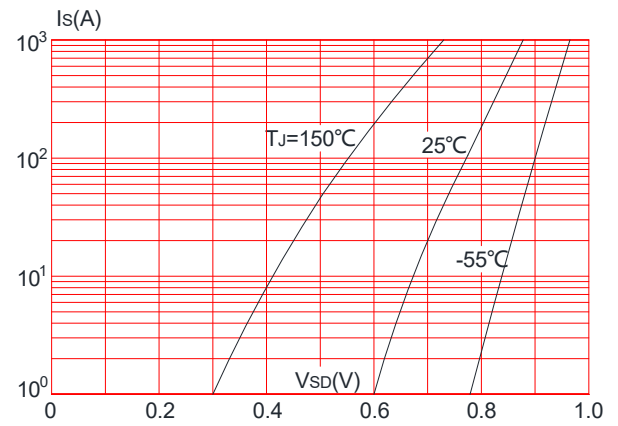
**Figure 2: Typical Transfer Characteristics**



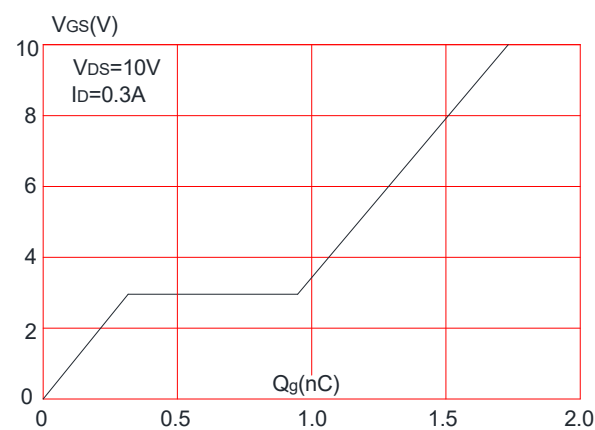
**Figure 3: On-resistance vs. Drain Current**



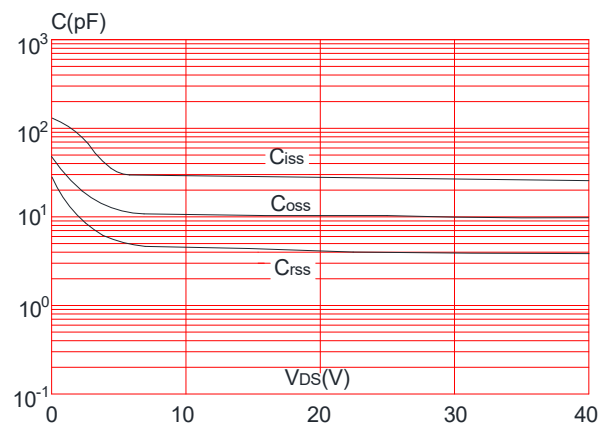
**Figure 4: Body Diode Characteristics**



**Figure 5: Gate Charge Characteristics**



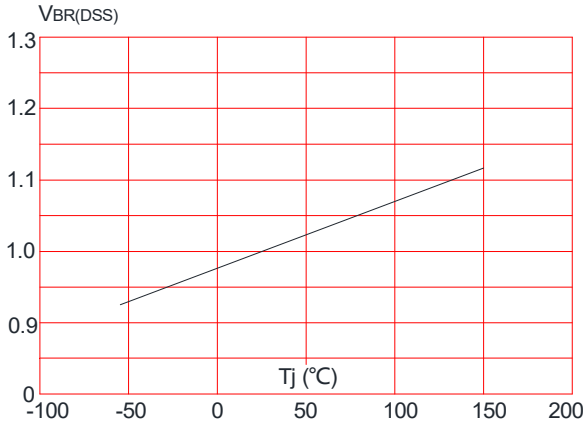
**Figure 6: Capacitance Characteristics**



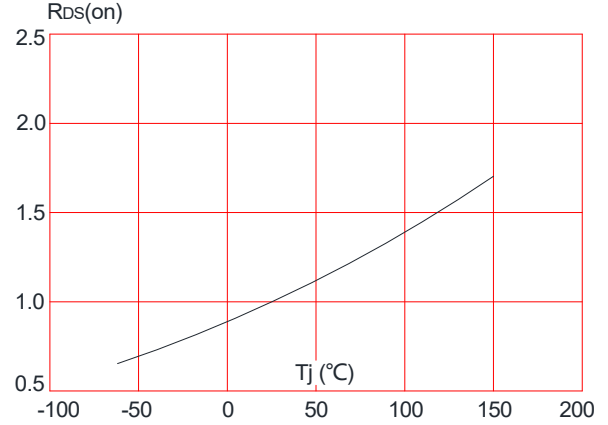


# JMTL2N7002KS

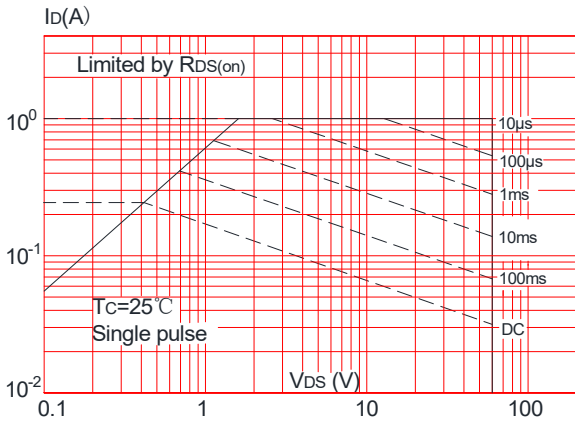
**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



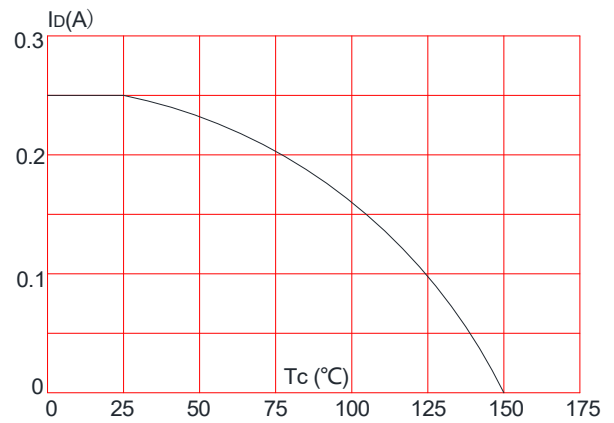
**Figure 8:** Normalized on Resistance vs. Junction Temperature



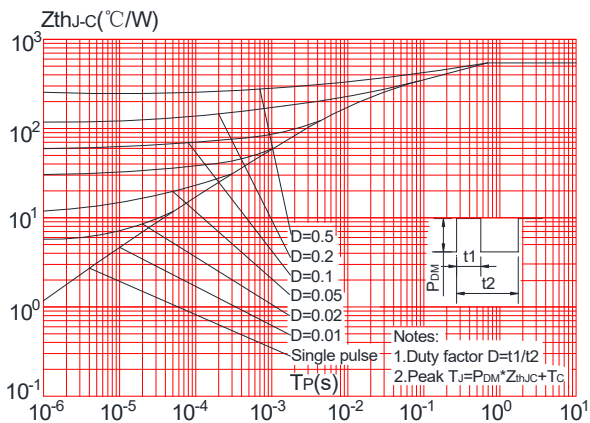
**Figure 9:** Maximum Safe Operating Area



**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature



**Figure 11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case



## Test Circuit

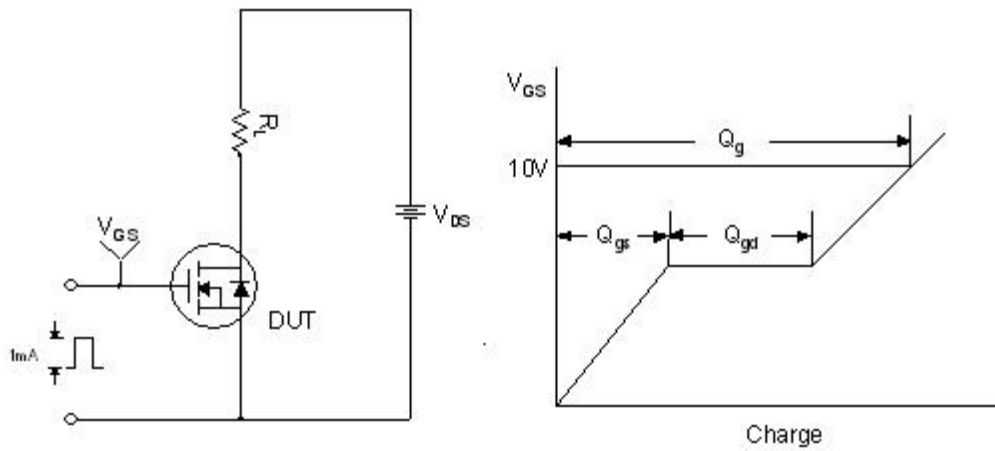


Figure 1. Gate Charge Test Circuit & Waveform

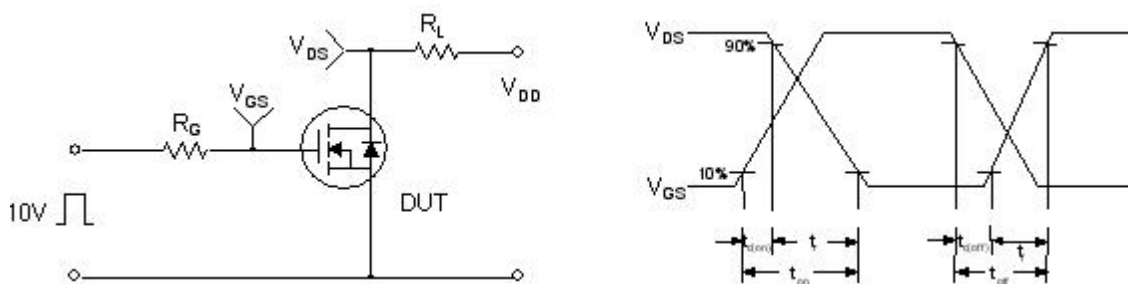


Figure 2. Resistive Switching Test Circuit & Waveforms

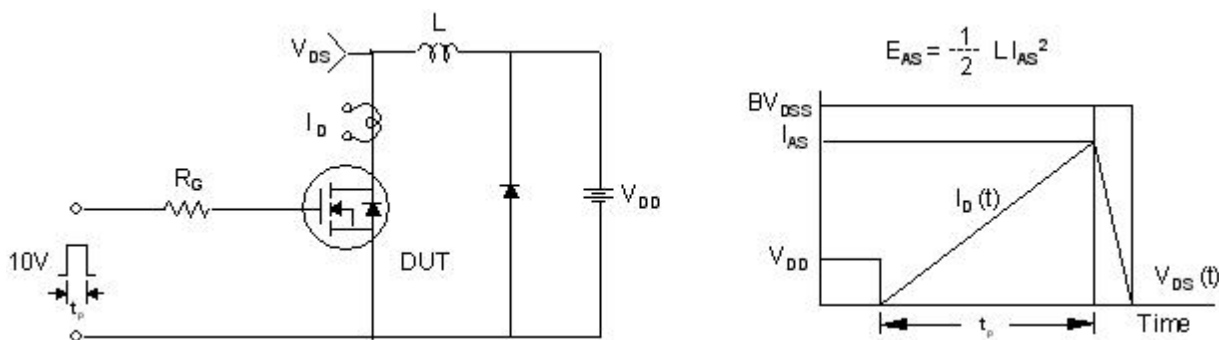
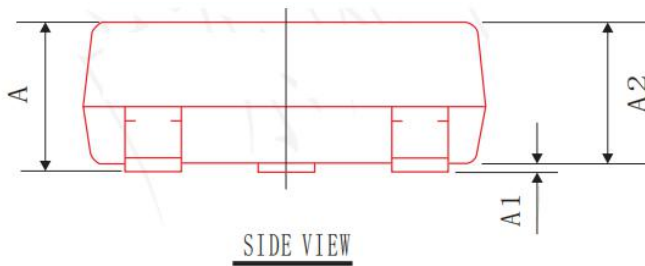
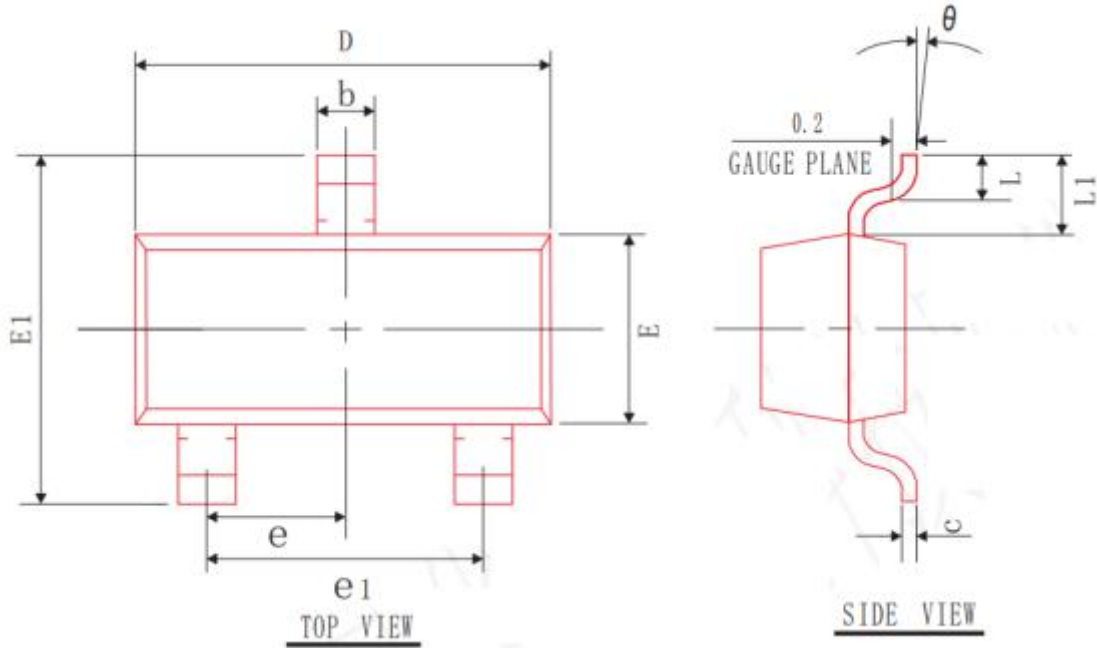


Figure 3. Unclamped Inductive Switching Test Circuit & Waveforms



## Package Mechanical Data




SYMBOL	MIN	NOM	MAX
A	0.90	1.05	1.20
A1	0.00	0.05	0.10
A2	0.90	1.00	1.10
b	0.30	0.40	0.50
c	0.08	0.10	0.15
D	2.80	2.90	3.00
E	1.20	1.30	1.40
E1	2.30	2.40	2.50
L	0.30	0.40	0.50
$\theta$	0°	5°	10°
L1	0.55 REF		
e	0.95 BSC		
e <sub>1</sub>	1.90 REF		



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