

### DESCRIPTION

JW<sup>®</sup>1551 is an active clamp flyback controller for offline flyback converter applications. The JW1551 can be adopted to reduce switching loss and provide high efficiency in whole load range.

JW1551 provide two control outputs, the main power switch control and the active clamp switch control.

JW1551 also has X-cap discharge function to discharge the X-cap when the input is unplugged, which lowers standby power.

The JW1551 is available in QFN4X4-20 package.

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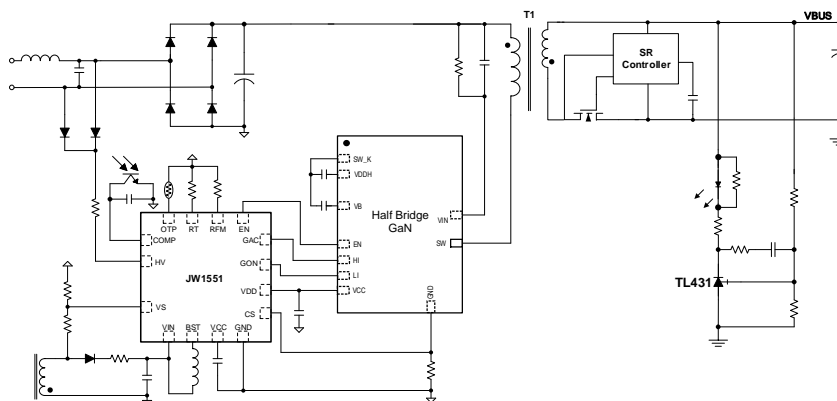
### FEATURES

- Boundary Mode Operation at Heavy Load
- DCM Operation at Light Load
- Burst Mode Control
- Built-in Soft-start Function
- X-cap Discharge Function
- Include a Boost Converter, Allow Vin Range 2.5-38V
- Maximum Frequency Setting with a Single External Resistor
- Adjustable Line Compensation
- High Switching Frequency up to 1.5MHz
- Reliable Fault Protections: VIN OVP/UVP, VS OVP/UVP, SCP, Brown-In/Out, OTP, CS Open and Short Protection
- QFN4X4-20 Package

### APPLICATIONS

- Adaptor

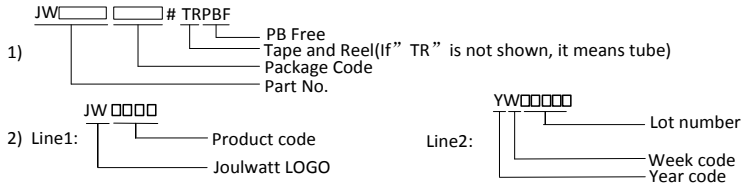
### TYPICAL APPLICATION



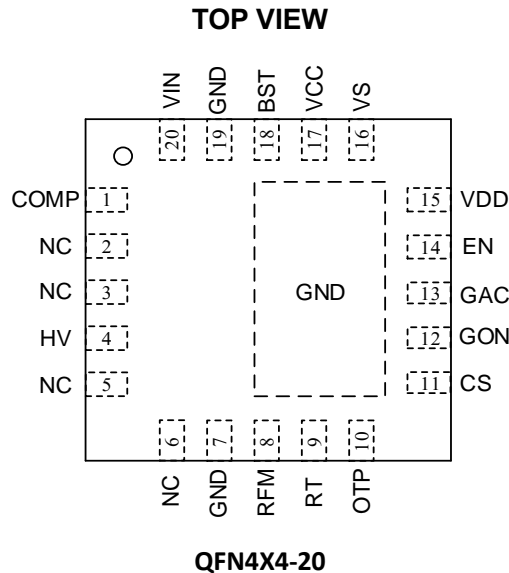
**ORDER INFORMATION**

DEVICE <sup>1)</sup>	PACKAGE	TOP MARKING <sup>2)</sup>
JW1551QFNAH#TRPBF	QFN4X4-20	JW1551 YW□□□□□

Note:



**PIN CONFIGURATION**



**ABSOLUTE MAXIMUM RATING<sup>1)</sup>**

HV.....	-0.3 to 600V
VDD.....	-0.3 to 16V
VIN, BST, VCC.....	-0.3 to 45V
VS.....	-1.1 to 5V, 5 to 5.5V<10us, -1.3 to -1.1V<10us
GON, GAC, EN.....	-0.3 to 5.5V, 5.5 to 6V<10us
All other Pins.....	-0.3 to 5V, 5 to 5.5V<10us
Junction temperature <sup>2) 3)</sup> .....	150°C
Storage temperature.....	-65°C to +150°C

**RECOMMENDED OPERATION CONDITIONS**

HV.....	0V to 500V
VIN.....	2.5V to 38V
Operating Junction Temperature.....	-40°C to 125°C

**THERMAL PERFORMANCE<sup>4)</sup>**

	$\theta_{JA}$	$\theta_{JC}$
QFN4X4-20.....	43.4	4.1°C/W

**Note:**

- 1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMEND OPERATION CONDITIONS.
- 2) Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

**ELECTRICAL CHARACTERISTICS**

<i>T<sub>A</sub>=25°C, unless otherwise noted</i>						
<b>PARAMETER</b>	<b>SYMBOL</b>	<b>TEST CONDITIONS</b>	<b>MIN</b>	<b>TYP</b>	<b>MAX</b>	<b>UNIT</b>
<b>Supply Voltage Management</b>						
Supply Current from HV	I <sub>VIN_CH</sub>	Current available from HV @VIN=6V, HV=30V	1.2	1.8	2.4	mA
VCC Turn On Threshold	V <sub>CC_ON</sub>		13.8	14.8	15.8	V
VCC Turn Off Threshold	V <sub>CC_OFF</sub>		9.6	10.6	11.6	V
Quiescent Current	I <sub>VCC_Q</sub>	V <sub>COMP</sub> =0V, V <sub>CS</sub> =0V, VCC=12V, output not switching	70	100	130	uA
Operation Current	I <sub>VCC_OP</sub>	VCC=12V, fs=1.5MHz, C <sub>GON/GAC</sub> =open	1.6	2	2.4	mA
VIN UVP Threshold	V <sub>IN_UVP</sub>		1.5	2	2.5	V
VIN OVP Threshold	V <sub>IN_OVP</sub>		38	40.5	43	V
VCC Operation Voltage when Boost Switching	V <sub>CC_MIN</sub>		13	14	15	V
VDD Operation Voltage	V <sub>DD</sub>		12	13	14	V
Boost Frequency	f <sub>BST</sub>		1.2	1.6	2	MHz
<b>Feedback Management (Pin COMP)</b>						
COMP Open Voltage	V <sub>COMP_OPEN</sub>		2.9	3	3.1	V
Internal Pull-up Resistor	R <sub>COMP</sub>		10.5	11.5	12.5	kΩ
Over-Load Set Point	V <sub>COMP_OLP</sub>		2.9	3	3.1	V
COMP Decreasing Level at which the Controller Enters Burst Mode	V <sub>COMPL</sub>		310	345	380	mV
COMP Decreasing Level at which the Controller Exits Burst Mode	V <sub>COMPH</sub>		360	390	420	mV
Power Limiting Debounce Time	t <sub>D_OLP</sub>		75	80	85	ms
Internal Soft Start Time	T <sub>SS</sub>		4	7.5	11	ms
<b>Current Sampling Management (Pin CS)</b>						
Minimum on Time	t <sub>ON_MIN</sub>		150	185	220	ns
SCP Blanking Time	t <sub>BLK</sub>		90	130	170	ns
Maximum on Time	t <sub>ON_MAX</sub>		10	11.5	13	us
Minimum Current Set Point	V <sub>CS_MIN</sub>	VCC=17V, COMP=0.4V to enter Burst Mode	110	135	160	mV
Maximum Current Set Point	V <sub>CS_MAX</sub>	VCC=17V, COMP=3V	540	600	660	mV
Short-circuit Protection Set Point	V <sub>SC</sub>		0.9	1	1.1	V

<i>T<sub>A</sub>=25 °C, unless otherwise noted</i>						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CS UVP Threshold	V <sub>CS_UVP</sub>		200	245	290	mV
Line-compensation Current Ratio <sup>5)</sup>	K <sub>LC</sub>		/	0.02	/	A/A
Propagation Delay of CS Comparator High to GON Low <sup>5)</sup>	t <sub>D(CS)</sub>	V <sub>CS</sub> step from 0V to 1V	/	30	36	ns
<b>Output Management (Pin GON/GAC/EN)</b>						
Output High Level	V <sub>H</sub>		5	5.25	5.5	V
Output Low Level	V <sub>L</sub>		/	0.03	0.3	V
Maximum Source Current	I <sub>SRC</sub>		2	3	/	mA
Maximum Sink Current	I <sub>SNK</sub>		25	30	/	mA
Delay from EN High to GON High	t <sub>D(EN-GON)</sub>		33	39.5	46	us
Delay from GON Low to GAC High <sup>5)</sup>	t <sub>D(GON-GAC)</sub>		/	80	/	ns
<b>Frequency and Dead time Management</b>						
Maximum Switching Frequency	f <sub>sw</sub>		1.2	1.35	1.5	MHz
Maximum Operating Frequency Set	f <sub>MAX</sub>	$f_{MAX} = 25 + \frac{5 \cdot 10^4}{R_{FM} (k\Omega)}$ R <sub>FM</sub> =105kΩ	400	475	550	kHz
Burst Frequency	f <sub>Burst</sub>		22	26	30	kHz
<b>Protection Management</b>						
Thermal Shutdown Threshold <sup>5)</sup>	T <sub>SD</sub>		/	140	/	°C
Thermal Shutdown Recovery Hysteresis <sup>5)</sup>	T <sub>HYS</sub>		/	50	/	°C
Fault Reset Delay Time	t <sub>FRD</sub>		1.5	1.6	1.7	s
NTC Shut-down Voltage	V <sub>NTCTH1</sub>		0.9	1	1.1	V
NTC Recovery Voltage	V <sub>NTCTH2</sub>		2	2.25	2.5	V
NTC Pull-up Current, out of Pin	I <sub>NTC</sub>		90	105	130	uA
Brown in Current Threshold <sup>5)</sup>	I <sub>VS_BI</sub>		410	467	523	uA
Brown out Current Threshold <sup>5)</sup>	I <sub>VS_BO</sub>		352	400	448	uA
VS OVP Current Threshold <sup>5)</sup>	I <sub>VS_OV</sub>		724	800	896	uA
VS UVP Current Threshold <sup>5)</sup>	I <sub>VS_UV</sub>		20	66.6	120	uA

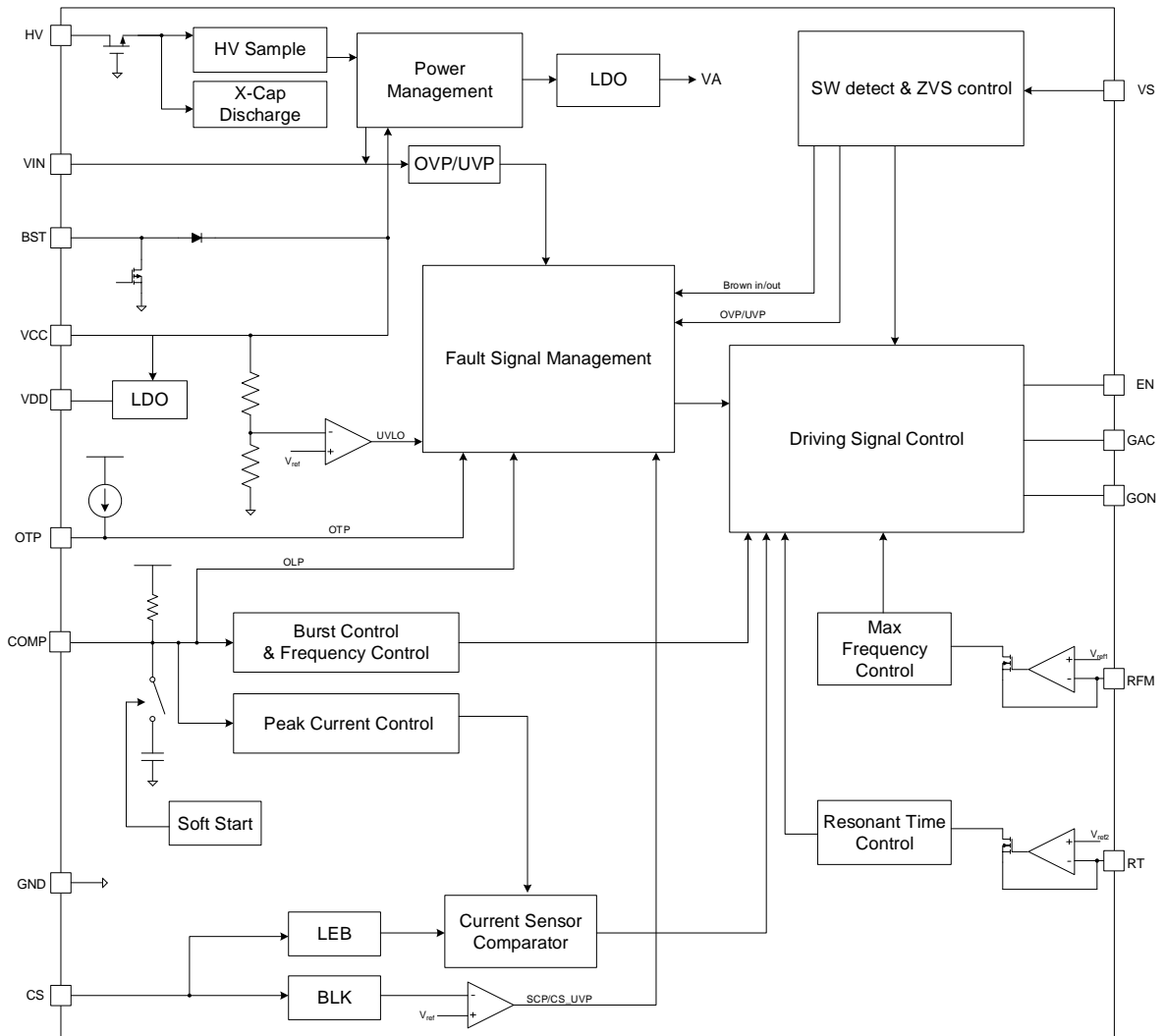
**Note:**

5) Guaranteed by design.

## PIN FUNCTIONS

Pin#	Name	Description
1	COMP	Compensation pin
2	NC	
3	NC	
4	HV	High voltage pin for startup
5	NC	
6	NC	
7	GND	Power ground
8	RFM	Switching converter frequency set
9	RT	Resonant time set
10	OTP	Over temperature protection pin
11	CS	Source of primary switch. Input of the primary current sense signal
12	GON	Enable main primary switch
13	GAC	Enable active clamp switch
14	EN	Enable pin to disable IC
15	VDD	13V regulator output
16	VS	Voltage sensing input pin
17	VCC	Power supply output
18	BST	Boost switching point
19	GND	Power ground
20	VIN	Power supply input

BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

JW1551 is an active clamp flyback controller for offline flyback converter applications.

### 1. Start-Up

Initially, the current source which is drawn from the HV pin drives the controller. The post stage starts switching and the start-up current source turns off after finishing soft start. The system stops switching and start-up current source turns on again when fault or VCC falls below  $V_{CC\_OFF}$ .

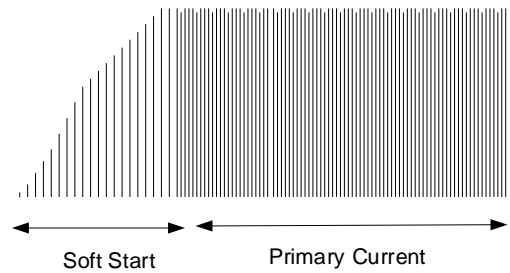


Figure 2: Soft Start

An internal soft-start circuit is included in JW1551 in order to reduce stress on the primary side switch, secondary diode and smoothly establish the output voltage during start-up. The internal soft-start time is about 5ms.

### 2. Normal Operation

#### 2.1 Peak Current and Frequency Control

JW1551 uses an adaptive multi-mode control to improve overall range efficiency. When load is heavy, JW1551 operates in BCM mode, the peak current is regulated according to the load condition. When COMP decreases, the controller enters BUR mode with  $N_{BUR}$  cycles which the peak current and switching frequency are fixed and BUR frequency is changing. When COMP decreases further, the controller enters DCM(PFM/PWM) mode, the switching frequency is folded back to 25kHz while freezing the peak current. When the load decrease to a given level, the controller freezes the frequency at 25kHz while decreasing its peak current until JW1551 enters Burst mode. During Burst mode, the peak current reaches its minimum value.

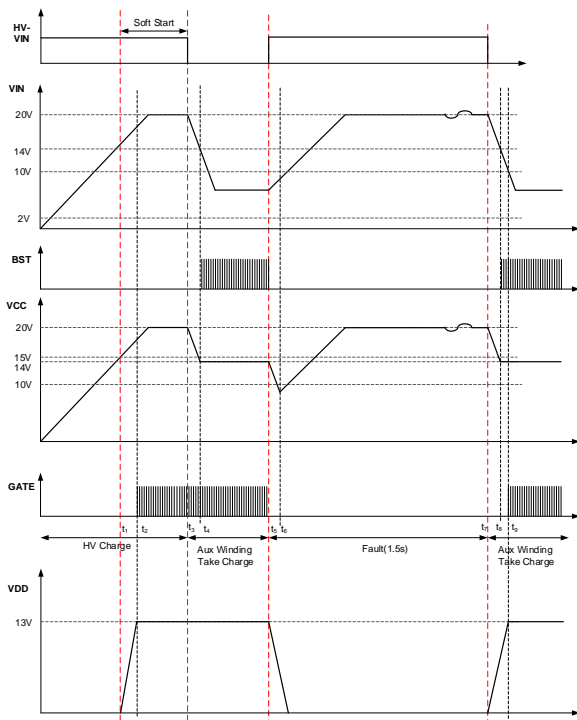


Figure 1: VCC UVLO



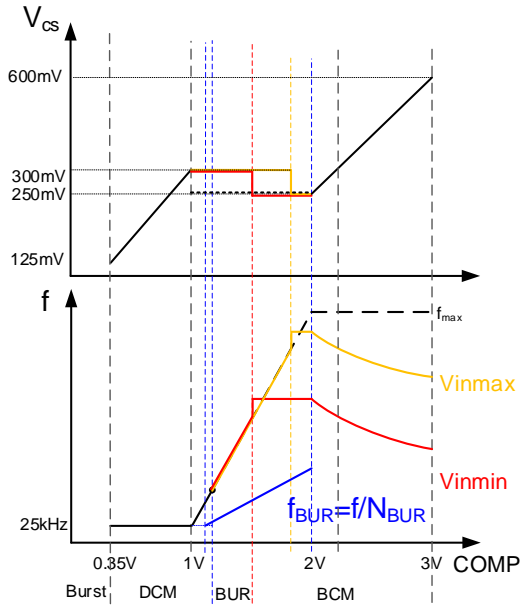


Figure 3: Peak Current and Frequency

JW1551 provides two signals GON and GAC to control the primary-side switch and the auxiliary switch. GON is turned on at the valley of  $V_{sw}$  when reaching the setting frequency and turned off when  $i_{pk}$  reaching the setting value according to COMP. When GON is off, GAC keeps on after dead time until the magnetizing current falls around 0, then GAC will be turned off. Then the primary switch can be turned on again with ZVS or valley switching.

2.2 BCM Operation

JW1551 operates in boundary conduction mode (BCM) at heavy load. In BCM, the converter operates with ZVS by proper control of GAC.

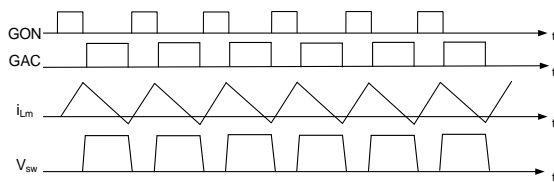


Figure 4: BCM Waveforms

2.3 BUR Operation

When  $COMP < 2V$ , the JW1551 features BUR operation with  $N_{BUR}$  cycles which the peak

current and switching frequency are fixed and BUR frequency  $f_{BUR}$  is changing.

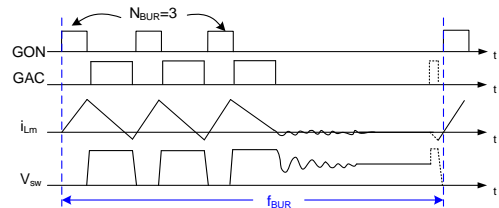


Figure 5: BUR Waveforms

2.3 DCM(PFM/PWM) Operation

The JW1551 features discontinuous conduction mode (DCM) operation at light load, where the JW1551 turns off the auxiliary switch when the magnetizing current is zero.

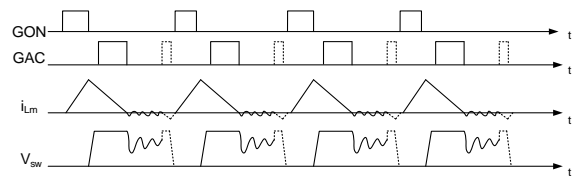


Figure 6: DCM Waveforms

2.4 Burst Operation

The JW1551 implements burst mode at no load and light load to lower stand-by power consumption. As the load decreases, the COMP voltage decreases. The controller stops the post stage when the COMP drops below  $V_{COMPL}$  (0.35V) and exit burst mode when COMP exceeds  $V_{COMPH}$  (0.4V).

GAC keeps switching during Burst mode the same as DCM mode.

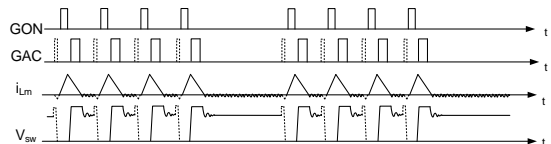


Figure 7: Burst Waveforms

3. Other Functions and Features

**3.1 Boost Converter**

To improve the efficiency of wide range output, JW1551 integrates a Boost converter internally. An inductor between VIN and BST pin is required for proper operation.

The Boost converter will enter burst mode in light load to improve efficiency further.

**3.2 X-Cap Discharge Function**

X-cap is typically positioned across a power supply’s input terminals to filter differential mode EMI noise. These components pose a potential hazard because they can store unsafe levels of voltage energy after the AC line is disconnected. Generally, resistors in parallel to the X-cap provide a discharge path to meet safety standards. However, this method produces a constant loss while the AC is connected, and contributes to no-load and standby input power consumption. Smart X-cap discharger is included in JW1551 to discharge X-cap only when AC lines unplug is detected.

**3.3 Resonant Time Setting**

The RT pin is used to set the parasitic resonant period to achieve better valley turn-on time. Set  $t_d$  to one quarter resonance period in DCM. The  $t_d$  is controlled by the resistor connected between RT pin and GND pin which can be represented as

$$t_d(\text{ns}) = K_d * R_{td}(\text{k}\Omega)$$

Where  $K_d$  is the ratio of  $t_d$  to  $R_{td}(\text{ns}/\text{k}\Omega)$  and can be approximated as 2.8~3.2.

**3.4 Maximum Frequency Setting**

The maximum switching frequency limit( $f_{MAX}$ ) of JW1551 can be set by RFM pin to meet different applications. The  $f_{MAX}$  is controlled by the resistor connected between RFM pin and GND pin which can be represented as

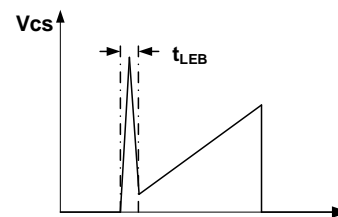
$$f_{MAX}(\text{kHz}) = 25 + \frac{5 * 10^4}{R_{FM}(\text{k}\Omega)}$$

**3.5 QR Frequency Quivering**

To achieve good EMI performance, frequency quivering method is integrated in JW1551. The frequency quivering in QR operation is achieved by peak current perturbation.

**3.6 Leading Edge Blanking**

In order to avoid the premature termination of the switching pulse due to the parasitic capacitance, an internal leading-edge blanking (LEB) is used between the CS pin and the current comparator input. The current comparator is disabled and can’t turn off the gate during the blanking time.



**Figure 8: LEB Blanking**

**3.7 Line Voltage Compensation**

The variation of max output power in QR system can be rather large if no compensation is provided. By placing a resistor externally in series on the current sense resistors and the CS pin, JW1551 can compensate the increased output power limit at higher AC voltage.

**4. Protections**

**4.1 VIN OVP/UVP**

VIN is the input voltage for the Boost converter. It has internal OVP and UVP protection. Once the fault is triggered, the controller shuts down and restarts after  $t_{FRD}$ .

#### 4.2 Brown-in and Brown-out

The line input voltage is detected by VS pin during GON on period, and then compared to the internal run and stop thresholds. A wide separation of run and stop thresholds allows clean start-up and shut-down of the power supply with the line voltage.

#### 4.3 Over Load Protection (OLP)

JW1551 turns off the switch when the power supply undergoes an overload. A fault signal is triggered when COMP pulls up to  $V_{COMP\_OLP}$  for  $t_{D\_OLP}$ . Then the controller shuts down and restarts after  $t_{FRD}$ .

#### 4.4 Short-Circuit Protection (SCP)

The JW1551 has short-circuit protection if  $V_{CS}$  reaches  $V_{SCP}$  after a reduced leading-edge blanking time  $t_{BLK}$  for three consecutive cycles. If SCP is triggered, the controller restarts after  $t_{FRD}$ .

#### 4.5 CS Pin Open/Short

When CS pin is open, the internal bias current will flow to the parasitic capacitance on the CS pin,  $V_{CS}$  will increase. If  $V_{CS}$  is above the  $V_{SC}$  within  $t_{BLK}$ , GON will be turned off right now. Once the fault is detected, the controller shuts down and restarts after  $t_{FRD}$ .

If CS pin is short, the JW1550A will integrate the current from VS pin when GON is high. If  $V_{CS}$  is below the  $V_{CS\_UVP}$  when the integral reaches 3.05nC, a CS-UVP fault is asserted and the

device shuts down and restarts after  $t_{FRD}$ .

#### 4.6 Output OVP/UVP (VS OVP/UVP)

The output over-voltage protection is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds over-voltage protection threshold for three consecutive switching cycles, a VS-OVP fault is asserted and the device shuts down and restarts after  $t_{FRD}$ .

If the voltage sample on VS pin continues below the under-voltage protection threshold for three consecutive switching cycles, a VS-UVP fault is asserted and the device shuts down and restarts after  $t_{FRD}$ .

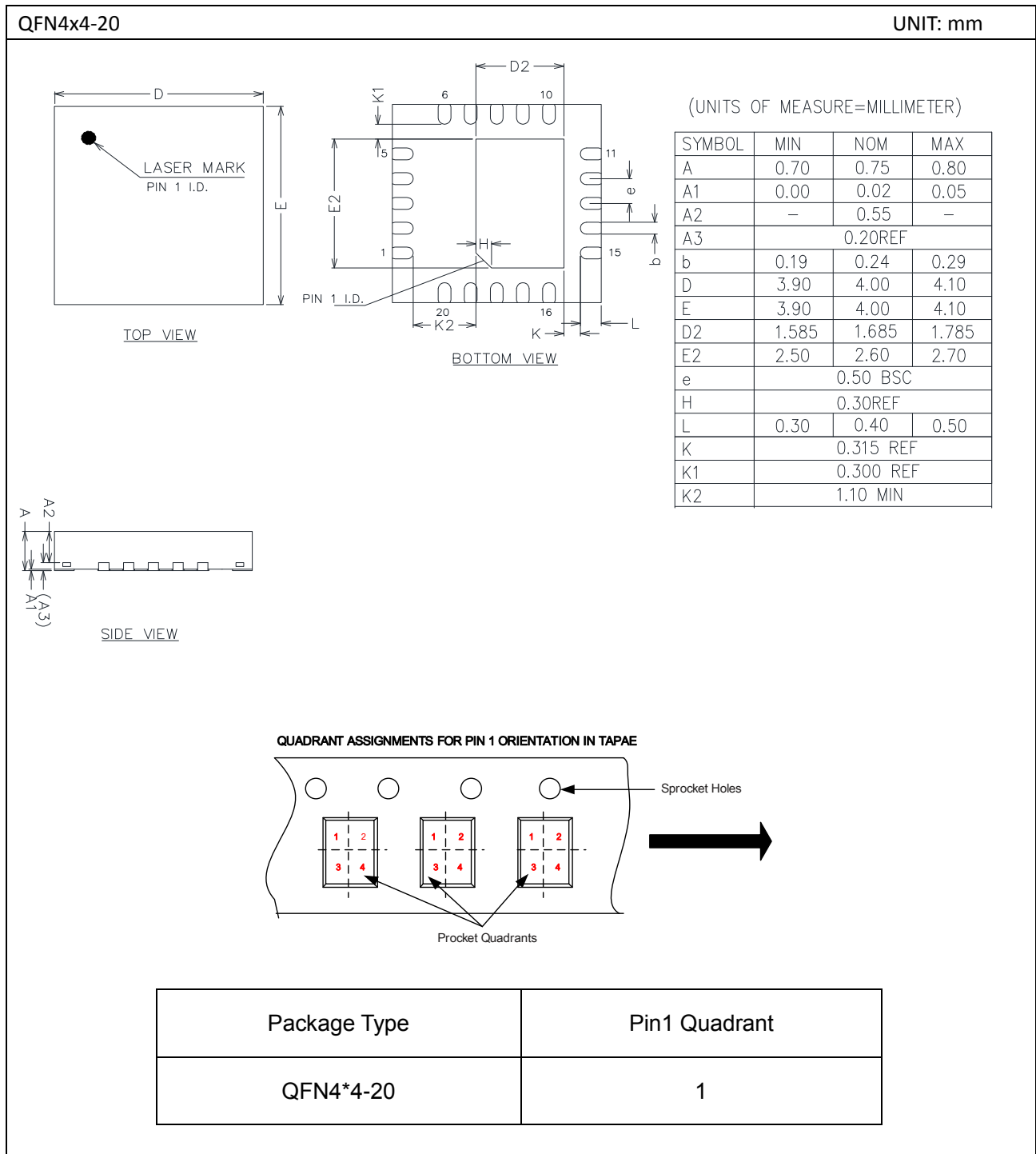
#### 4.7 Over Temperature Protection (OTP)

The JW1551 uses an external NTC resistor ( $R_{NTC}$ ) tied to the OTP pin to program a thermal shutdown temperature near the hotspot of the converter. If the OTP voltage stays lower than the NTC shut-down threshold ( $V_{NTCTH1}$ ), an OTP fault event is triggered, and  $V_{NTCTH1}$  is increased to the NTC recovery threshold ( $V_{NTCTH2}$ ). The JW1551 resumes operation when the OTP voltage stays higher than  $V_{NTCTH2}$ .

#### 4.8 Thermal Shutdown

When the junction temperature of JW1551 exceeds  $T_{SD}$ , the controller shuts down. The JW1551 resumes operation when the temperature drops below  $T_{SD} - T_{HYS}$ .

PACKAGE OUTLINE



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