JW77216

60V, 10mΩ Synchronous Rectifier

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

JW®77216 is a synchronous rectifier, used for the secondary side rectification of isolation topologies, such as Active Clamp Flyback and CCM/QR/DCM Flyback. JW77216 is able to significantly improve the efficiency comparing with the conventional Diode rectifier.

When JW77216 senses V_{ds} of MOSFET less than -140mV, it turns on the internal MOSFET. Once the V_{ds} is greater than -3mV, JW77216 turns off the internal MOSFET.

JW77216 supports multiple operation modes, such as DCM, CrCM, CCM and Quasi-Resonant. By implementing the Joulwatt proprietary technology, JW77216 is able to handle CCM operation.

JW77216 is available in SOP-8 package.

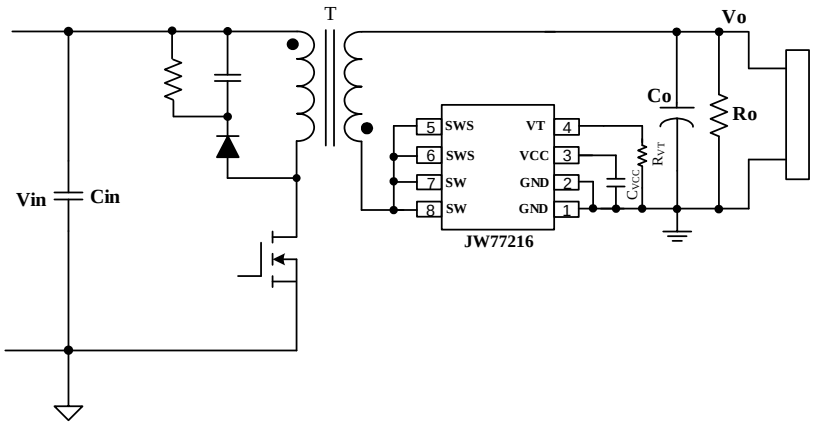
FEATURES

- Supports Active Clamp Flyback, DCM, Quasi-Resonant, and CCM Flyback
- Support High-side and Low-side Rectification
- Output Voltage Directly Supply VCC
- Low Quiescent Current
- Fast Driver Capability for CCM Operation
- SOP-8 Package

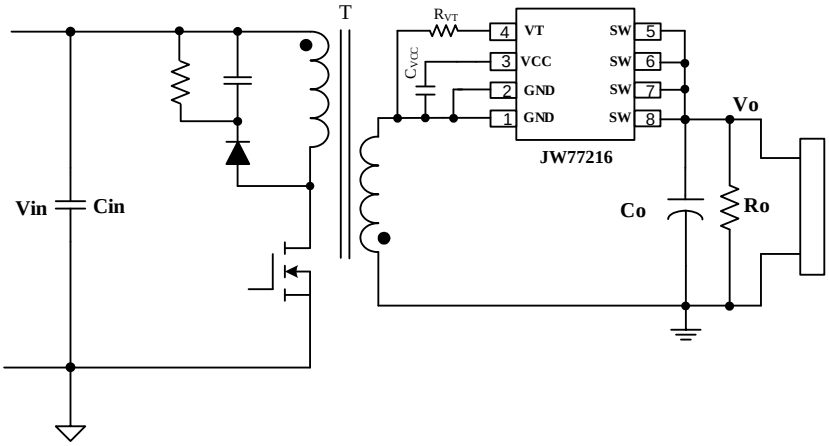
APPLICATIONS

- Active Clamp Flyback and Flyback Converters
- Adaptor
- LCD and PDP TV

TYPICAL APPLICATION



JW77216 Typical Application for Low-side



JW77216 Typical Application for High-side.

ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JW77216SOPB#TR	SOP8	JW77216 YW□□□□□	Green

Notes:

1) JW□□□#TR
- Tape and Reel (If TR is not shown, it means Tube)
- Package Code
- Part No.

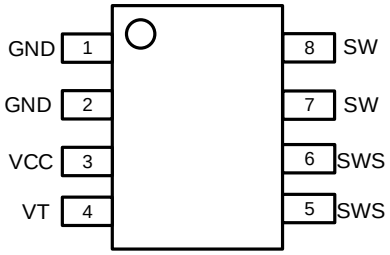
2) Line1: JW □□□□
- Product code
- Joulwatt LOGO

Line2: YW □□□□□
- Lot number
- Week code
- Year code

3) All Joulwatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION

TOP VIEW



SOP-8

ABSOLUTE MAXIMUM RATING[1)]

SW PIN .....-1 to 140V
VO PIN .....-0.3 to 28V
VCC PIN.....-0.3 to 8.7V
VT PIN..... ....-0.3 to 7V
Junction Temperature [2) 3)].....150ºC
Lead Temperature ….....260ºC
Storage Temperature….....-65ºC to150ºC
Continuous Power Dissipation(T_A=+25℃)[4)] SOP-8….....….....1.04W
ESD Susceptibility (Human Body Model) 2kV
MSL (Moisture-Sensitive Level) ..... MSL 3

RECOMMENDED OPERATING CONDITIONS

SW Pin.....4.7V to 48V
VT Pin.....0V to 5V
VCC PIN.....4V to 8.5V
Operation Junction Temperature..... -40ºC to 125ºC

THERMAL PERFORMANCE[5)]

	θ_{JA}	θ_{Jc}
SOP-8	120	60ºC/W

Note：

1) Exceeding these ratings may damage the device. These stress rating do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$.

5) Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

TA = 25ºC, unless otherwise stated

Item	Symbol	Condition	Min.	Typ.	Max.	Units
VCC Section						
VCC Voltage	VCC	SW=40V, VCC=2.2uF		8		V
VCC Startup Voltage	$V_{CC\_Startup}$	VCC Rising		4.5		V
VCC Startup Voltage Hysteresis				0.5		V
Operation Current (GT On)	I_{VCC}	GT=5nF,VCC=2.2uF		0.9		mA
Quiescent Current	I_q	VCC=4.5V, VCC=2.2uF		110		uA
SW and VO Section						
Internal MOS Turn on Threshold	V_{MOS_ON}			-140		mV
Internal MOS Turn off Threshold	V_{MOS_OFF}			-3		mV
Internal MOS Minimum on Time	T_{MIN_ON}			1.1		uS
Turn-on Total Delay	T_{DON}	6)		50		nS
Turn-off Total Delay	T_{DOF}	6)		20		nS
VCC Charge Current	I_{SW_CHG}	SW=40V, VCC=6V		85		mA
Internal MOSFET Section						
Internal MOSFET Rdson	Rdson	VGT=10V		10		mΩ
Breakdown Voltage	$B_{(BR)DSS}$		60			V

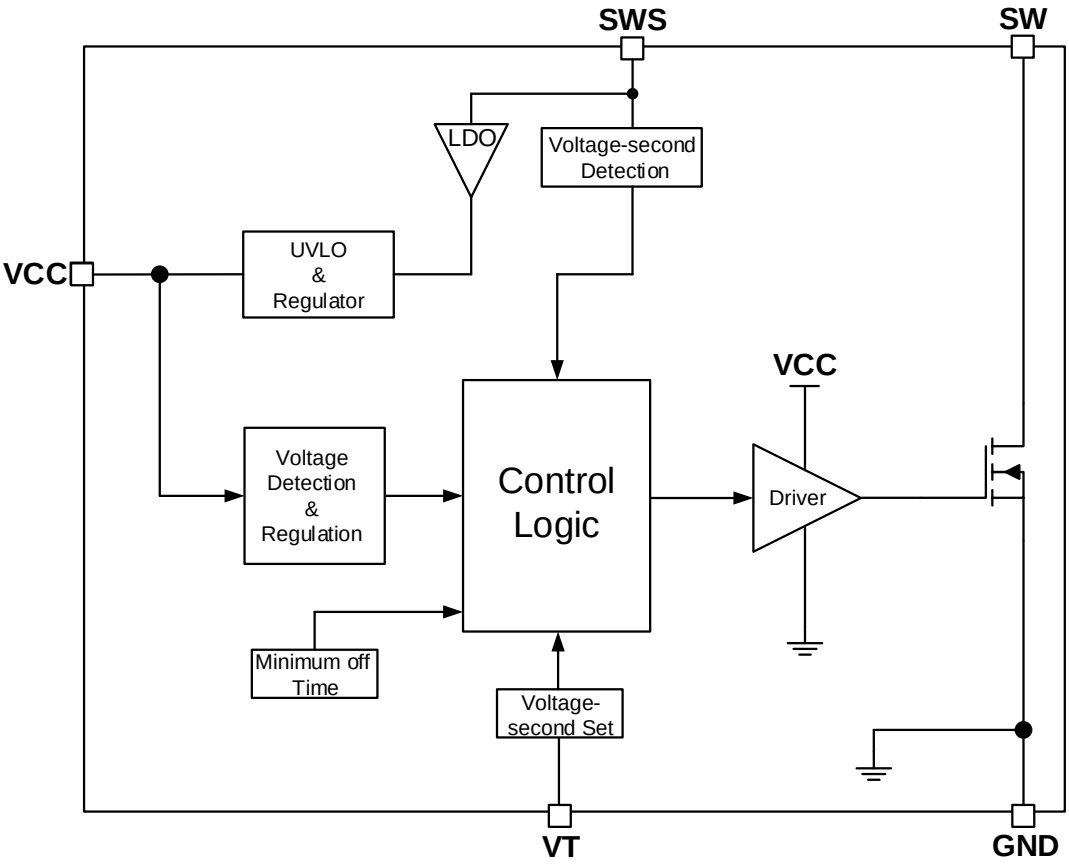
Note:

6) Guaranteed by design.

PIN DESCRIPTION

Pin	Name	Description
1,2	GND	Ground.
3	VCC	Power supply. Bypass a Capacitor Between VCC and GND.
4	VT	Set the voltage-second product.
5,6	SWS	Internal Power MOSFET Drain Voltage Sensing. Charging to VCC.
7,8	SW	Internal Power MOSFET Drain.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Operation

JW77216 is a synchronous rectifier combined with internal MOSFET can replace the Schottky Barrier Diode. It supports all operations, such as DCM, CrCM, (Quasi-Resonant) and CCM when adopted in Active Clamp Flyback and Flyback converters.

Startup

During the startup period, when the VCC is charged up by the two internal LDOs connected to SW and VO pin respectively.

A capacitor between VCC and GND is required to store the energy and supply to IC during the SR turn-on period.

Once the VCC voltage exceeds $V_{CC\_Startup}$, the JW77216 exits the UVLO. If VCC is lower than V_{CC_UVLO} ($V_{CC\_Startup}$-0.5V), the internal MOSFET is turned off. The current flows though body diode before the VCC reaches to the startup voltage $V_{cc\_startup}$.

Under-Voltage Lockout (UVLO)

When the VCC is below UVLO($V_{CC\_Startup}$-0.5V) threshold, the internal MOSFET is turned off and pulled low internally. Once the VCC exceeds the startup voltage Vcc_startup, the parts is activated again.

Turn On Phase

There are two conditions for the JW77216 to turn on the internal MOSFET, i.e. Vsw, voltage-second value on SW pin when primary side switch is on, and the turn on phase is shown in Figure. 1.

1) Vsw: when the synchronous MOEFET is conducting, current flows through the body diode of MOSFET, which generates a negative voltage V_{SW} across it. When V_{SW} is lower than V_{MOS_ON}, the part will pull the gate high to turn on the synchronous MOSFET after turn on delay time T_{DON} if the other condition is met.

2) Volt-second of SW: in DCM and QR operation, there are parasitic oscillations. In some applications, the drain resonant voltage may fall below the SR turn on threshold, especially for the first couple rings. SR could be falsely turned on, which may cause shoot through issue and result in high power loss. The volt-second value of SW pin can be used to distinguish the parasitic ring from normal primary side switch on. The threshold can be set by the resistance at VT pin. The curve is shown in Figure. 2.

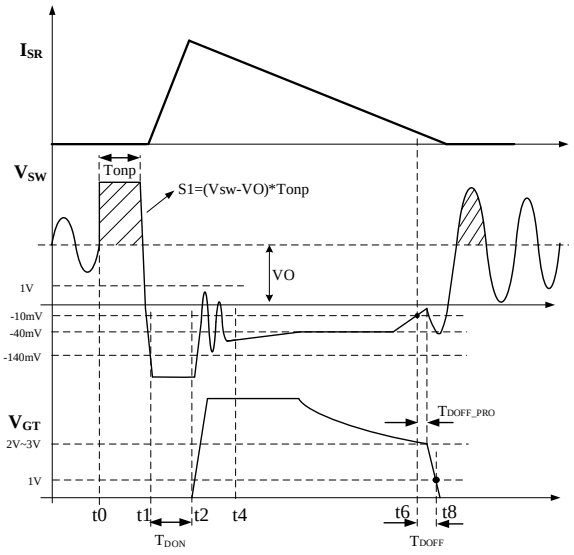


Figure. 1 Turn on delay and turn off delay

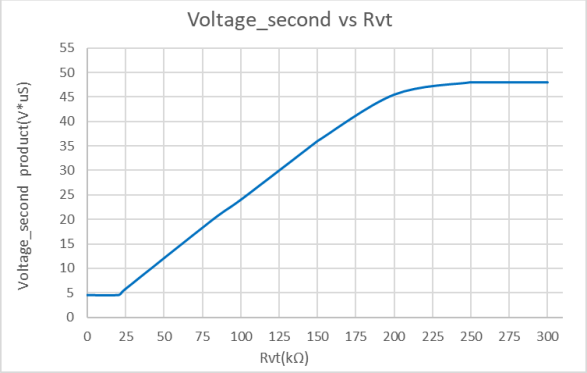


Figure-2 Volt-second value vs. VT resistance

Minimum On Time (MOT)

When the synchronous MOSFET is turn on, there is a minimum on time for the SR. The V_{SW} voltage may have a parasitic ring when the synchronous MOSFET turns on. So, a minimum on time (MOT) is very important to avoid the MOSFET turn off threshold is false triggered. Minimum on time is about 1.1us.

Conducting Phase

When the synchronous MOSFET is turned on, the drain source voltage V_{SW} it is determined by its on resistance and the current through it. The part adjusts the gate voltage and regulates the Vsw to the internal threshold (typical -40mV) after the synchronous MOSFET turn on. When the V_{SW} is lower than -40mV, the gate keeps its maximum voltage. And the synchronous MOSFET is fully on.

The V_{SW} rises when the current follow through the MOSFET decreases. The gate voltage will be decreased to increase its on resistance and regulate the V_{SW} around -40mV.

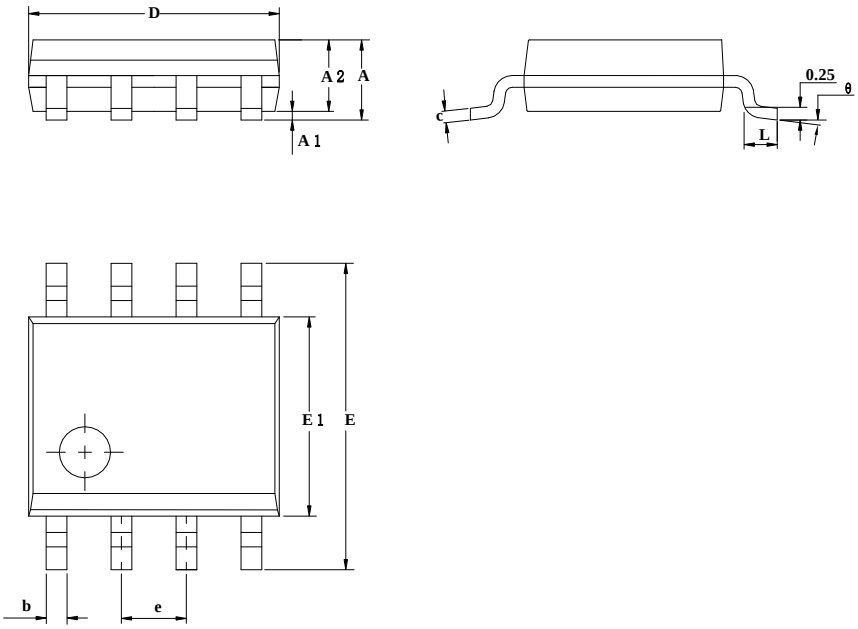
It should be noted that the typical regulation threshold (typical -40mV) during MOSFET on time is not fixed, it can be internally changed to ensure the proper operation under CCM mode.

Turn Off Phase

After synchronous MOSFET conducting, once the voltage V_{SW} touches the MOSFET turn off threshold, the gate is pulled to low after a turn off delay time T_{DOFF}. A 365nS blanking time is necessary to avoid error trigger. The banking time is reset once Vsw rises above +2.5V.

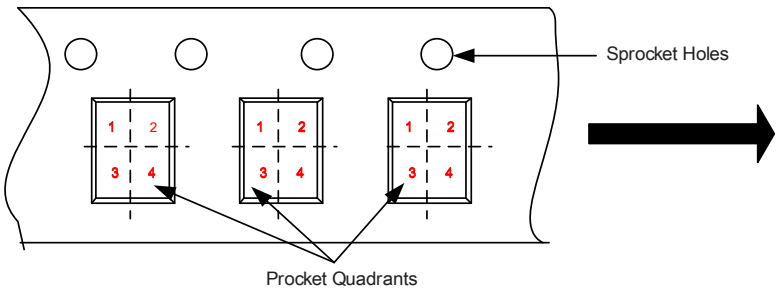
PACKAGE OUTLINE

SOP8 Unit: mm



Symbol	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	0.15	0.25
A2	1.25	1.40	1.65
b	0.32	0.42	0.52
c	0.10	0.20	0.30
D	4.50	5.00	5.50
E	5.50	6.00	6.50
E1	3.50	3.90	4.30
e	1.27TYP		
L	0.40	—	1.27
θ	0°	—	8°

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
SOP8	1

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