FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC138 are high-speed Si-gate CMOS devices and are pin compatible with low power Scotty TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC138 decoders accept three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provide 8 mutually exclusive active LOW outputs (Y_0 to Y_7).

The “138” features three enable inputs: two active LOW (E_1 and E_2) and one active HIGH (E_3). Every output will be HIGH unless E_1 and E_2 are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the “138” to a 1-of-32 (5 lines to 32 lines) decoder with just four “138” ICs and one inverter.

The ”138” can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The ”138” is identical to the “238” but has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CPMDITIONS	TYPICAL		UNIT
			HC	HCT	
tPHL/ tPLH tPHL/ tPLH	Propagation delay An to Yn E3 to Yn En to Yn	CL=15pF; Vcc=5V	12 14	17 19	ns ns
CI	Input capacitance		3.5	3.5	pF
C_{PD}	Power dissipation capacitance per package	Notes 1 and 2	67	67	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}

   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See

PIN DESCRIPTION

PIN NO	SYMBOL	NAME AND FUNCTION
1, 2, 3	A0 to A2	Address inputs
4, 5	E1, E2	Enable inputs (active LOW)
6	E3	Enable input (active HIGH)
8	GND	Ground (0V)
15, 14, 13, 12, 11, 10, 9, 7	Yo to Y7	Outputs (active LOW)
16	Vcc	Positive supply voltage

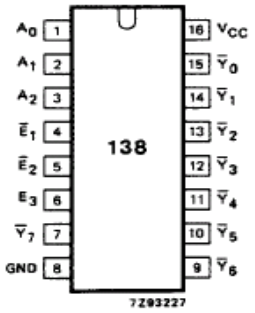


Fig.1 Pin configuration.

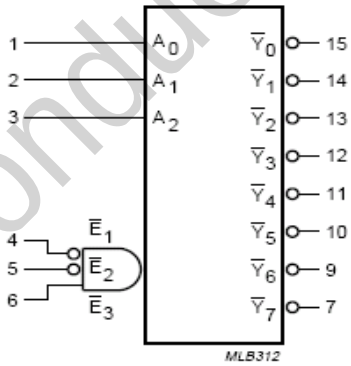


Fig.2 Logic symbol.

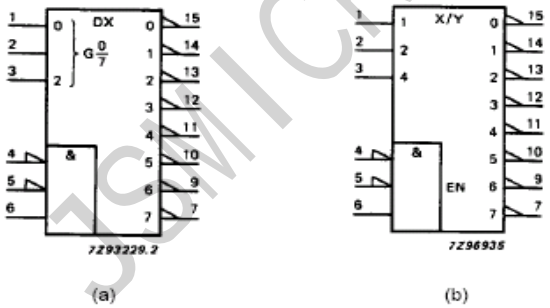


Fig.3 IEC logic symbol.

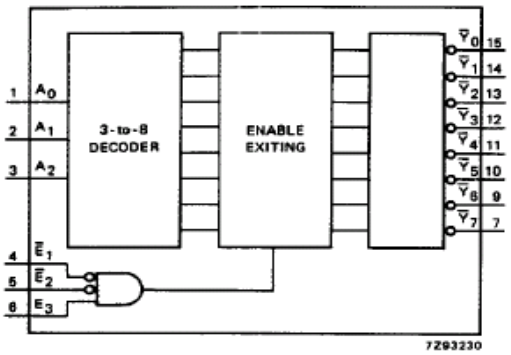


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
E1	E2	E3	A0	A1	A2	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care

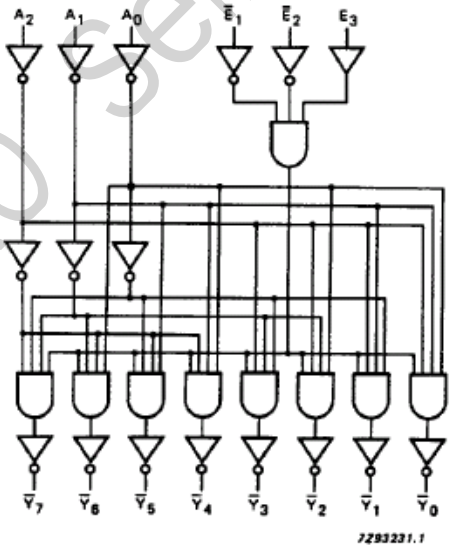


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see

Output capability: standard

Icc category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 Pf

SYMBOL	PARAMETER	Tamb(℃)							UNIT	TEST CONDITIONS	
		74HC									
		+25			-40 to +85		-40 to +125			Vcc (v)	WAVEFORMS
		min	typ	max	min	max	min	max			
tPHL/ tPLH	Propagation delay An to Yn		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
tPHL/ tPLH	Propagation delay E3 to Yn		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
tPHL/ tPLH	Propagation delay En to Yn		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
tTHL/ tTLH	Output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see

Output capability: standard

Icc category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔIcc) for a unit load of 1 is given in the family specifications. To determine ΔIcc per input, multiply this value by the unit load coefficient shown in the table below.

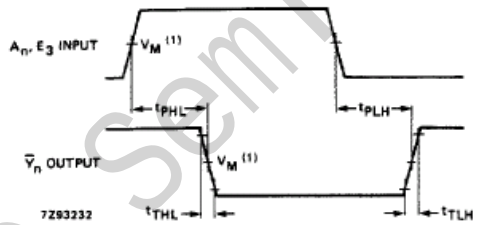
INPUT	UNIT LOAD COEFFICIENT
An	1.50
En	1.25
E3	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

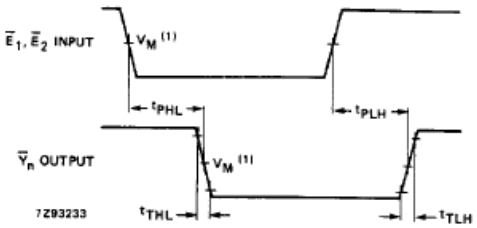
SYMBOL	PARAMETER	Tamb(℃)							UNIT	TEST CONDITIONS	
		74HCT									
		+25			-40 to +85		-40 to +125			Vcc (v)	WAVEFORMS
		min	typ	max	min	max	min	max			
tPHL/ tPLH	Propagation delay An to Yn		20	35		44		53	ns	4.5	Fig. 6
tPHL/ tPLH	Propagation delay E3 to Yn		18	40		50		60	ns	4.5	Fig. 6
tPHL/ tPLH	Propagation delay En to Yn		19	40		50		60	ns	4.5	Fig. 7
tTHL/ tTLH	Output transition time		7	15		19		22	ns	4.5	Fig. 6 and 7

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the address input (A_n) and enable input (E_3) to output ($\overline{Y}_n$) propagation delays and the output transition times.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the enable input ($\overline{E}_n$) to output ($\overline{Y}_n$) propagation delays and the output transition times.

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