

■ DESCRIPTION

The FDS4435BZ is the P-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology..

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching

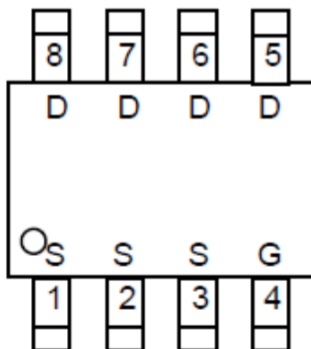
■ FEATURE

- ◆ -30V/-9.7A, $R_{DS(ON)}=19.5m\Omega$ (typ.)@ $V_{GS}=-10V$
- ◆ -30V/-7.0A, $R_{DS(ON)}=23.5m\Omega$ (typ.)@ $V_{GS}=-4.5V$
- ◆ Super high design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and Maximum DC current capability
- ◆ Full RoHS compliance
- ◆ SOP8 package design

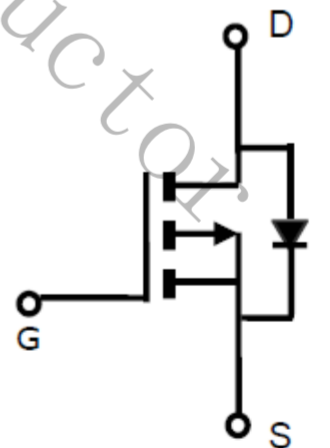
■ APPLICATIONS

- ◆ High Frequency Point-of-Load Synchronous
- ◆ Newworking DC-DC Power System
- ◆ Load Switch

■ PIN CONFIGURATION



TOP VIEW
SOP-8



P-Channel

■ ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

Symbol	Parameter	Typical	Unit
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current ($T_A=25^\circ\text{C}$)	$V_{GS}=10\text{V}$ -9.7	A
I_{DM}	Pulsed Drain Current	-40	A
I_S	Continuous Source Current (Diode Conduction)	-2.1	A
P_D	Power Dissipation	$T_A=25^\circ\text{C}$	3.0
		$T_A=70^\circ\text{C}$	2.1
T_J	Operation Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55~+150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	85	$^\circ\text{C/W}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress rating only and functional device operation is not implied

ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.2	-1.4	-2.7	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-24V, V_{GS}=0$			-1	uA
		$V_{DS}=-24V, V_{GS}=0$ $T_J=55^\circ\text{C}$			-5	
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS}=-10V, I_D=-9.7A$		19.5	28	m Ω
		$V_{GS}=-4.5V, I_D=-7A$		23	35	
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	$I_S=-1.0A, V_{GS}=0V$		-0.7	-1.0	V
Dynamic Parameters						
Q_g	Total Gate Charge	$V_{DS}=-15V$ $V_{GS}=-15V$ $V_{GS}=10V$		33.82	43.97	nC
Q_{gs}	Gate-Source Charge			4.93	6.41	
Q_{gd}	Gate-Drain Charge			5.2	6.76	
C_{iss}	Input Capacitance	$V_{DS}=-15V$ $V_{GS}=0V$ $f=1\text{MHz}$		1573	1900	pF
C_{oss}	Output Capacitance			319		
C_{rss}	Reverse Transfer Capacitance			211	295	
$T_{d(on)}$	Turn-On Time	$V_{DS}=-15V$ $I_D=-10A$		15.44	30.88	nS
T_r				5.04	10.08	
$T_{d(off)}$	Turn-Off Time	$V_{GEN}=-10V$ $R_G=6\Omega$		71.04	142.08	
T_f				16.8	33.6	

Note: 1. Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

2. Static parameters are based on package level with recommended wire bonding

■ **TYPICAL CHARACTERISTICS (25°C Unless Note)**

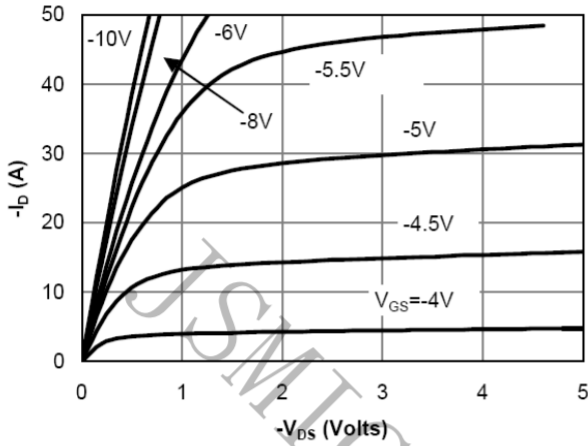


Fig 1: On-Region Characteristics

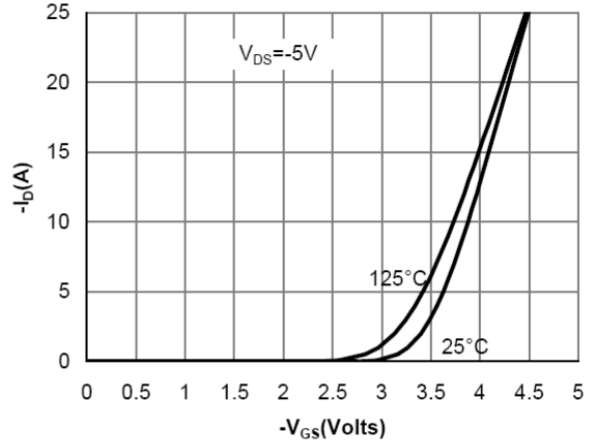


Figure 2: Transfer Characteristics

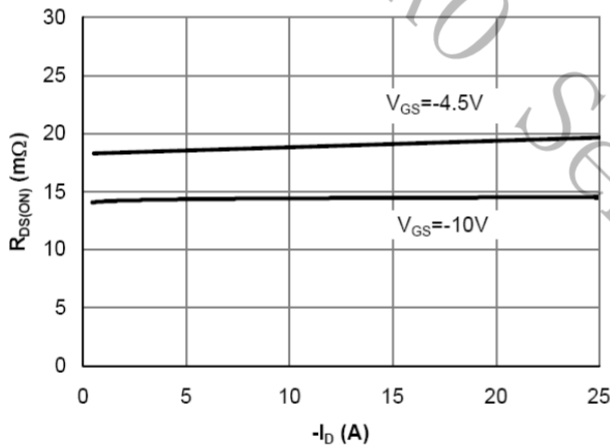


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

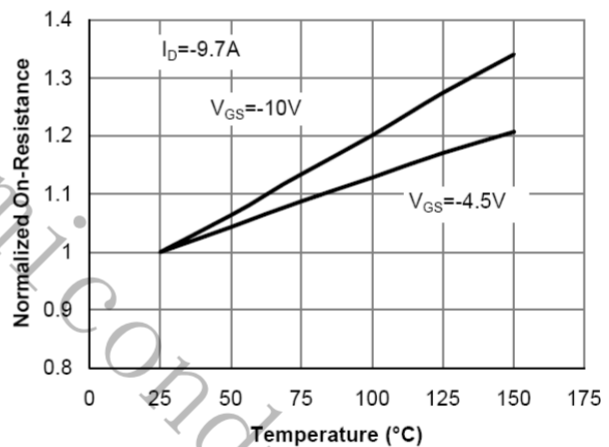


Figure 4: On-Resistance vs. Junction Temperature

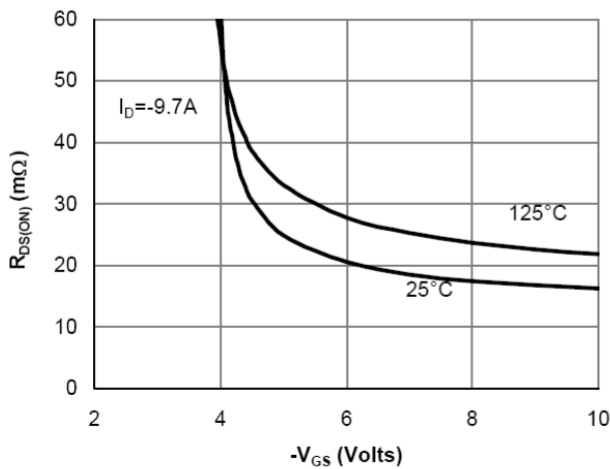


Figure 5: On-Resistance vs. Gate-Source Voltage

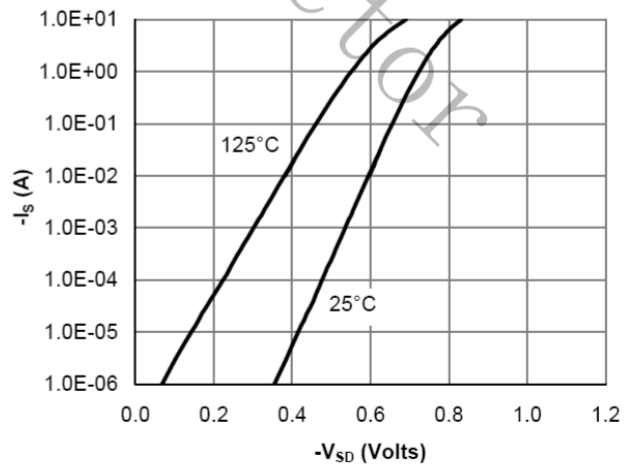


Figure 6: Body-Diode Characteristics

■ **TYPICAL CHARACTERISTICS** (continuous)

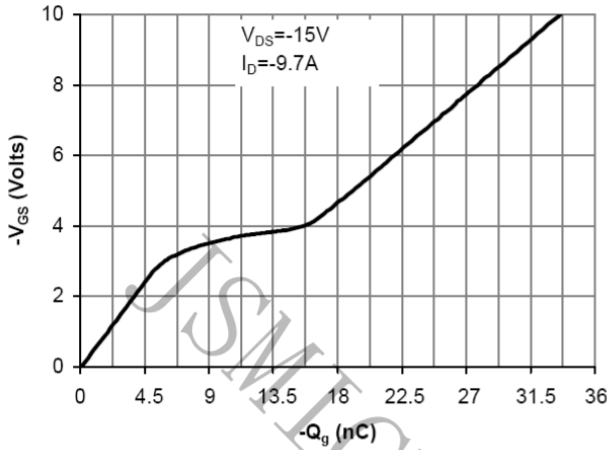


Figure 7: Gate-Charge Characteristics

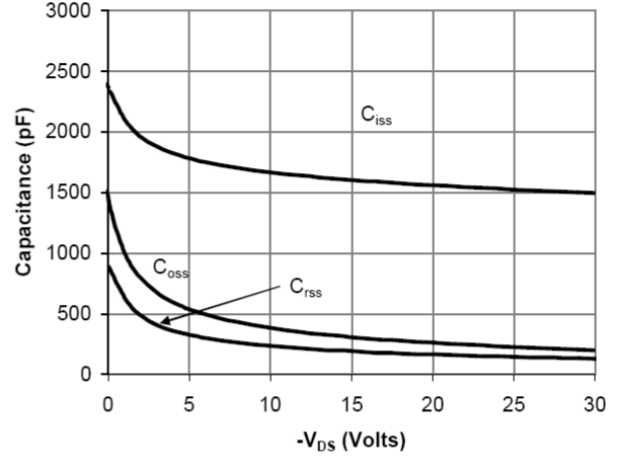


Figure 8: Capacitance Characteristics

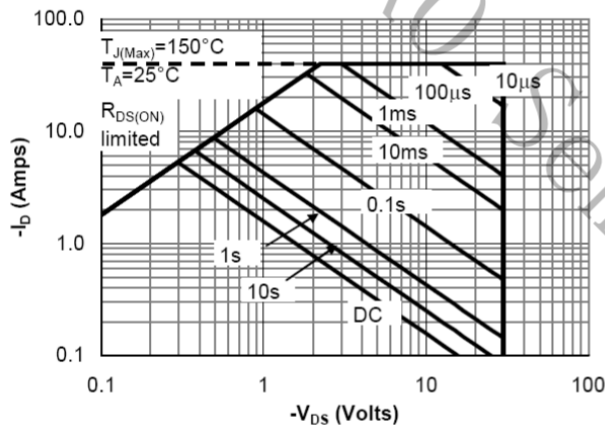


Figure 9: Maximum Forward Biased Safe Operating Area

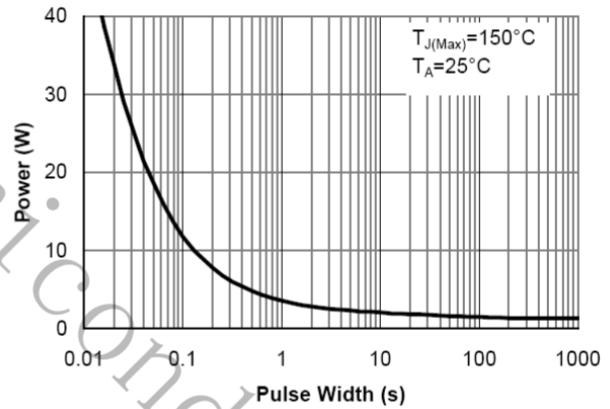


Figure 10: Single Pulse Power Rating Junction-to-Ambient

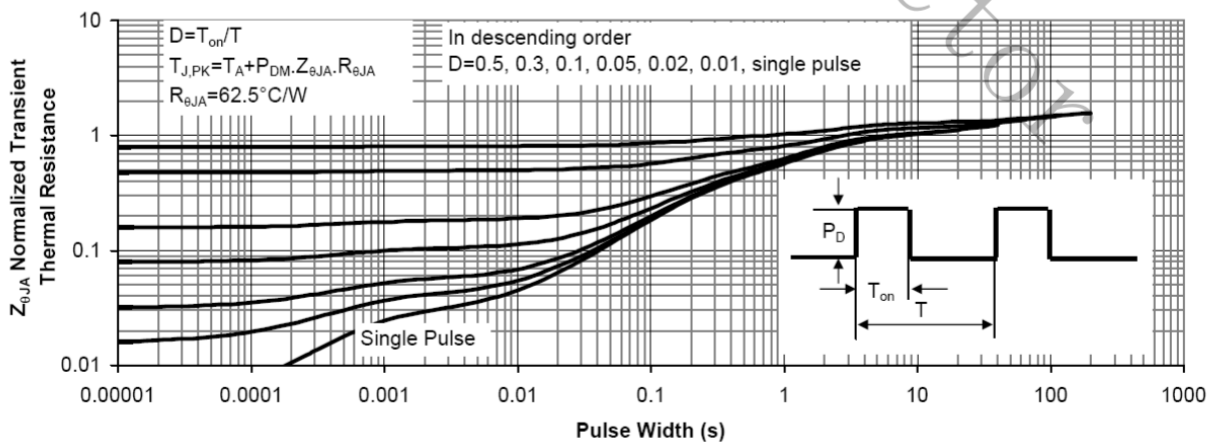
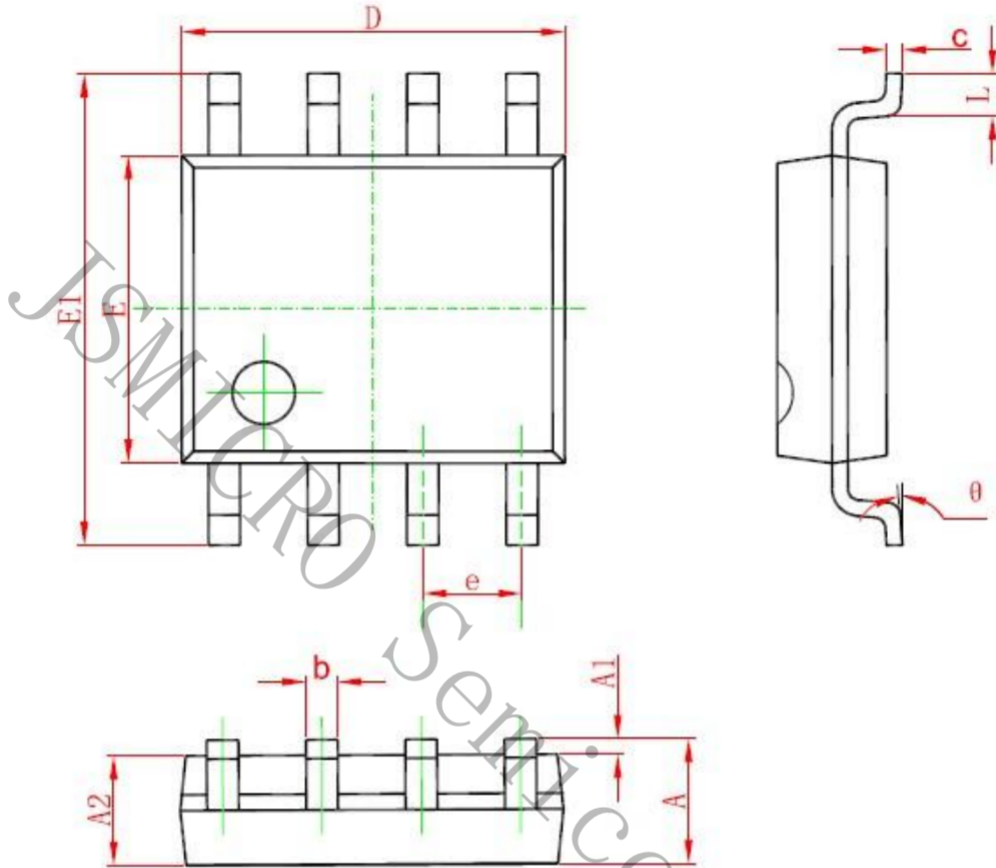


Figure 11: Normalized Maximum Transient Thermal Impedance

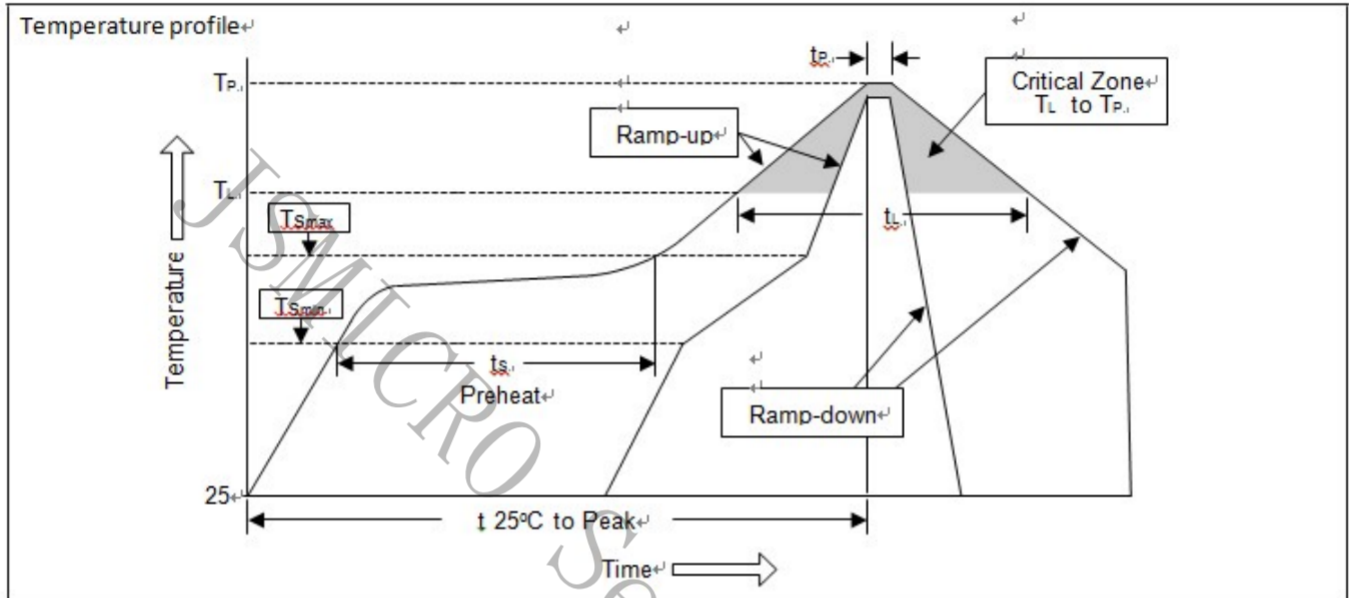
■ SOP8 PACKAGE OUTLINE DIMENSIONS


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°

■ SOLDERING METHODS FOR UNIVERCHIP

Storage environment Temperature=10°C~35°C Humidity=65%±15%

Reflow soldering of surface mount device



Profile Feature	Sn-Pb Eutectic Assembly	Pb free Assembly
Average ramp-up rate (T_L to T_P)	<3°C/sec	<3°C/sec
Preheat		
-Temperature Min ($T_{s_{min}}$)	100°C	150°C
-Temperature Max ($T_{s_{max}}$)	150°C	200°C
-Time (min to max) (t_s)	60~120 sec	60~180 sec
$T_{s_{max}}$ to T_L		
-Ramp-up Rate	<3°C/sec	<3°C/sec
Time maintained above		
-Temperature (T_L)	183°C	217°C
-Time (t_L)	60~150 sec	60~150 sec
Peak Temperature (T_P)	240°C+0/-5°C	260°C+0/-5°C
Time within 5°C of actual Peak Temperature (t_p)	10~30 sec	20~40 sec
Ramp-down Rate	<6°C/sec	<6°C/sec
Time 25°C to Peak Temperature	<6 minutes	<6 minutes

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