

30V N-Channel MOSFET
N-Channel Enhancement Mode Power MOSFET
General Features

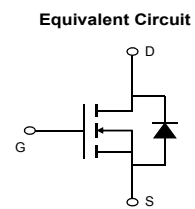
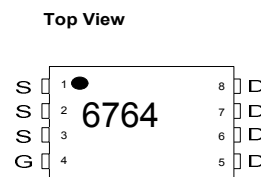
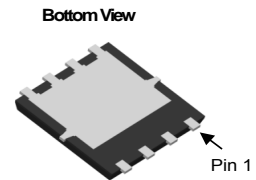
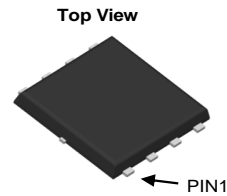
V_{DS}	30V
I_D (at $V_{GS}=10V$)	85A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 4.00m Ω
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 5.00m Ω

100% UIS Tested
 100% Rg Tested

- Trench Power α MOS Technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

Applications

- DC/DC Converters in Computing
- Isolated DC/DC Converters in Telecom and Industrial

PDFN5X6-8L


Orderable Part Number		Package Type	Form	Minimum Order Quantity	
JSM6764		DFN 5x6	Tape&Reel	3000	
Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted					
Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		V_{DS}	30	V	
Gate-Source Voltage		V_{GS}	± 12	V	
Continuous Drain Current ^G	$T_C=25^\circ\text{C}$	I_D	85	A	
Pulsed Drain Current ^C		I_{DM}	190		
Continuous Drain Current	$T_A=25^\circ\text{C}$	I_{DSM}	37	A	
Avalanche Current ^C		I_{AS}	42	A	
Avalanche energy	$L=0.05\text{mH}$ ^C	E_{AS}	44	mJ	
V_{DS} Spike	10 μs	V_{SPIKE}	36	V	
Power Dissipation ^B	$T_C=25^\circ\text{C}$	P_D	42	W	
Power Dissipation ^A	$T_A=25^\circ\text{C}$	P_{DSM}	6.2	W	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$	
Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$t \leq 10\text{s}$	$R_{\theta JA}$	15	20	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A D}	Steady-State		40	50	$^\circ\text{C/W}$
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	2.4	3	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	ID=10mA, VGS=0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V			0.5	uA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±12V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.1	1.5	1.9	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A		3.8	4.0	mΩ
		V _{GS} =4.5V, I _D =20A		4.5	5.0	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		167		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.5	0.7	V
I _S	Maximum Body-Diode Continuous Current				30	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		2120		pF
C _{oss}	Output Capacitance			700		pF
C _{rss}	Reverse Transfer Capacitance			69		pF
R _g	Gate resistance	f=1MHz	0.9	1.8	2.7	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A		37		nC
Q _{g(4.5V)}	Total Gate Charge			16.8		nC
Q _{gs}	Gate Source Charge			5		nC
Q _{gd}	Gate Drain Charge			4.9		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω		7		ns
t _r	Turn-On Rise Time			3.5		ns
t _{D(off)}	Turn-Off DelayTime			36		ns
t _f	Turn-Off Fall Time			6		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=500A/μs		15.5		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=500A/μs		33		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

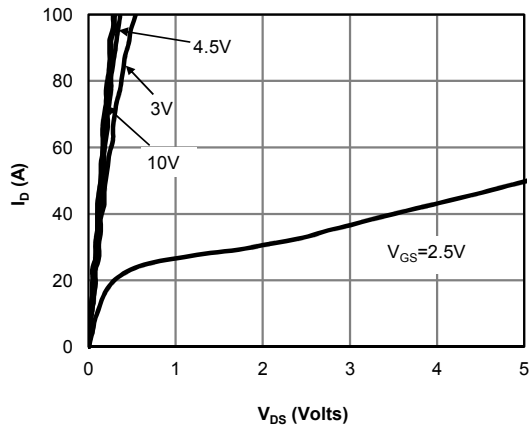
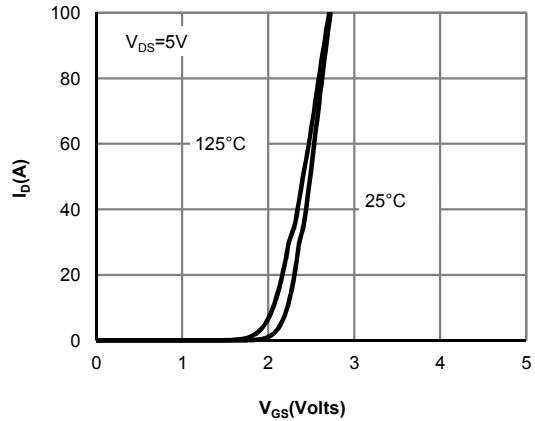
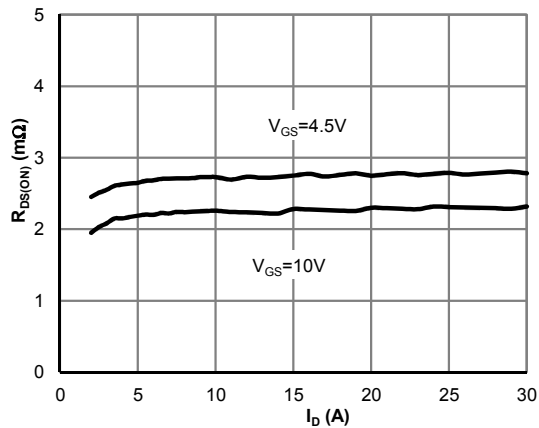
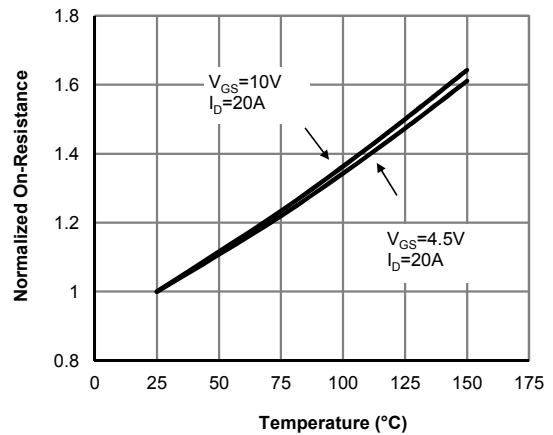
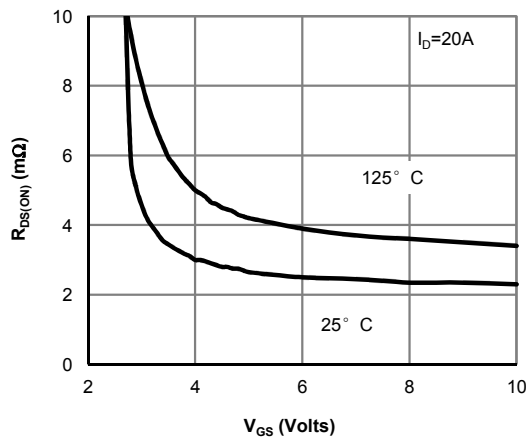
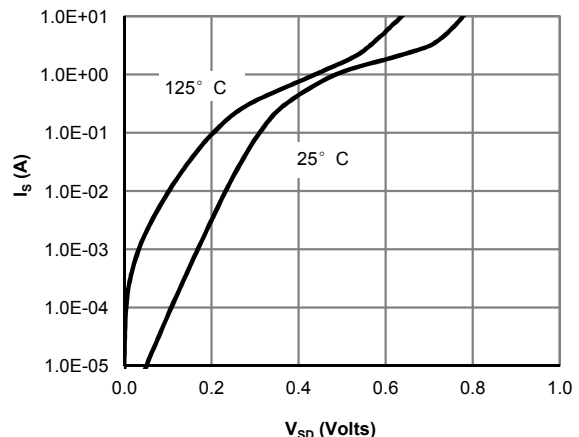
D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 1: On-Region Characteristics (Note E)

Figure 2: Transfer Characteristics (Note E)

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

Figure 4: On-Resistance vs. Junction Temperature (Note E)

Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

Figure 6: Body-Diode Characteristics (Note E)

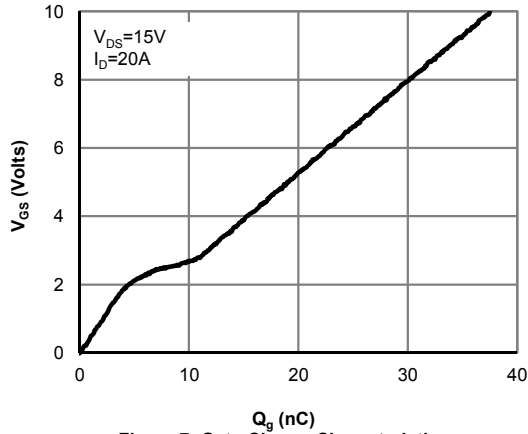
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS


Figure 7: Gate-Charge Characteristics

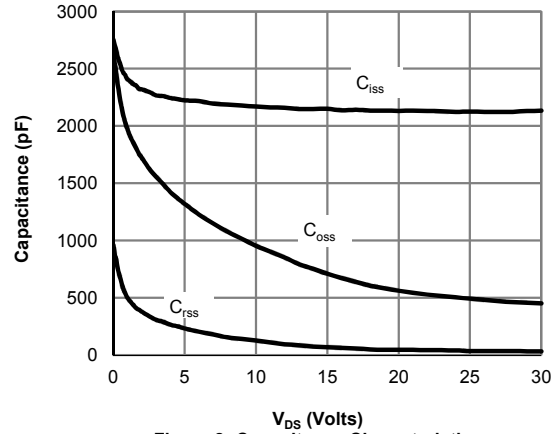


Figure 8: Capacitance Characteristics

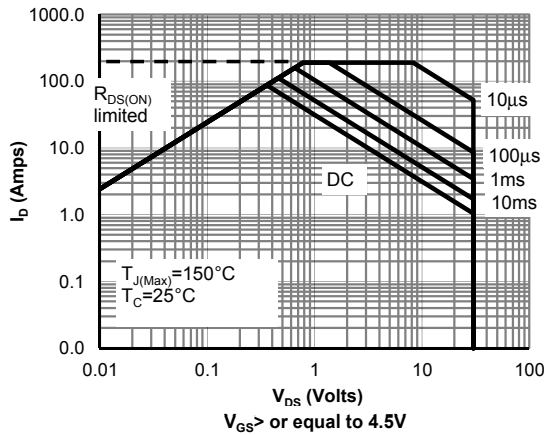


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

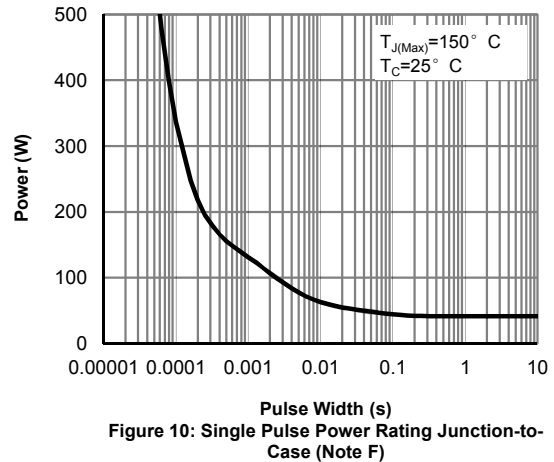


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

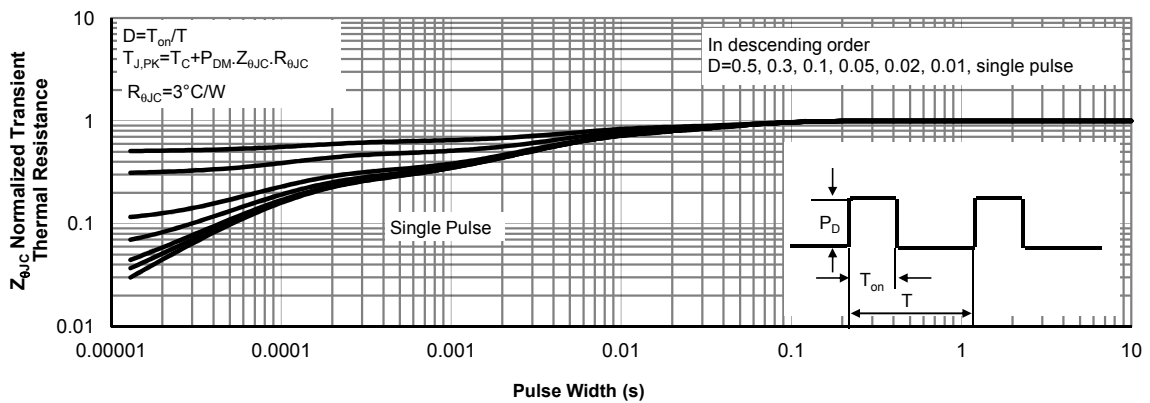


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

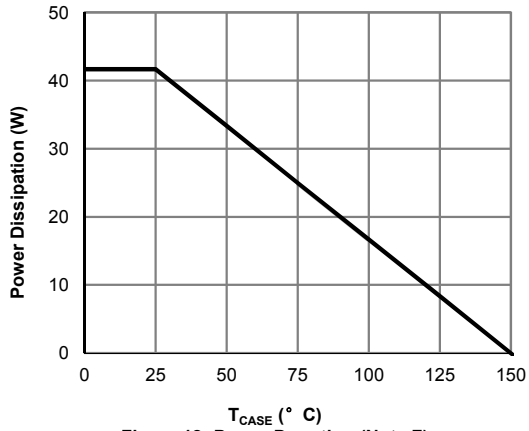
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS


Figure 12: Power De-rating (Note F)

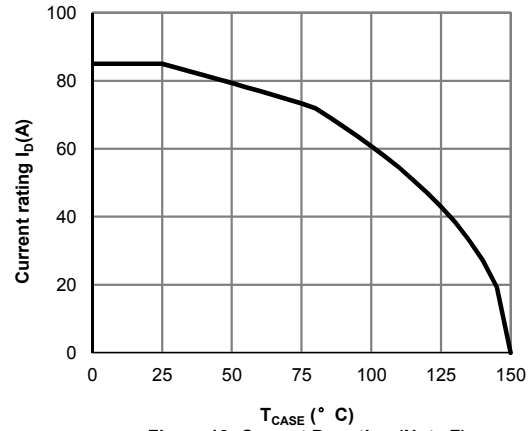


Figure 13: Current De-rating (Note F)

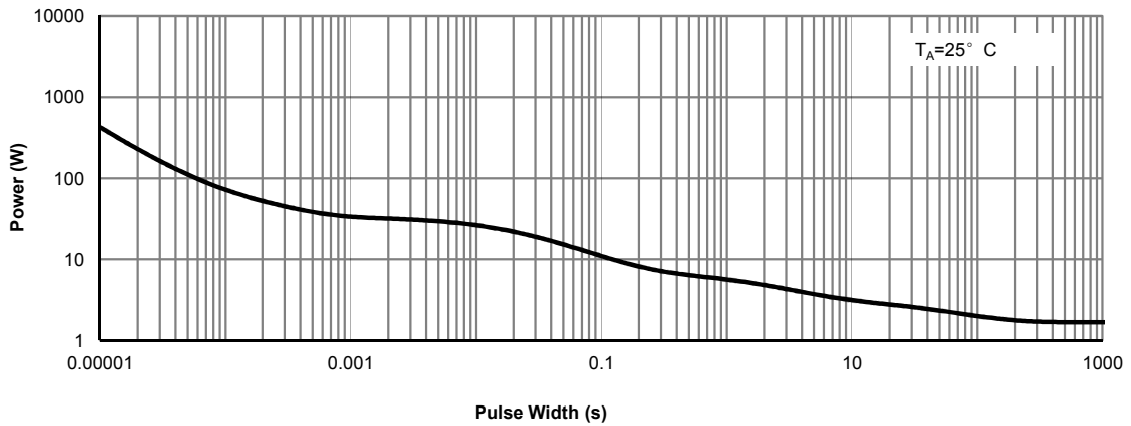


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

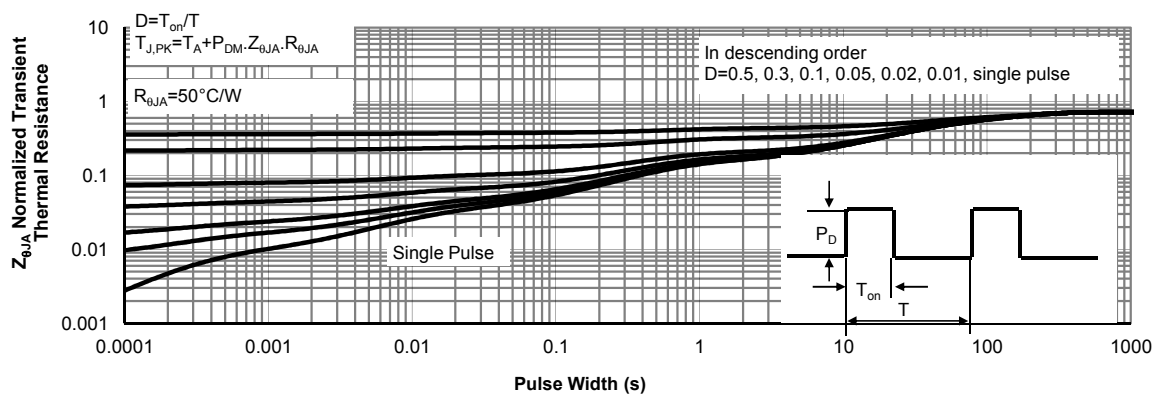
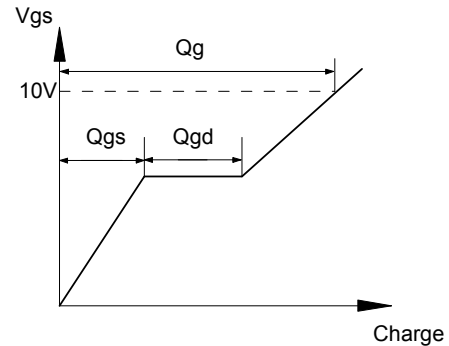
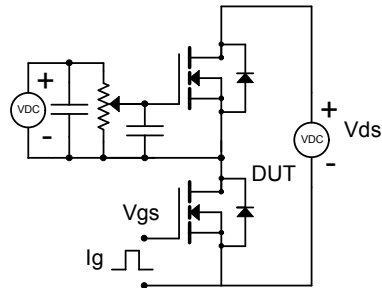
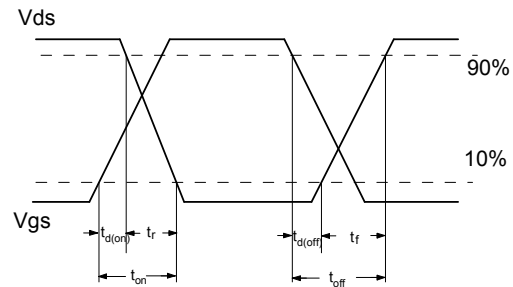
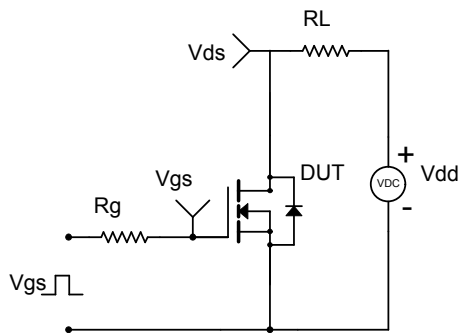
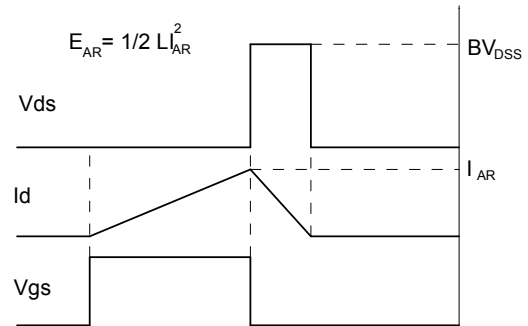
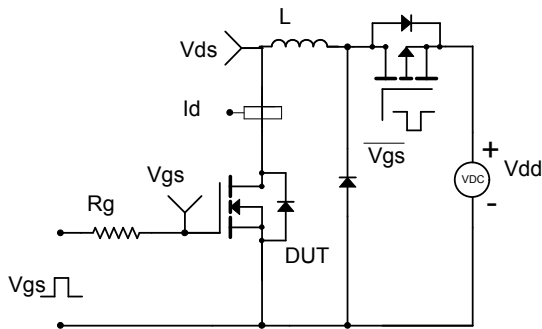
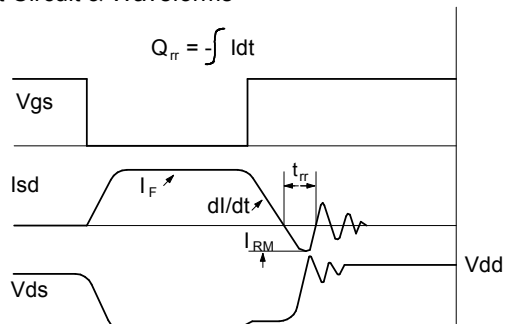
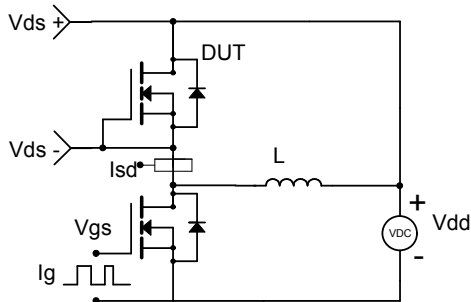
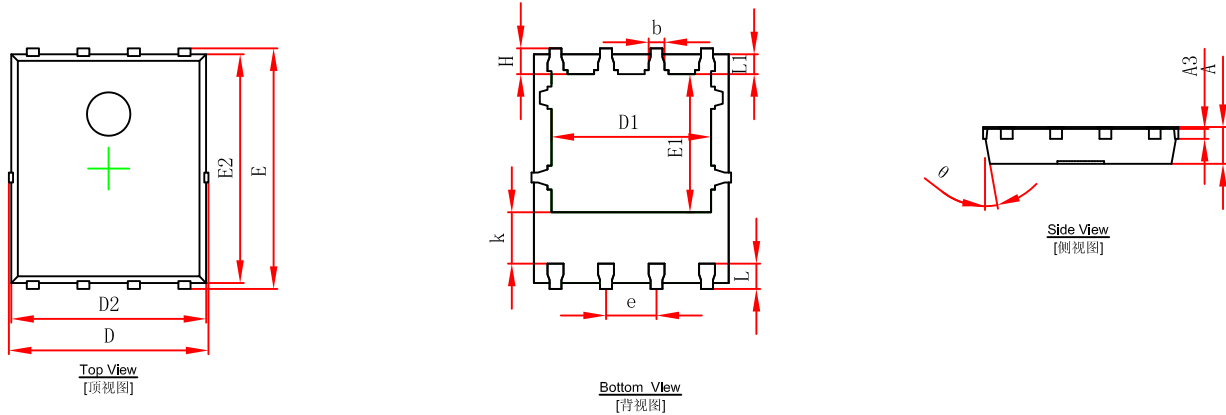
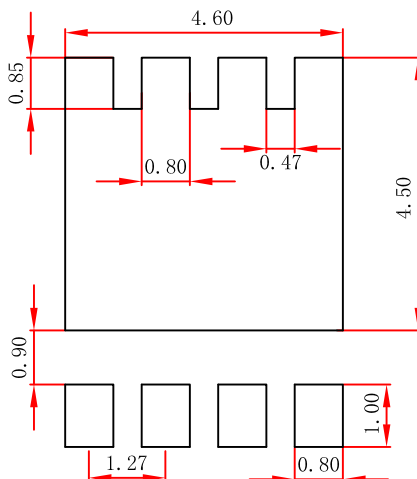


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

Diode Recovery Test Circuit & Waveforms


PDFNWB5x6-8L Package Outline Dimensions


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

PDFNWB5x6-8L Suggested Pad Layout


- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.

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