Surface Mount Multilayer Ceramic Chip Capacitors (SMD MLCCs)

KPS "L", SnPb Termination, X7R Dielectric, 10 – 250 VDC (Commercial Grade)

Overview

KEMET Power Solutions (KPS) Commercial "L" with Tin/Lead Termination stacked capacitors utilize a proprietary lead-frame technology to vertically stack one or two multilayer ceramic chip capacitors into a single compact surface mount package. The attached lead-frame mechanically isolates the capacitor's from the printed circuit board, therefore offering advanced mechanical and thermal stress performance. Isolation also addresses concerns for audible, microphonic noise that may occur when a bias voltage is applied. A two chip stack offers up to double the capacitance in the same or smaller design footprint when compared to traditional surface mount MLCC devices. Providing up to 10 mm of board flex capability, KEMET's tin/lead electroplating process is designed to meet a 5% minimum lead content and address concerns for a more robust and reliable lead containing termination system. As the bulk of the electronics industry moves towards RoHS compliance, KEMET continues to provide tin/lead terminated products for military, aerospace and industrial applications and will ensure customers have a stable and long-term source of supply. These devices provide lower ESR, ESL and higher ripple current capability when compared to other dielectric solutions.

Combined with the stability of an X7R dielectric, KEMET's KPS devices exhibit a predictable change in capacitance with respect to time and voltage and boast a minimal change in capacitance with reference to ambient temperature. Capacitance change is limited to ±15% from −55°C to +125°C.

Benefits

- Operating temperature range of −55°C to +125°C
- Reliable and robust termination system
- EIA 1210 and 2220 case sizes
- DC voltage ratings of 10 V, 16 V, 25 V, 50 V, 63 V, 100 V and 250 V
- Capacitance offerings ranging from 0.1 up to 47 µF

Ordering Information

C	2220	C	106	M	5	R	2	L	7186
Ceramic	Case Size (L" x W")	Specification/ Series	Capacitance Code (pF)	Capacitance Tolerance[1]	Rated Voltage (VDC)	Dielectric	Failure Rate/ Design	Leadframe Finish[2]	Packaging/ Grade (C-Spec)
	1210 2220	C = Standard	Two Significant Digits and Number of Zeroes	K = ±10% M = ±20%	8 = 10 4 = 16 3 = 25 5 = 50 M = 63 1 = 100 A = 250	R = X7R	1 = KPS Single Chip Stack 2 = KPS Double Chip Stack	L = SnPb (5% Pb min.)	See "Packaging C-Spec Ordering Options Table"

[1] Double chip stacks ("2" in the 13th character position of the ordering code) are only available in M (±20%) capacitance tolerance. Single chip stacks ("1" in the 13th character position of the ordering code) are available in K (±10%) or M (±20%) tolerances.

[2] Additional leadframe finish options may be available. Contact KEMET for details.

Packaging C-Spec Ordering Options Table

Packaging Type[1]	Packaging/Grade Ordering Code (C-Spec)
7" Reel (Embossed Plastic Tape)/Unmarked	7186
13" Reel (Embossed Plastic Tape)/Unmarked	7289

[1] The terms "Marked" and "Unmarked" pertain to laser marking option of capacitors. All packaging options labeled as "Unmarked" will contain capacitors that have not been laser marked. The option to laser mark is not available on these devices. For more information see "Capacitor Marking."

Benefits cont.

- Available capacitance tolerances of ±10% and ±20%
- Higher capacitance in the same footprint
- Potential board space savings
- Advanced protection against thermal and mechanical stress
- Provides up to 10mm of board flex capability
- Reduces audible, microphonic noise
- Extremely low ESR and ESL
- SnPb plated termination finish (5% Pb minimum)
- Non-polar device, minimizing installation concerns
- Tantalum and electrolytic alternative

Applications

Typical applications include smoothing circuits, DC/DC converters, power supplies (input/output filters), noise reduction (piezoelectric/mechanical), circuits with a direct battery or power source connection, critical and safety relevant circuits without (integrated) current limitation, and any application that is subject to high levels of board flexure or temperature cycling. Markets include industrial, aerospace, automotive and telecommunications.

Qualification/Certification

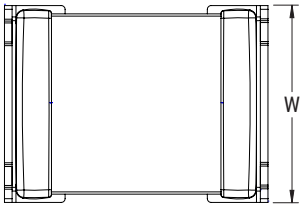
Commercial grade products are subject to internal qualification. Details regarding test methods and conditions are referenced in Table 4, Performance & Reliability.

Environmental Compliance

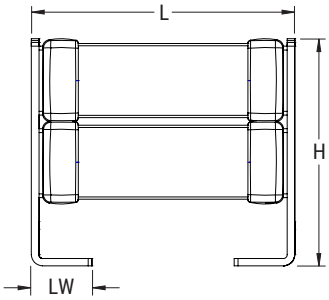
These devices do not meet RoHS criteria due to the concentration of Lead (Pb) in the termination finish.

Dimensions – Inches (Millimeters)

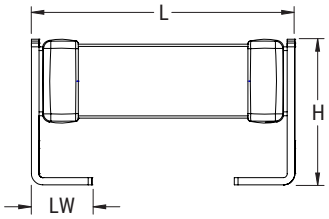
Single or Double Chip Stack



Double Chip Stack



Single Chip Stack



Number of Chips	EIA SIZE CODE	METRIC SIZE CODE	L LENGTH	W WIDTH	H HEIGHT	LW LEAD WIDTH	Mounting Technique
Single	1210	3225	3.50 (0.138) ±0.30 (0.012)	2.60 (0.102) ±0.30 (0.012)	3.35 (0.132) ±0.10 (0.004)	0.80 (0.032) ±0.15 (0.006)	Solder Reflow Only
	2220	5650	6.00 (0.236) ±0.50 (0.020)	5.00 (0.197) ±0.50 (0.020)	3.50 (0.138) ±0.30 (0.012)	1.60 (0.063) ±0.30 (0.012)	
Double	1210	3225	3.50 (0.138) ±0.30 (0.012)	2.60 (0.102) ±0.30 (0.012)	6.15 (0.242) ±0.15 (0.006)	0.80 (0.031) ±0.15 (0.006)	
	2220	5650	6.00 (0.236) ±0.50 (0.020)	5.00 (0.197) ±0.50 (0.020)	5.00 (0.197) ±0.50 (0.020)	1.60 (0.063) ±0.30 (0.012)	

Electrical Parameters/Characteristics

Item	Parameters/Characteristics
Operating Temperature Range	−55°C to +125°C
Capacitance Change with Reference to +25°C and 0 Vdc Applied (TCC)	±15%
[1]Aging Rate (Maximum % Capacitance Loss/Decade Hour)	3.0%
[2]Dielectric Withstanding Voltage (DWV)	250% of rated voltage (5 ±1 seconds and charge/discharge not exceeding 50 mA)
[3]Dissipation Factor (DF) Maximum Limit at 25°C	5% (10 V), 3.5% (16 V and 25 V) and 2.5%(50 V to 250 V)
[4]Insulation Resistance (IR) Minimum Limit at 25°C	See Insulation Resistance Limit Table (Rated voltage applied for 120 ±5 seconds at 25°C)

[1] Regarding Aging Rate: Capacitance measurements (including tolerance) are indexed to a referee time of 48 or 1,000 hours. Please refer to a part number specific datasheet for referee time details.

[2] DWV is the voltage a capacitor can withstand (survive) for a short period of time. It exceeds the nominal and continuous working voltage of the capacitor.

[3] Capacitance and dissipation factor (DF) measured under the following conditions:

1 kHz ±50 Hz and 1.0 ±0.2 V_{rms} if capacitance ≤ 10 µF

120 Hz ±10 Hz and 0.5 ±0.1 V_{rms} if capacitance > 10 µF

[4] To obtain IR limit, divide MΩ - µF value by the capacitance and compare to GΩ limit. Select the lower of the two limits.

Note: When measuring capacitance it is important to ensure the set voltage level is held constant. The HP4284 and Agilent E4980 have a feature known as Automatic Level Control (ALC). The ALC feature should be switched to "ON."

Post Environmental Limits

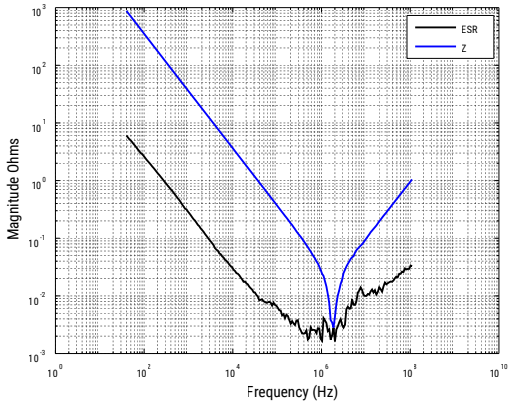
High Temperature Life, Biased Humidity, Moisture Resistance					
Dielectric	Rated DC Voltage	Capacitance Value	Dissipation Factor (Maximum %)	Capacitance Shift	Insulation Resistance
X7R	> 25	All	3.0	±20%	10% of Initial Limit
	16/25		5.0		
	< 16		7.5		

Insulation Resistance Limit Table

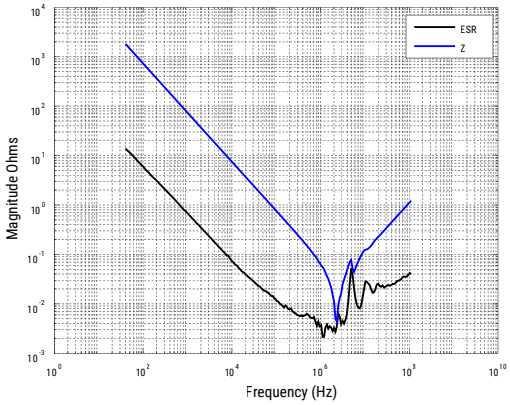
EIA Case Size	1,000 Megohm Microfarads or 100 GΩ	500 Megohm Microfarads or 10 GΩ
1210	< 0.39 µF	≥ 0.39 µF
2220	< 10 µF	≥ 10 µF

Electrical Characteristics

Z and ESR C1210C475M5R1L



Z and ESR C2220C225MAR2L



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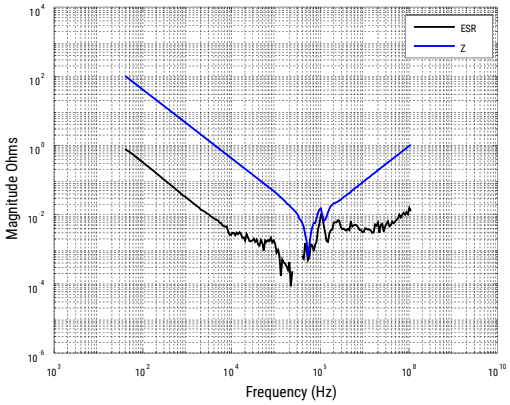
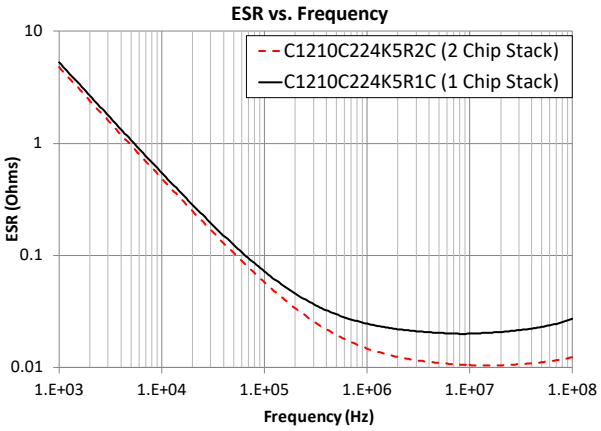
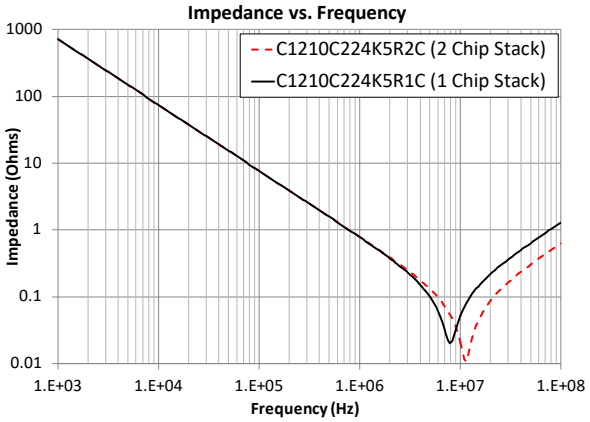


ESR – 1210, .22 µF, 50 V X7R

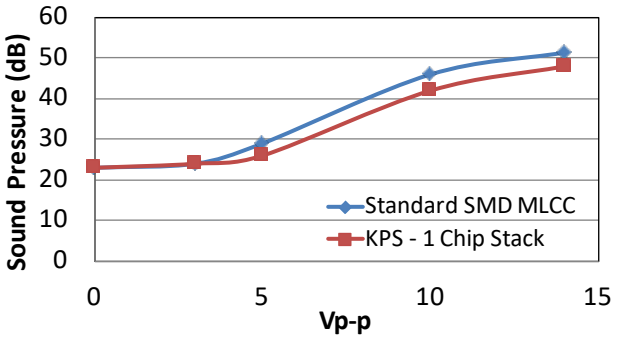


Impedance – 1210, .22 µF, 50 V X7R

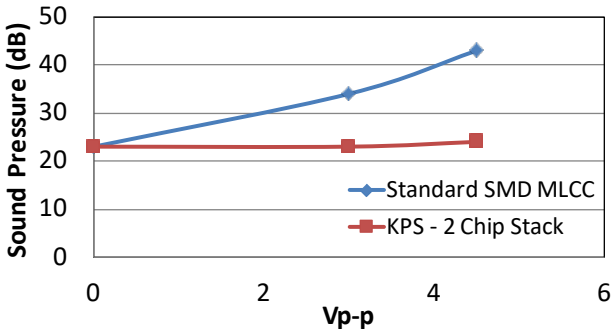


Electrical Characteristics cont.

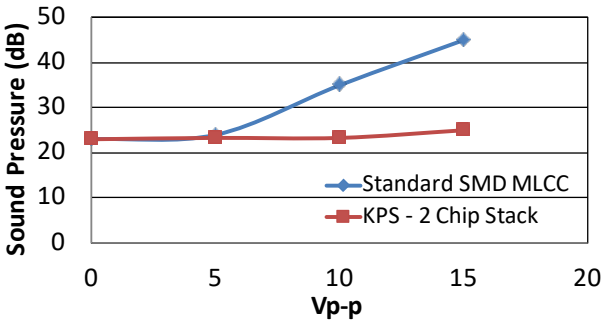
Microphonics – 1210, 4.7 µF, 50 V, X7R



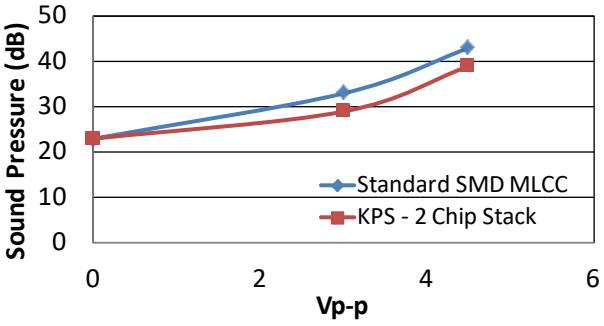
Microphonics – 2220, 22 µF, 50 V, X7R



Microphonics – 2220, 47 µF, 25 V, X7R

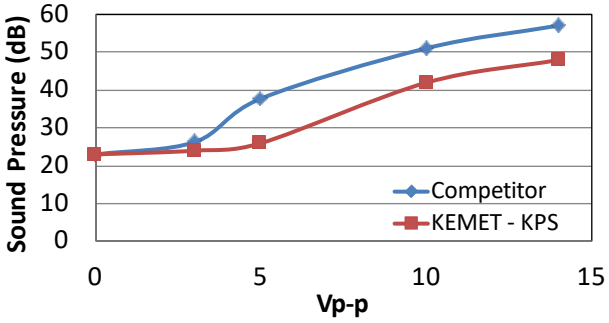


Microphonics – 1210, 22 µF, 25 V, X7R

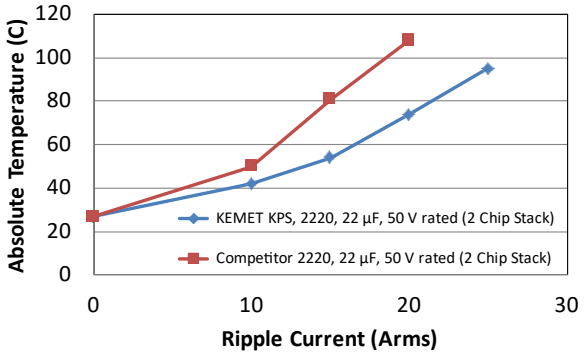


Competitive Comparision

Microphonics – 1210, 4.7 µF, 50 V, X7R



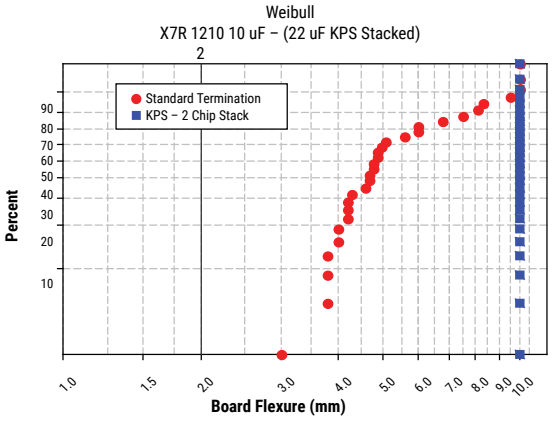
Ripple Current (Arms) 2220, 22 µF, 50 V



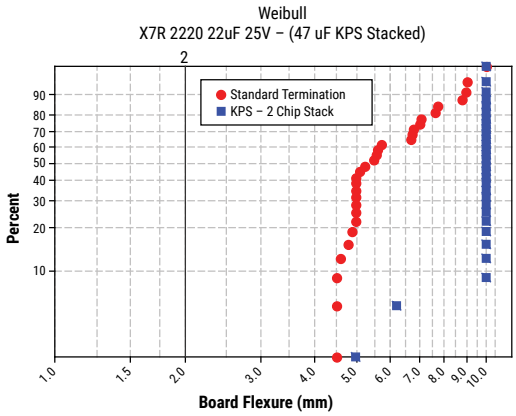
Note: Refer to Table 4 for test method.

Electrical Characteristics cont.

Board Flex vs. Termination Type



Board Flex vs. Termination Type



Board Flexure to 10 mm

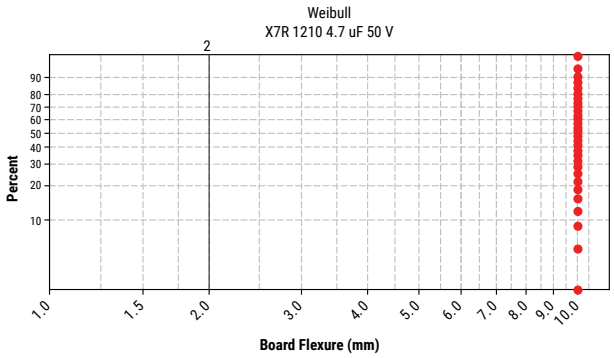


Table 1 – Capacitance Range/Selection Waterfall (1210 & 2220 Case Sizes)

Capacitance	Capacitance Code	Case Size/ Series		C1210C						C2220C					
		Voltage Code		8	4	3	5	1	A	4	3	5	M	1	A
		Rated Voltage (VDC)		10	16	25	50	100	250	16	25	50	63	100	250
		Capacitance Tolerance		Product Availability and Chip Thickness Codes See Table 2 for Chip Thickness Dimensions											
Single Chip Stack															
0.10 µF	104	K	M	FV	FV	FV	FV	FV	FV	JP	JP	JP	JP	JP	JP
0.22 µF	224	K	M	FV	FV	FV	FV	FV		JP	JP	JP	JP	JP	JP
0.47 µF	474	K	M	FV	FV	FV	FV	FV		JP	JP	JP	JP	JP	JP
1.0 µF	105	K	M	FV	FV	FV	FV	FV		JP	JP	JP	JP	JP	JP
2.2 µF	225	K	M	FV	FV	FV	FV			JP	JP	JP	JP	JP	
3.3 µF	335	K	M	FV	FV	FV	FV			JP	JP	JP	JP	JP	
4.7 µF	475	K	M	FV	FV	FV	FV			JP	JP	JP	JP		
10 µF	106	K	M	FV	FV	FV				JP	JP	JP	JP		
15 µF	156	K	M	FV						JP	JP				
22 µF	226	K	M	FV						JP	JP				
Double Chip Stack															
0.10 µF	104		M	FW	FW	FW	FW	FW	FW	JR	JR	JR	JR	JR	JR
0.22 µF	224		M	FW	FW	FW	FW	FW	FW	JR	JR	JR	JR	JR	JR
0.47 µF	474		M	FW	FW	FW	FW	FW		JR	JR	JR	JR	JR	JR
1.0 µF	105		M	FW	FW	FW	FW	FW		JR	JR	JR	JR	JR	JR
2.2 µF	225		M	FW	FW	FW	FW	FW		JR	JR	JR	JR	JR	JR
3.3 µF	335		M	FW	FW	FW	FW	FW		JR	JR	JR	JR	JR	
4.7 µF	475		M	FW	FW	FW	FW			JR	JR	JR	JR	JR	
10 µF	106		M	FW	FW	FW	FW			JR	JR	JR	JR		
22 µF	226		M	FW	FW	FW				JR	JR	JR	JR		
33 µF	336		M	FW						JR	JR				
47 µF	476		M	FW						JR	JR				
Capacitance	Capacitance Code	Rated Voltage (VDC)		10	16	25	50	100	250	16	25	50	63	100	250
		Voltage Code		8	4	3	5	1	A	4	3	5	M	1	A
		Case Size/Series		C1210C						C2220C					

Table 2 – Chip Thickness/Tape & Reel Packaging Quantities

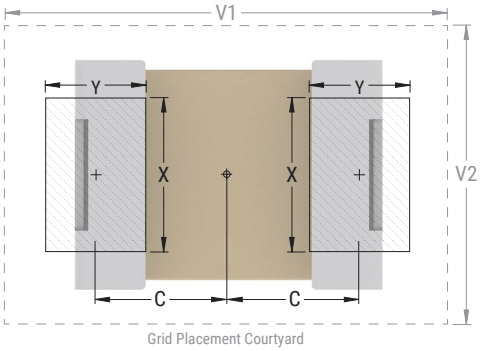
Thickness Code	Case Size	Thickness ± Range (mm)	Paper Quantity		Plastic Quantity	
			7" Reel	13" Reel	7" Reel	13" Reel
FV	1210	3.35 ±0.10	0	0	600	2,000
FW	1210	6.15 ±0.15	0	0	300	1,000
JP	2220	3.50 ±0.30	0	0	300	1,300
JR	2220	5.00 ±0.50	0	0	200	800
Thickness Code	**Case Size**	**Thickness ± Range (mm)**	**7" Reel**	**13" Reel**	**7" Reel**	**13" Reel**
			Paper Quantity		**Plastic Quantity**	

Package quantity based on finished chip thickness specifications.

Table 3 – KPS Land Pattern Design Recommendations (mm)

EIA SIZE CODE	METRIC SIZE CODE	Median (Nominal) Land Protrusion				
		C	Y	X	V1	V2
1210	3225	1.50	1.14	1.75	5.05	3.40
2220	5650	2.69	2.08	4.78	7.70	6.00

Image at right based on an EIA 1210 case size.



KEMET's KPS Series land pattern design recommendations have been evaluated through extensive internal testing and validation. KPS lead frames are used to mechanically isolate the MLCC from the PCB and provide stress relief for increased mechanical robustness. The land pattern dimensions for each EIA size code are designed to be encompassed within the end terminations thus regulating solder wicking and maintaining lead frame flexibility. This design is optimized to enable durable solder joint fillets which improve the mechanical integrity and reliability upon placement.

Soldering Process

KEMET's KPS devices are compatible with IR reflow techniques. Preheating of these components is recommended to avoid extreme thermal stress. KEMET's recommended profile conditions for IR reflow reflect the profile conditions of the IPC/J-STD-020D standard for moisture sensitivety testing.

To prevent degradation of temperature cycling capability, care must be taken to prevent solder from flowing into the inner side of the lead frames (inner side of "J" lead in contact with the circuit board).

After soldering, the capacitors should be air cooled to room temperature before further processing. Forced air cooling is not recommended.

Hand soldering should be performed with care due to the difficulty in process control. If performed, care should be taken to avoid contact of the soldering iron to the capacitor body. The iron should be used to heat the solder pad, applying solder between the pad and the lead, until reflow occurs. Once reflow occurs, the iron should be removed immediately. (Preheating is required when hand soldering to avoid thermal shock.)

Profile Feature	SnPb Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Minimum (T_{Smin})	100°C	150°C
Temperature Maximum (T_{Smax})	150°C	200°C
Time (t_s) from T_{smin} to T_{smax})	60 – 120 seconds	60 – 120 seconds
Ramp-up Rate (T_L to T_P)	3°C/seconds maximum	3°C/seconds maximum
Liquidous Temperature (T_L)	183°C	217°C
Time Above Liquidous (t_L)	60 – 150 seconds	60 – 150 seconds
Peak Temperature (T_P)	235°C	250°C
Time within 5°C of Maximum Peak Temperature (t_P)	20 seconds maximum	10 seconds maximum
Ramp-down Rate (T_P to T_L)	6°C/seconds maximum	6°C/seconds maximum
Time 25°C to Peak Temperature	6 minutes maximum	8 minutes maximum

Note: All temperatures refer to the center of the package, measured on the capacitor body surface that is facing up during assembly reflow.

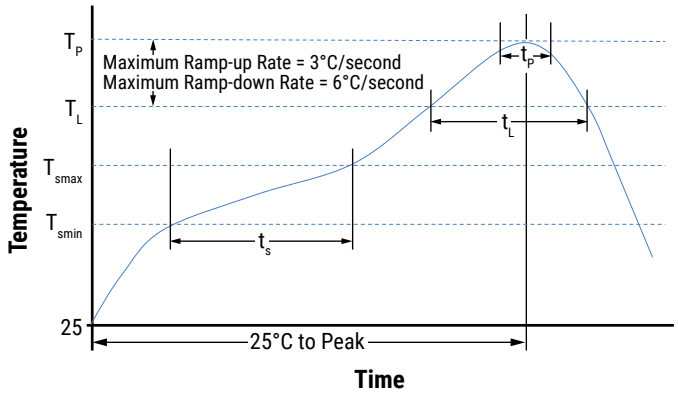


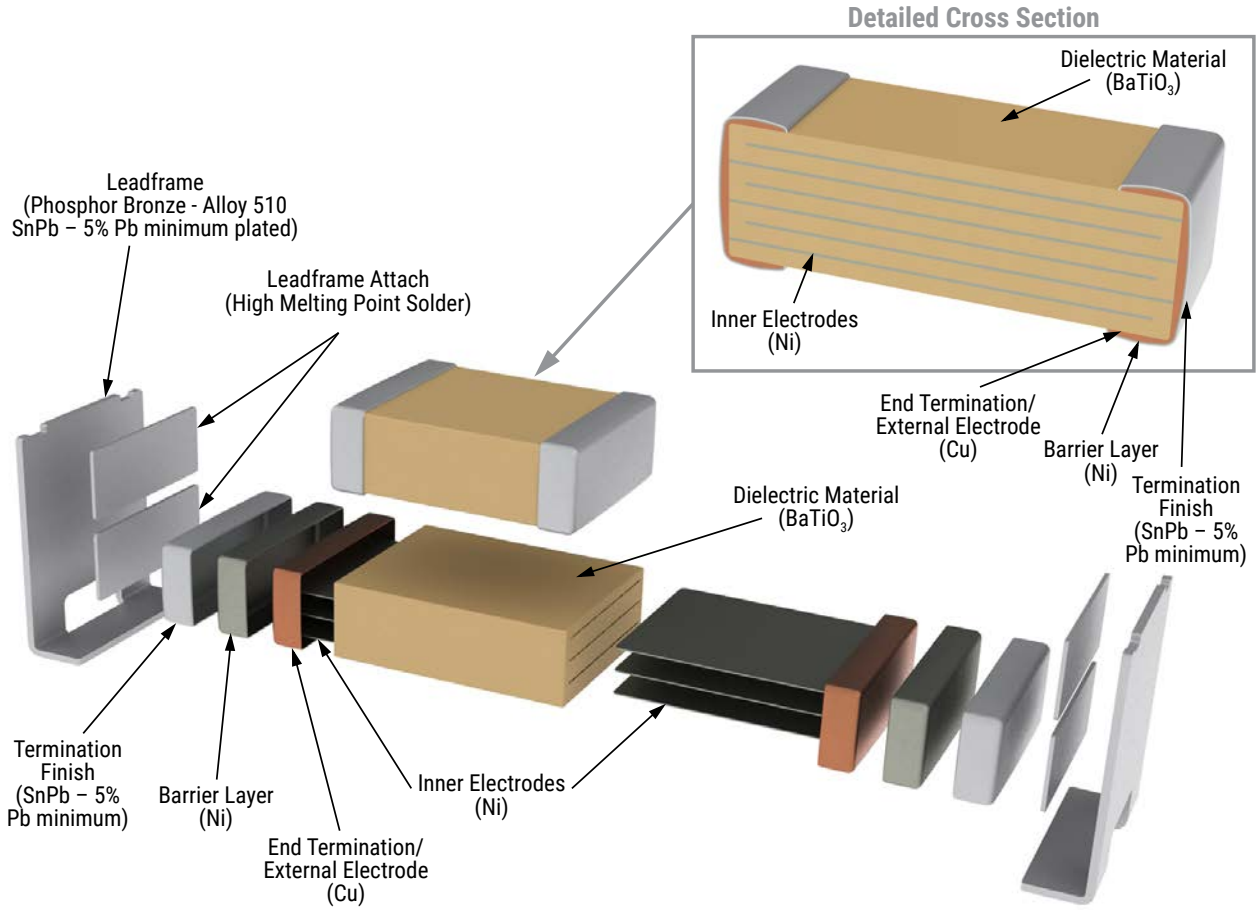
Table 4 – Performance & Reliability: Test Methods & Conditions

Stress	Reference	Test or Inspection Method
Terminal Strength	JIS-C-6429	Appendix 1, Note: Force of 1.8kg for 60 seconds
Board Flex	JIS-C-6429	Appendix 2, Note: 5.0 mm minimum
Solderability	J-STD-002	Magnification 50X. Conditions:
		a) Method B, 4 hours at 155°C, dry heat at 235°C
		b) Method B at 215°C category 3
		c) Method D, category 3 at 250°C
Temperature Cycling	JESD22 Method JA-104	1,000 Cycles (–55°C to +125°C), measurement at 24 hours ±4 hours after test conclusion.
Biased Humidity	MIL-STD-202 Method 103	Load Humidity: 1,000 hours 85°C/85% RH and rated voltage. Add 100K ohm resistor. Measurement at 24 hours ±4 hours after test conclusion.
		Low Volt Humidity: 1,000 hours 85C°/85%RH and 1.5V. Add 100K ohm resistor. Measurement at 24 hours ±4 hours after test conclusion.
Moisture Resistance	MIL-STD-202 Method 106	t = 24 hours/cycle. Steps 7a and 7b not required. Measurement at 24 hours ±4 hours after test conclusion.
Thermal Shock	MIL-STD-202 Method 107	–55°C/+125°C. Note: Number of cycles required – 300, maximum transfer time – 20 seconds, dwell time – 15 minutes. Air – air.
High Temperature Life	MIL-STD-202 Method 108	1,000 hours at 125°C with 1.5X rated voltage applied.
Storage Life	MIL-STD-202 Method 108	150°C, 0 VDC, for 1,000 hours.
Vibration	MIL-STD-202 Method 204	5 g's for 20 minutes, 12 cycles each of 3 orientations. Note: Use 8" X 5" PCB 0.031" thick 7 secure points on one long side and 2 secure points at corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10 – 2,000 Hz
Mechanical Shock	MIL-STD-202 Method 213	Figure 1 of Method 213, Condition F.
Resistance to Solvents	MIL-STD-202 Method 215	Add aqueous wash chemical – OKEM clean or equivalent.

Storage & Handling

Ceramic chip capacitors should be stored in normal working environments. While the chips themselves are quite robust in other environments, solderability will be degraded by exposure to high temperatures, high humidity, corrosive atmospheres, and long term storage. In addition, packaging materials will be degraded by high temperature – reels may soften or warp and tape peel force may increase. KEMET recommends that maximum storage temperature not exceed 40°C and maximum storage humidity not exceed 70% relative humidity. In addition, temperature fluctuations should be minimized to avoid condensation on the parts and atmospheres should be free of chlorine and sulfur bearing compounds. For optimized solderability chip stock should be used promptly, preferably within 1.5 years of receipt.

Construction



Product Marking

Laser marking option is not available on:

- C0G, Ultra-Stable X8R and Y5V dielectric devices
- EIA 0402 case size devices
- EIA 0603 case size devices with Flexible Termination option
- KPS Commercial and Automotive grade stacked devices

These capacitors are supplied unmarked only.

Tape & Reel Packaging Information

KEMET offers multilayer ceramic chip capacitors packaged in 8, 12 and 16 mm tape on 7" and 13" reels in accordance with EIA Standard 481. This packaging system is compatible with all tape-fed automatic pick and place systems. See Table 2 for details on reeling quantities for commercial chips.

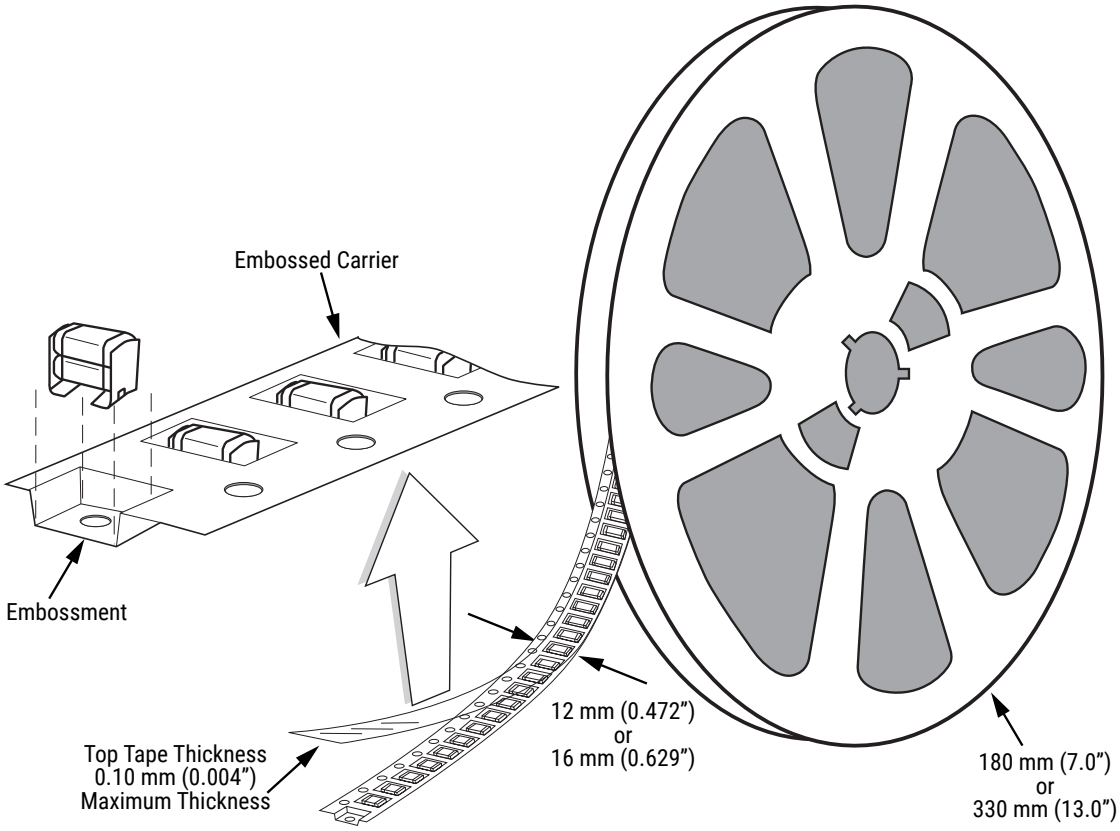


Table 5 – Carrier Tape Configuration – Embossed Plastic (mm)

EIA Case Size	Tape Size (W)*	Pitch (P_1)*
01005 – 0402	8	2
0603 – 1210	8	4
1805 – 1808	12	4
≥ 1812	12	8
KPS 1210	12	8
KPS 1812 and 2220	16	12
Array 0612	8	4

**Refer to Figure 1 for W and P_1 carrier tape reference locations.*
**Refer to Table 5 for tolerance specifications.*

Figure 1 – Embossed (Plastic) Carrier Tape Dimensions

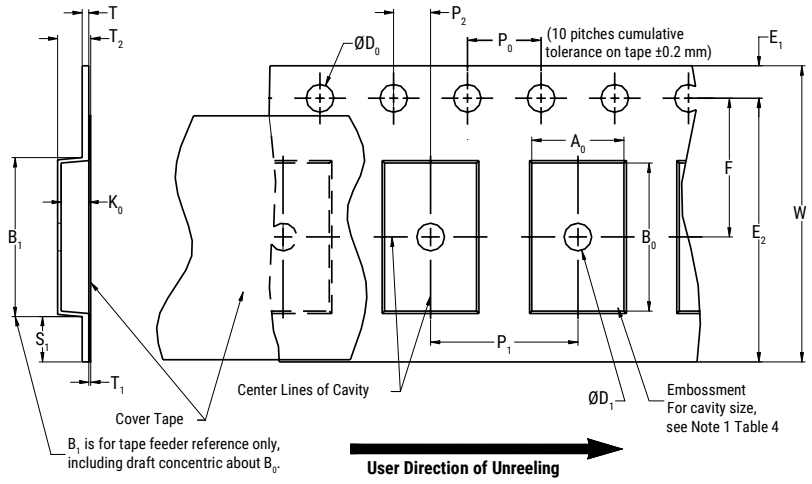


Table 6 – Embossed (Plastic) Carrier Tape Dimensions

Metric will govern

Constant Dimensions — Millimeters (Inches)									
Tape Size	D_0	D_1 Minimum Note 1	E_1	P_0	P_2	R Reference Note 2	S_1 Minimum Note 3	T Maximum	T_1 Maximim
8 mm	1.5 +0.10/0.0–0.0 (0.059 +0.004/–0.0)	1.0 (0.039)	1.75 ±0.10 (0.069 ±0.004)	4.0 ±0.10 (0.157 ±0.004)	2.0 ±0.05 (0.079 ±0.002)	25.0 (0.984)	0.600 (0.024)	0.600 (0.024)	0.100 (0.004)
12 mm		1.5 (0.059)				30 (1.181)			
16 mm									

Variable Dimensions — Millimeters (Inches)								
Tape Size	Pitch	B_1 Maximum Note 4	E_2 Minimum	F	P_1	T_2 Maximum	W Maximum	A_0, B_0 & K_0
8 mm	Single (4 mm)	4.35 (0.171)	6.25 (0.246)	3.5 ±0.05 (0.138 ±0.002)	4.0 ±0.10 (0.157 ±0.004)	2.5 (0.098)	8.3 (0.327)	Note 5
12 mm	Single (4 mm) and Double (8 mm)	8.2 (0.323)	10.25 (0.404)	5.5 ±0.05 (0.217 ±0.002)	8.0 ±0.10 (0.315 ±0.004)	4.6 (0.181)	12.3 (0.484)	
16 mm	Triple (12 mm)	12.1 (0.476)	14.25 (0.561)	7.5 ±0.05 (0.138 ±0.002)	12.0 ±0.10 (0.157 ±0.004)	4.6 (0.181)	16.3 (0.642)	

1. The embossment hole location shall be measured from the sprocket hole controlling the location of the embossment. Dimensions of embossment location and hole location shall be applied independent of each other.

2. The tape with or without components shall pass around R without damage (see Figure 5).

3. If S_1 < 1.0 mm, there may not be enough area for cover tape to be properly applied (see EIA Standard 481 paragraph 4.3 section b).

4. B_1 dimension is a reference dimension for tape feeder clearance only.

5. The cavity defined by A_0, B_0 and K_0 shall surround the component with sufficient clearance that:

(a) the component does not protrude above the top surface of the carrier tape.

(b) the component can be removed from the cavity in a vertical direction without mechanical restriction, after the top cover tape has been removed.

(c) rotation of the component is limited to 20° maximum for 8 and 12 mm tapes and 10° maximum for 16 mm tapes (see Figure 2).

(d) lateral movement of the component is restricted to 0.5 mm maximum for 8 and 12 mm wide tape and to 1.0 mm maximum for 16 mm tape (see Figure 3).

(e) for KPS Series product, A_0 and B_0 are measured on a plane 0.3 mm above the bottom of the pocket.

(f) see Addendum in EIA Standard 481 for standards relating to more precise taping requirements.

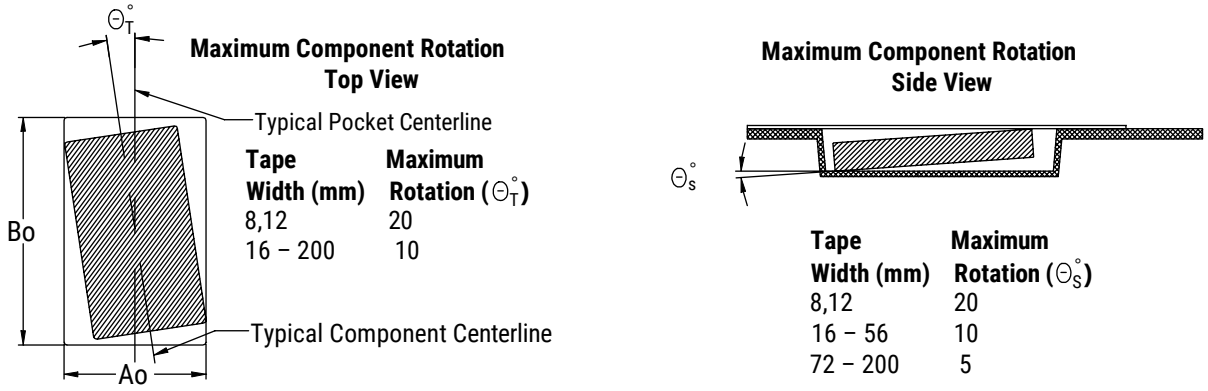
Packaging Information Performance Notes

1. Cover Tape Break Force: 1.0 kg minimum.
2. Cover Tape Peel Strength: The total peel strength of the cover tape from the carrier tape shall be:

Tape Width	Peel Strength
8 mm	0.1 to 1.0 newton (10 to 100 gf)
12 and 16 mm	0.1 to 1.3 newton (10 to 130 gf)

The direction of the pull shall be opposite the direction of the carrier tape travel. The pull angle of the carrier tape shall be 165° to 180° from the plane of the carrier tape. During peeling, the carrier and/or cover tape shall be pulled at a velocity of 300 ±10 mm/minute.
3. Labeling: Bar code labeling (standard or custom) shall be on the side of the reel opposite the sprocket holes. *Refer to EIA Standards 556 and 624*.

Figure 2 – Maximum Component Rotation



Tape Width (mm)	Maximum Rotation (Θ_T°)
8,12	20
16 – 200	10

Tape Width (mm)	Maximum Rotation (Θ_S°)
8,12	20
16 – 56	10
72 – 200	5

Figure 3 – Maximum Lateral Movement

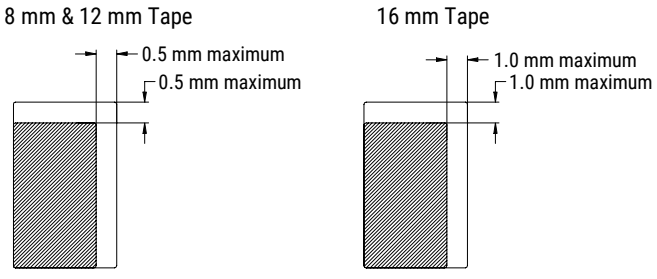


Figure 4 – Bending Radius

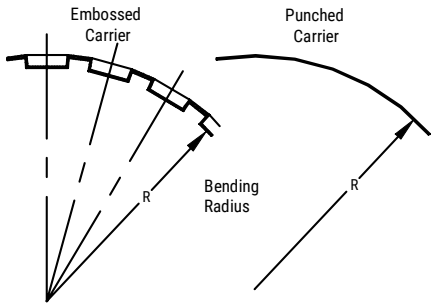
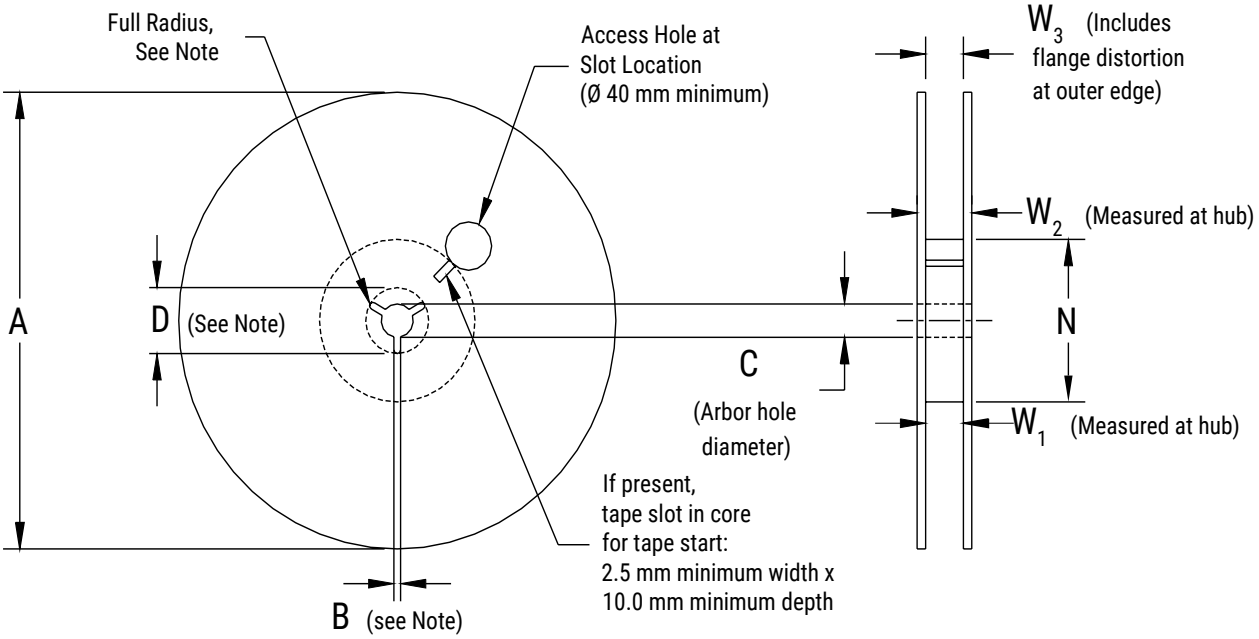


Figure 5 – Reel Dimensions



Note: Drive spokes optional; if used, dimensions B and D shall apply.

Table 7 – Reel Dimensions

Metric will govern

Constant Dimensions — Millimeters (Inches)				
Tape Size	A	B Minimum	C	D Minimum
8 mm	178 ±0.20 (7.008 ±0.008) or 330 ±0.20 (13.000 ±0.008)	1.5 (0.059)	13.0 +0.5/−0.2 (0.521 +0.02/−0.008)	20.2 (0.795)
12 mm				
16 mm				

Variable Dimensions — Millimeters (Inches)				
Tape Size	N Minimum	W_1	W_2 Maximum	W_3
8 mm	50 (1.969)	8.4 +1.5/−0.0 (0.331 +0.059/−0.0)	14.4 (0.567)	Shall accommodate tape width without interference
12 mm		12.4 +2.0/−0.0 (0.488 +0.078/−0.0)	18.4 (0.724)	
16 mm		16.4 +2.0/−0.0 (0.646 +0.078/−0.0)	22.4 (0.882)	

Figure 6 – Tape Leader & Trailer Dimensions

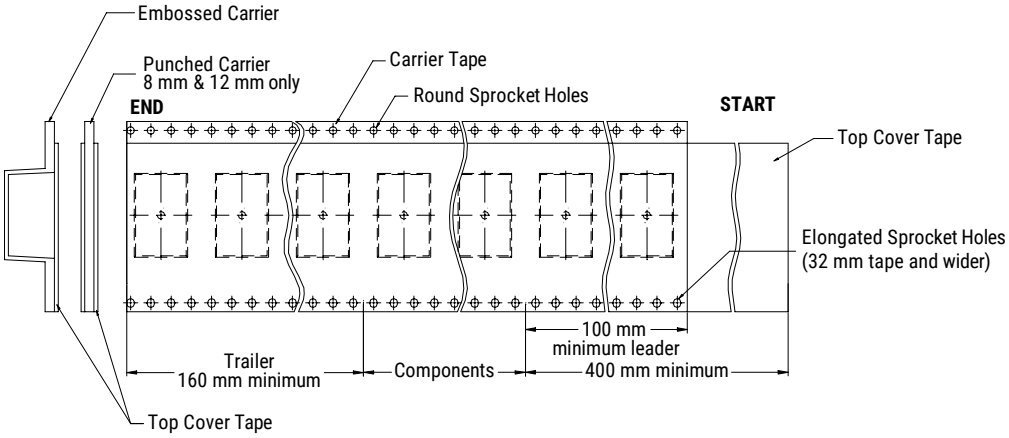
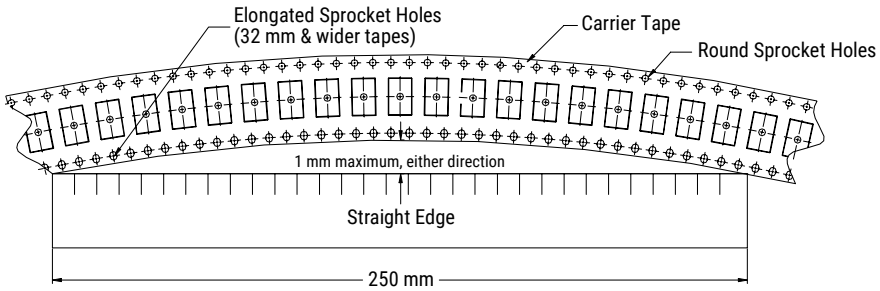


Figure 7 – Maximum Camber



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