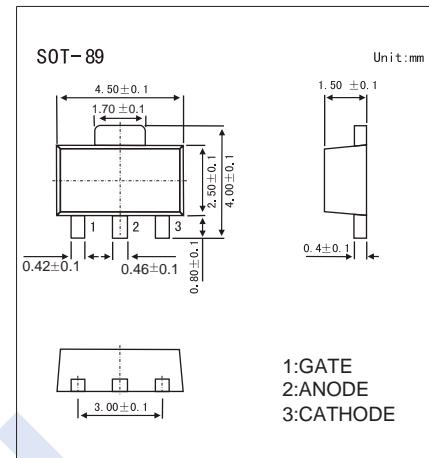


## SCR Thyristor

### BT169 (KT169)

#### ■ Features

- Repetitive peak off-state voltages :400V
- Average on-state current :0.5A
- RMS on-state current :0.8A
- Non-repetitive peak on-state current :8A



#### ■ Absolute Maximum Ratings Ta = 25°C

Parameter	Symbol	Rating	Unit
Peak Repetitive Forward and Reverse Blocking Voltages	BT169-400	V <sub>DRM</sub> V <sub>RRM</sub>	400
Average on-state Current	I <sub>T(AV)</sub>	0.5	
Forward Current RMS	I <sub>T(RMS)</sub>	0.8	
Non-Repetitive Peak on-state Current (t=10ms)	I <sub>TSM</sub>	8	A
Non-Repetitive Peak on-state Current (t=8.3ms)		9	
Circuit Fusing Considerations (t = 10ms)	I <sup>2</sup> t	0.32	A <sup>2</sup> s
Repetitive Rate of rise of on-state Current after Triggering	dI/dt	50	A/us
Peak Gate Current	I <sub>GM</sub>	1	A
Peak Gate Voltage	V <sub>GM</sub>	5	V
Peak Gate Voltage — Reverse	V <sub>GRM</sub>	5	
Peak Gate Power — Forward	P <sub>GM</sub>	2	W
Average Gate Power — Forward	P <sub>GF(AV)</sub>	0.1	
Thermal Resistance Junction to Ambient	R <sub>thJA</sub>	150	K/W
Thermal Resistance Junction to Case	R <sub>thJC</sub>	60	
Junction Temperature	T <sub>J</sub>	125	°C
Storage Temperature Range	T <sub>stg</sub>	-40 to 150	

## SCR Thyristor

### BT169 (KT169)

■ Electrical Characteristics ( $T_a = 25^\circ\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
Peak Repetitive Forward and Reverse Blocking Voltages	$V_{DRM}$ $V_{RRM}$	$I_{DRM}=I_{RRM}50\mu\text{A}$	400			V
Off-state Leakage Current	$I_D, I_R$	$V_{DRM}=V_{RRM}(\text{max}); T_j=125^\circ\text{C}; R_{GK}=1\text{k}\Omega$		0.1	mA	
On-state Voltage	$V_{TM}$	$I_T=1\text{A}$		1.5		
Gate Trigger Voltage	$V_{GT}$	$V_D=12\text{V}, I_T=10\text{mA}$		0.8		V
		$V_D= V_{DRM}(\text{max}), I_T=10\text{mA}; T_j=125^\circ\text{C}$	0.2			
Gate Trigger Current (Continuous dc)	$I_{GT}$	$V_D=12\text{V}, I_T=10\text{mA}$		200	uA	
Latching Current	$I_L$	$V_D=12\text{V}, I_{GT}=0.5\text{mA}; R_{GK}=1\text{k}\Omega$		6		
Holding Current	$I_H$	$V_D=12\text{V}, I_{GT}=0.5\text{mA}; R_{GK}=1\text{k}\Omega$		5		
Critical Rate of rise of off-state Voltage	$dV/dt$	$V_{DM}=67\% V_{DRM}(\text{max}); T_j=125^\circ\text{C}$ exponential waveform; $R_{GK}=1\text{k}\Omega$		25		V/us
Gate Controlled turn-on time	$t_{gt}$	$I_{TM}=2\text{A}; V_D=V_{DRM}(\text{max}), G=10\text{mA};$ $dI_G/dt=0.1\text{A/us}$		2		
Circuit Commutated turn-off time	$t_q$	$V_D=67\% V_{DRM}(\text{max}); T_j=125^\circ\text{C},$ $T_M=1.6\text{A}; V_R=35\text{V};$ $dI_M/dt=30\text{A/us}, dV/dt=2\text{V/us}; R_{GK}=1\text{k}\Omega$		100		us

■ Classification of  $I_{GT}$  (uA)

Type	BT169-400	BT169-400A	BT169-400B
Range	0-200	10-30	30-60
Marking	BT/C39	BT/C35	BT/C36

## SCR Thyristor

### BT169 (KT169)

#### ■ Typical Characteristics

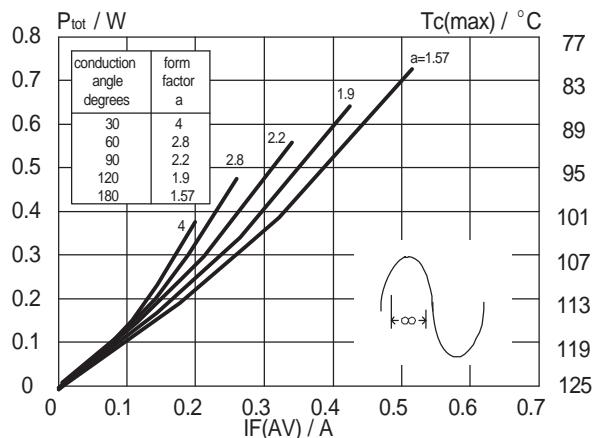


FIG.1 Maximum on-state dissipation,  $P_{tot}$ , versus average on-state current,  $I_{F(AV)}$ , where  $a$ =form factor= $I_{T(RMS)} / I_{F(AV)}$

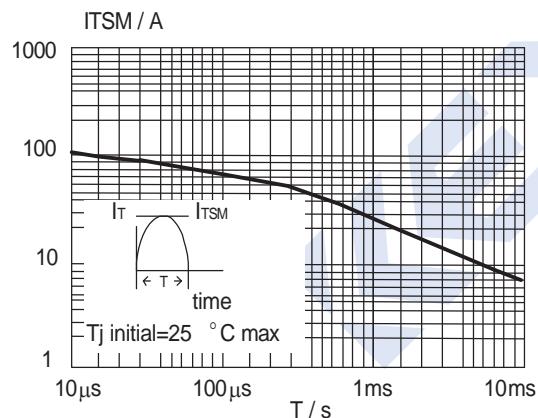


FIG.2 Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus pulse width  $t_p$ , for sinusoidal currents,  $t_p \leq 10\text{ms}$ .

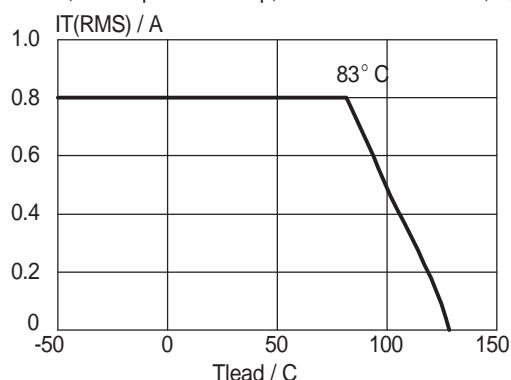


FIG.3 Maximum permissible rms current  $I_{T(RMS)}$ , versus lead temperature,  $T_{lead}$

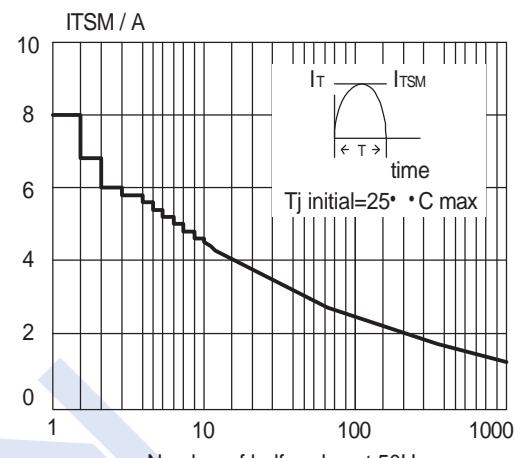


FIG.4 Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus number of cycles, for sinusoidal currents,  $f = 50\text{Hz}$ .

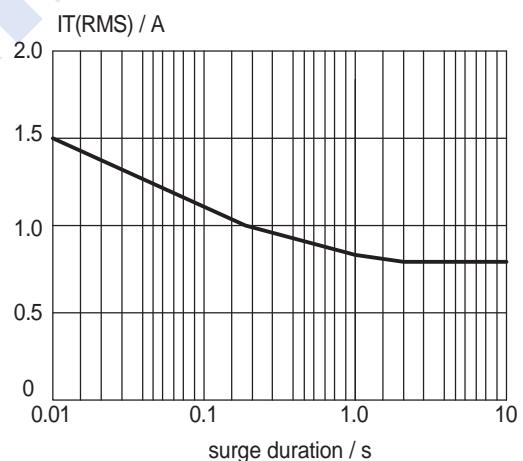


FIG.5 Maximum permissible repetitive rms on-state current  $I_{T(RMS)}$ , versus surge duration, for sinusoidal currents,  $f = 50\text{Hz}$ ;  $T_{lead} \leq 83^\circ\text{C}$

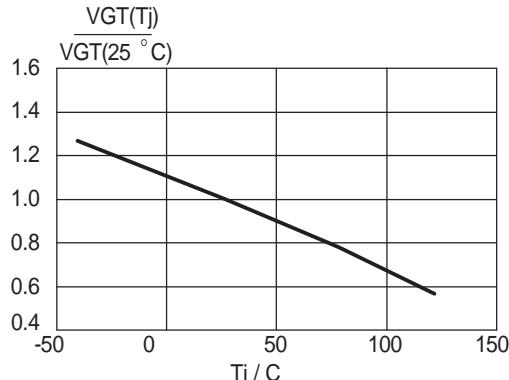


FIG.6 Normalised gate trigger voltage  $V_{GT}(T_j) / V_{GT}(25^\circ\text{C})$ , versus junction temperature  $T_j$

## SCR Thyristor

### BT169 (KT169)

#### ■ Typical Characteristics

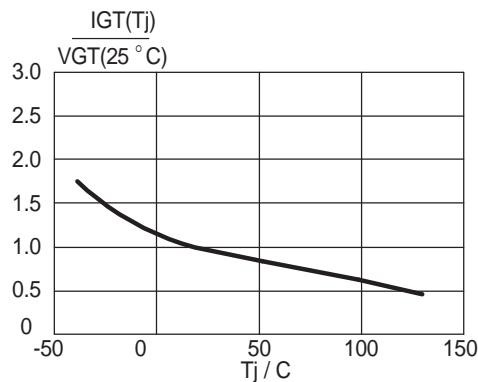


FIG.7 Normalised gate trigger current  $I_{GT}(T_j)/I_{GT}(25^\circ C)$ , versus junction temperature  $T_j$

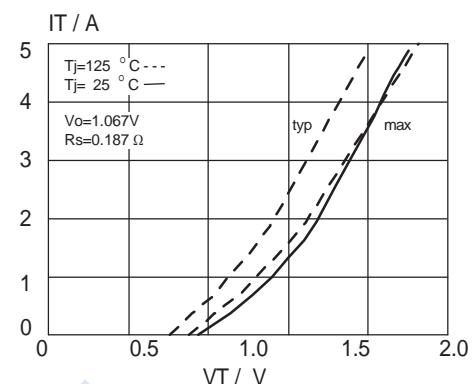


FIG.10 Typical and maximum on-state characteristic.

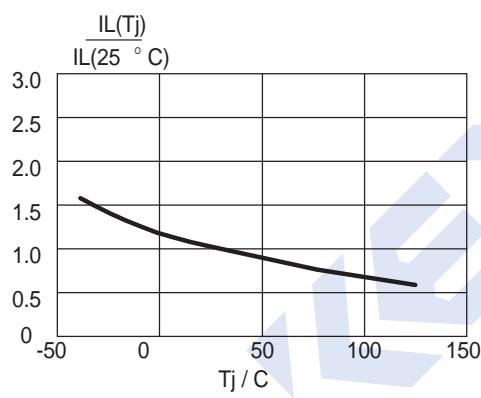


FIG.8 Normalised latching current  $I_L(T_j)/I_L(25^\circ C)$ , versus junction temperature  $T_j$ ,  $R_{GK}= 1K\Omega$

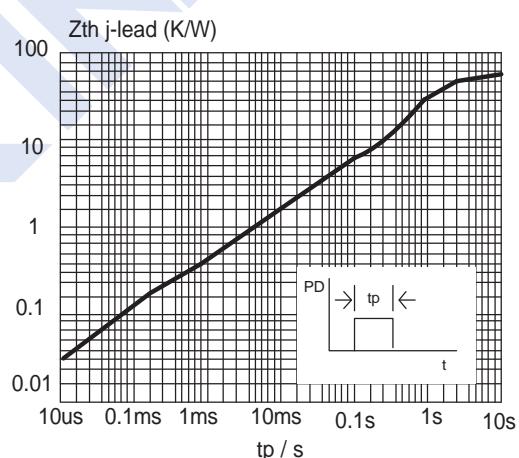


FIG.11 Transient thermal impedance  $Z_{th} \text{ j-lead}$ , versus pulse width  $t_p$ .

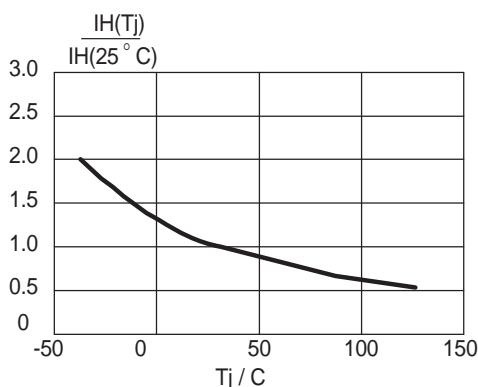


FIG.9 Normalised holding current  $I_H(T_j)/I_H(25^\circ C)$ , versus junction temperature  $T_j$ ,  $R_{GK}=1K\Omega$

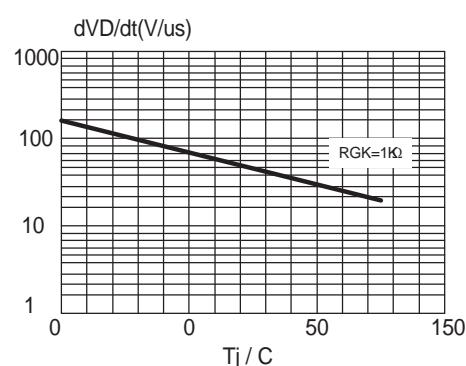


FIG.12 Typical, critical rate of rise of off-state voltage,  $dV/dt$  versus junction temperature  $T_j$ .

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