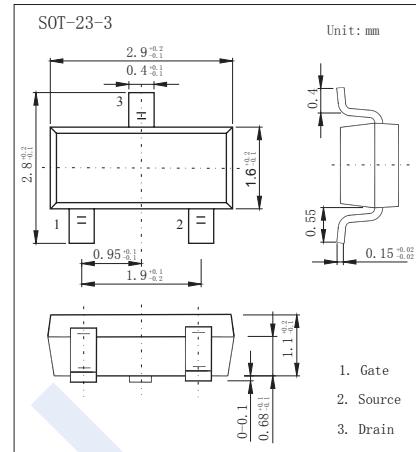
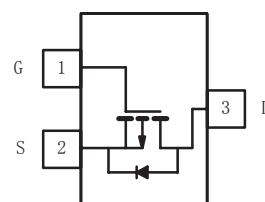


P-Channel Enhancement MOSFET

SI2333CDS (KI2333CDS)

■ Features

- V_{DS} (V) = -12V
- I_D = -5.1A (V_{GS} = -4.5V)
- $R_{DS(ON)} < 35m\Omega$ (V_{GS} = -4.5V)
- $R_{DS(ON)} < 45m\Omega$ (V_{GS} = -2.5V)
- $R_{DS(ON)} < 59m\Omega$ (V_{GS} = -1.8V)



■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	5 sec	Steady State	Unit
Drain-Source Voltage	V_{DS}	-12		V
Gate-Source Voltage	V_{GS}	± 8		
Continuous Drain Current ($T_j = 150^\circ\text{C}$) *1	I_D	-7.1	-5.1	A
		-5.7	-4.0	
Pulsed Drain Current	I_{DM}	-20		
Power Dissipation	P_D	2.5	1.25	W
		1.6	0.8	
Thermal Resistance.Junction- to-Ambient	R_{thJA}	100		$^\circ\text{C}/\text{W}$
Thermal Resistance.Junction- to-Foot	R_{thJF}	50		
Junction Temperature	T_J	150		$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to 150		

*1 Surface Mounted on 1" x 1" FR4 Board.

P-Channel Enhancement MOSFET

SI2333CDS (KI2333CDS)

■ Electrical Characteristics $T_a = 25^\circ\text{C}$

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DSS}	$I_D = -250 \mu\text{A}, V_{GS} = 0\text{V}$	-12			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12\text{V}, V_{GS} = 0\text{V}$			-1	μA
		$V_{DS} = -12\text{V}, V_{GS} = 0\text{V}, T_J = 55^\circ\text{C}$			-10	
Gate-Body leakage current	I_{GSS}	$V_{DS} = 0\text{V}, V_{GS} = \pm 8\text{V}$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-0.4		-1	V
Static Drain-Source On-Resistance *1	$R_{DS(on)}$	$V_{GS} = -4.5\text{V}, I_D = -5.1\text{A}$		28.5	35	$\text{m}\Omega$
		$V_{GS} = -2.5\text{V}, I_D = -4.5\text{A}$		36	45	
		$V_{GS} = -1.8\text{V}, I_D = -2.0\text{A}$		46	59	
On state drain current *1	$I_{D(on)}$	$V_{GS} = -4.5\text{V}, V_{DS} = -5\text{V}$	-20			A
Forward Transconductance *1	g_{FS}	$V_{DS} = -5\text{V}, I_D = -1.9\text{A}$		1.6		S
Gate Resistance	R_g	$f = 1\text{MHz}$		4.0		Ω
Input Capacitance	C_{iss}	$V_{GS} = 0\text{V}, V_{DS} = -6\text{V}, f = 1\text{MHz}$		1225		pF
Output Capacitance	C_{oss}			315		
Reverse Transfer Capacitance	C_{rss}			260		
Total Gate Charge	Q_g	$V_{GS} = -4.5\text{V}, V_{DS} = -6\text{V}, I_D = -5.1\text{A}$		15	25	nC
		$V_{GS} = -2.5\text{V}, V_{DS} = -6\text{V}, I_D = -5.1\text{A}$		9	15	
Gate Source Charge	Q_{gs}	$V_{GS} = -4.5\text{V}, V_{DS} = -6\text{V}, I_D = -5.1\text{A}$		1.9		nC
Gate Drain Charge	Q_{gd}			3.8		
Turn-On DelayTime	$t_{d(on)}$	$V_{GS} = -4.5\text{V}, V_{DS} = -6\text{V}, R_L = 6\Omega, R_{GEN} = 1\Omega$ $I_D = -1.0\text{A}$		13	20	ns
Turn-On Rise Time	t_r			35	60	
Turn-Off DelayTime	$t_{d(off)}$			45	70	
Turn-Off Fall Time	t_f			12	20	
Body Diode Reverse Recovery Charge	Q_{rr}	$IF = 1.0\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$		20	40	nC
Body Diode Reverse Recovery Time	t_{rr}			32	50	
Reverse Recovery Fall Time	t_a			16		ns
Reverse Recovery Rise Time	t_b			16		
Maximum Body-Diode Continuous Current	I_S	$T_c = 25^\circ\text{C}$			-1.0	A
Pulse Diode Forward Current *1	I_{SM}				-20	
Diode Forward Voltage	V_{SD}	$I_S = -1.0\text{A}, V_{GS} = 0\text{V}$		-0.7	-1.2	V

*1Pulse test: PW $\leq 300\text{us}$ duty cycle $\leq 2\%$.

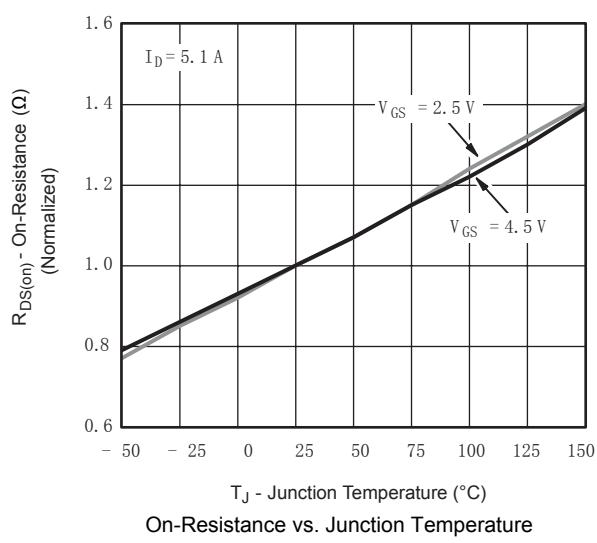
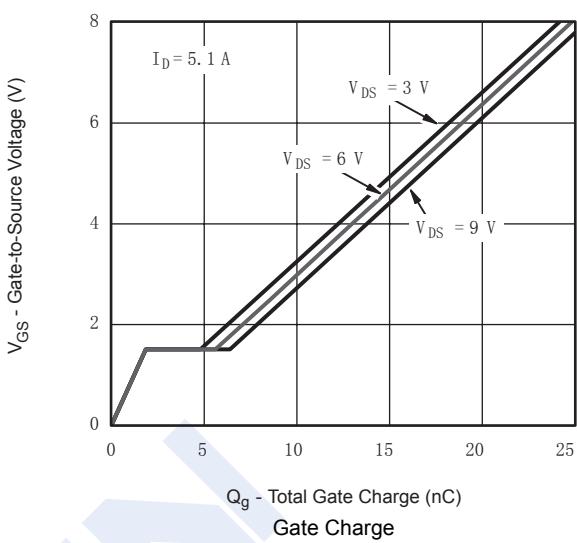
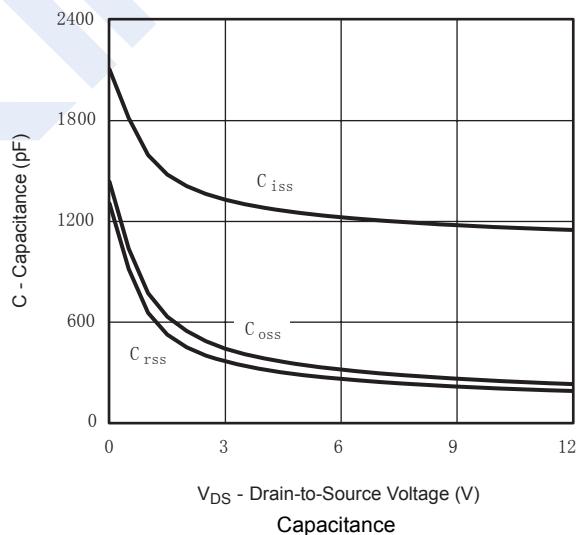
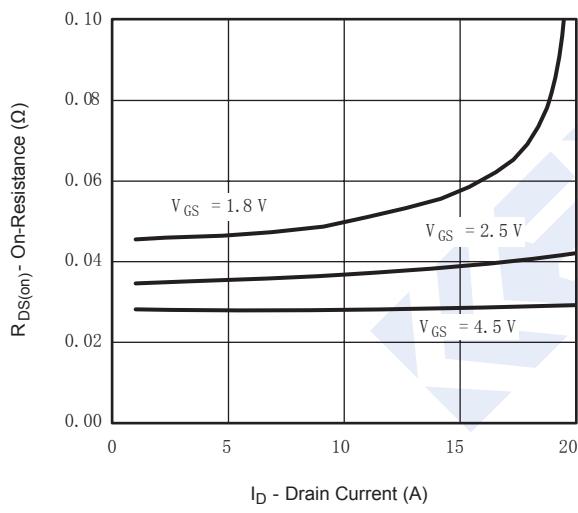
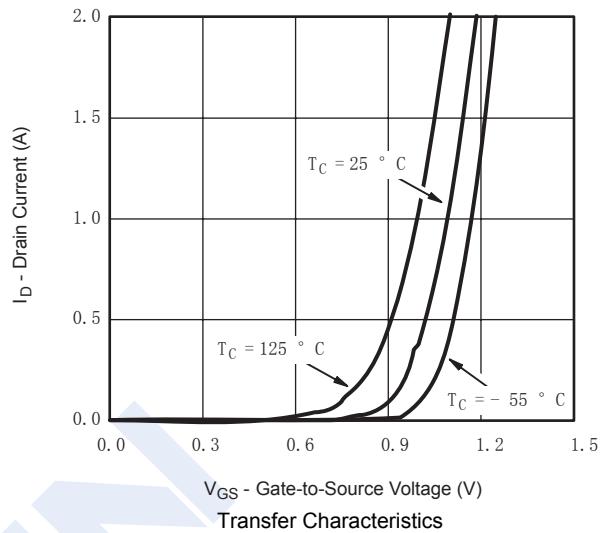
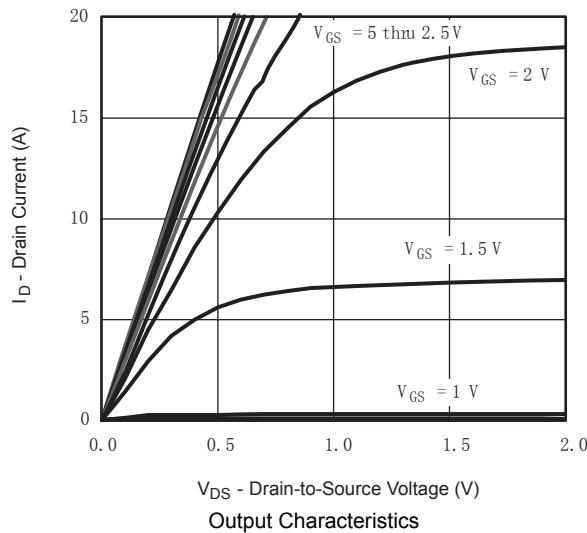
■ Marking

Marking	O3*
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P-Channel Enhancement MOSFET

SI2333CDS (KI2333CDS)

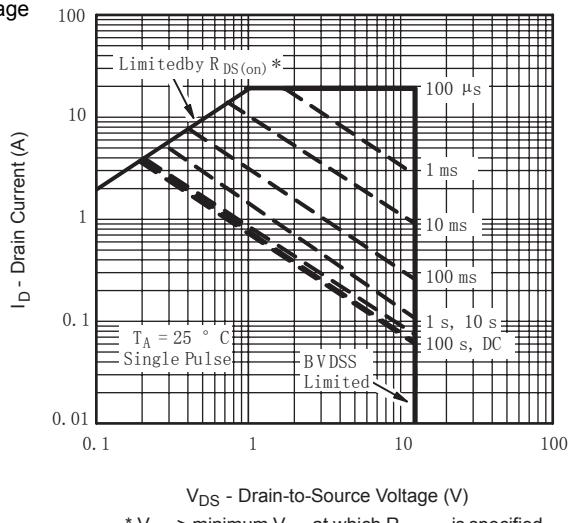
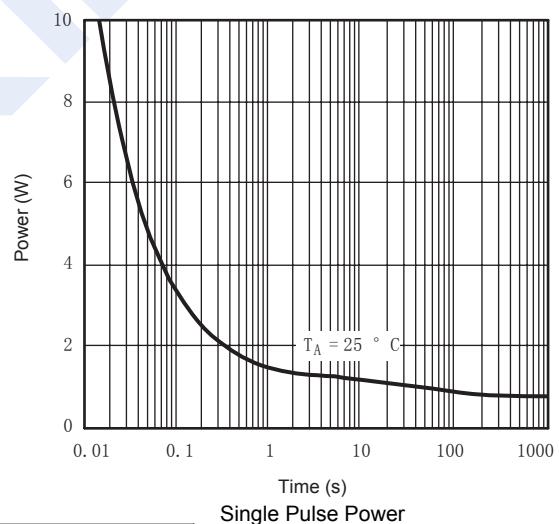
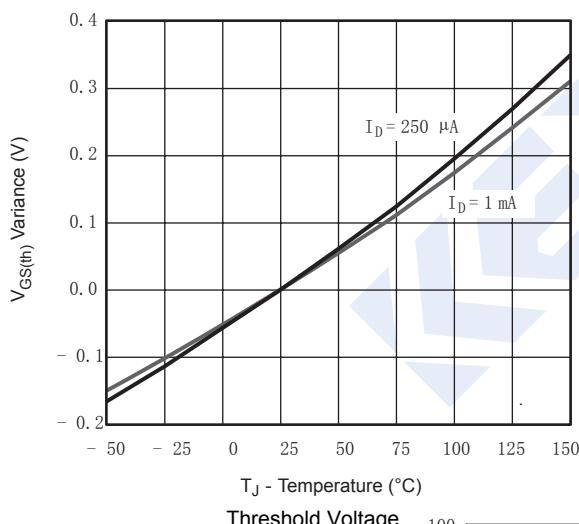
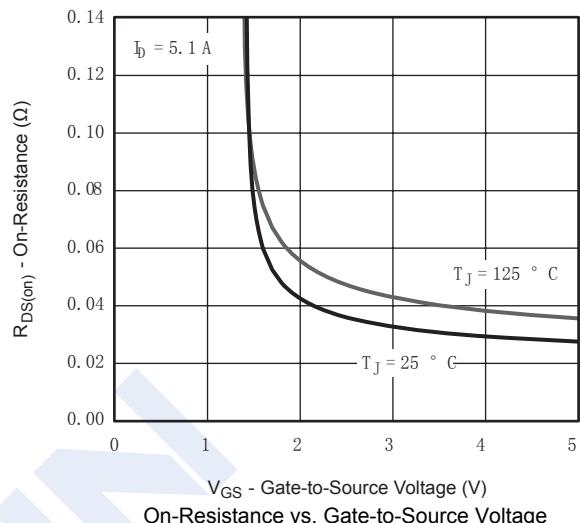
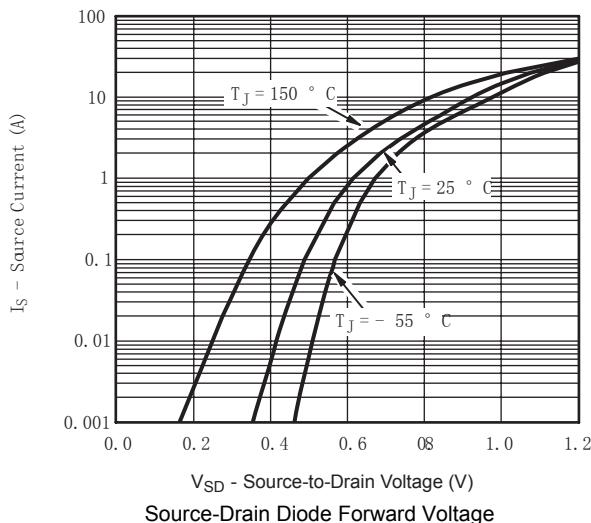
■ Typical Characteristics



P-Channel Enhancement MOSFET

SI2333CDS (KI2333CDS)

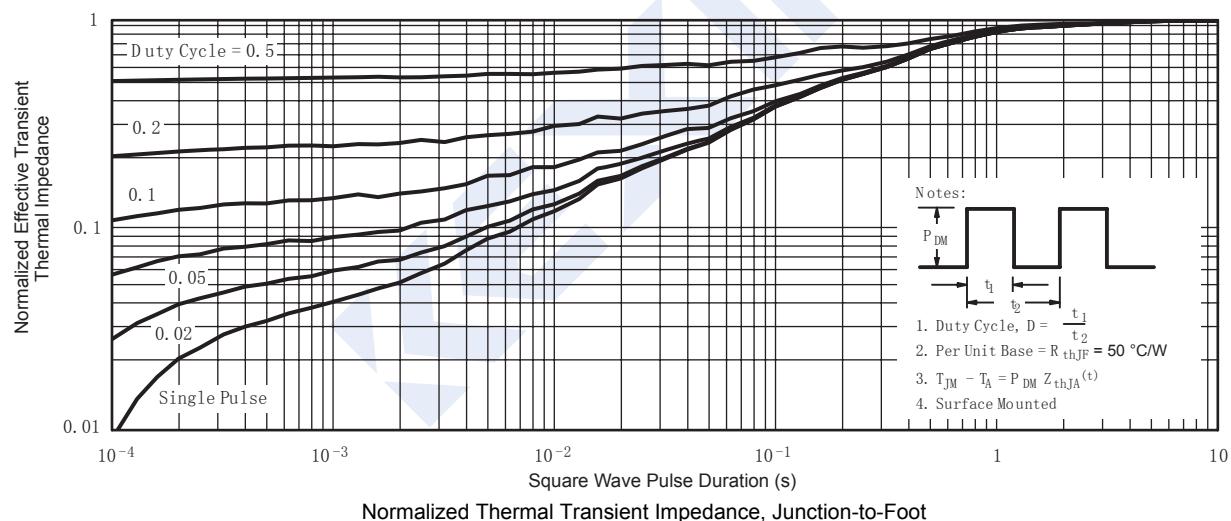
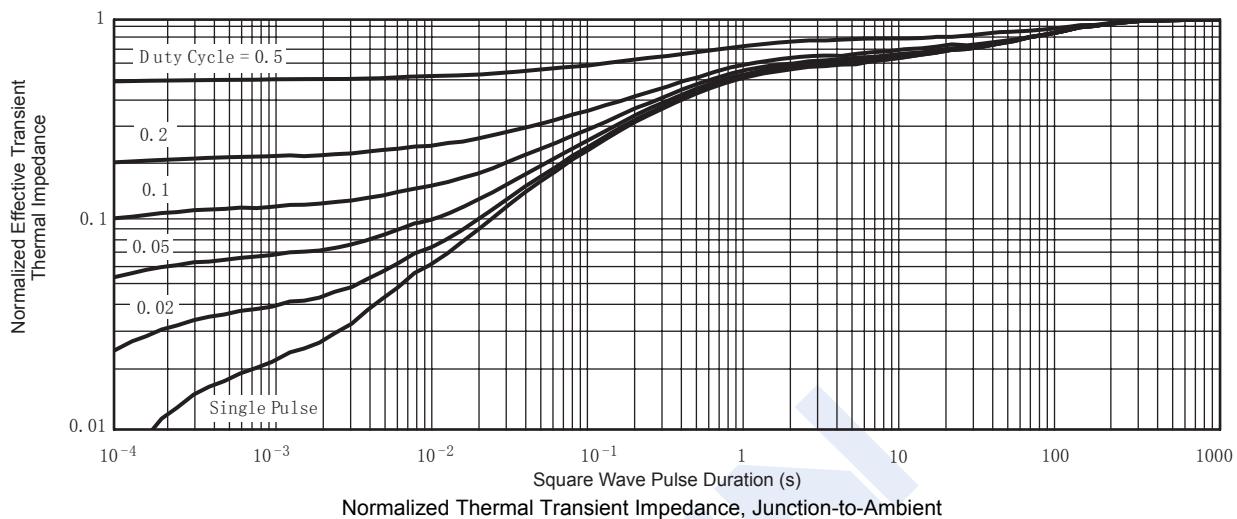
■ Typical Characteristics



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified
Safe Operating Area

P-Channel Enhancement MOSFET
SI2333CDS (KI2333CDS)

■ Typical Characteristics



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