

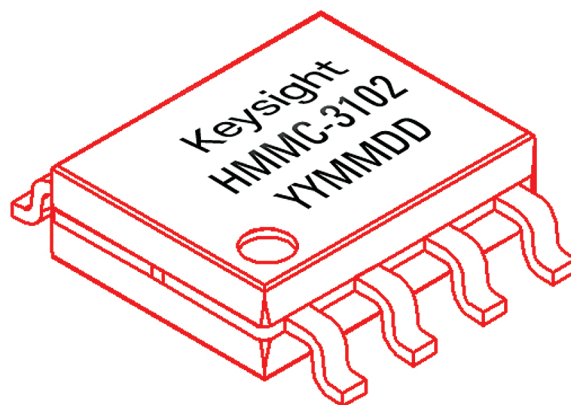
Keysight Technologies

HMMC-3102 DC-1 GHz Packaged Divide-by-Prescaler

1GC1-8204-TR1-7" diameter reel/500 each

1GC1-8204-BLK-bubble strip/10 each

Data Sheet

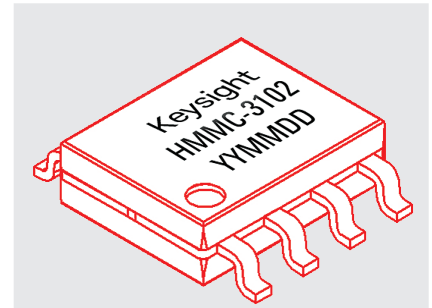


Features

- Wide frequency range:
0.2 - 16 GHz
- High input power sensitivity:
On-chip pre- and post-amps
 - 20 to +10 dBm (1 - 10 GHz)
 - 15 to +10 dBm (10 - 12 GHz)
 - 10 to +5 dBm (12 - 15 GHz)
- P_{out} : +6 dBm ($0.99 V_{p-p}$)
will drive ECL
- Low phase noise:
-153 dBc/Hz @ 100 kHz offset
- (+) or (-) Single supply bias
with wide range: 4.5 to 6.5 V
- Differential I/O with on-chip
50 Ω matching

Description

The Keysight Technologies, Inc. HMMC-3102 is a packaged GaAs HBT MMIC prescaler which offers dc to 16 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise.



Package type:
8-lead SOIC plastic
Package dimensions:
4.9 x 3.9 mm typ.
Package thickness:
1.55 mm typ.
Lead pitch:
1.25 mm nom.
Lead width:
0.42 mm nom.

Absolute maximum ratings¹

(@ $T_A = 25\text{ }^\circ\text{C}$, unless otherwise indicated)

| Symbol | Parameters/conditions | Min | Max | Units |
|-------------------|---|----------------|------------------|------------------|
| $V_{CC} - V_{EE}$ | Bias supply voltage | | +7 | volts |
| V_{EE} | Bias supply voltage | -7 | | volts |
| $V_{CC} - V_{EE}$ | Bias supply delta | 0 | +7 | volts |
| V_{Logic} | Logic threshold voltage | $V_{CC} - 1.5$ | $V_{CC} - 1.2$ | volts |
| $P_{in(CW)}$ | CW RF input power | | +10 | dBm |
| V_{RFIn} | DC input voltage (@ RF_{in} or RF_{in} ports) | | $V_{CC} \pm 0.5$ | volts |
| T_{BS}^2 | Backside ambient temperature | -40 | +85 | $^\circ\text{C}$ |
| T_{st} | Storage temperature | -65 | +165 | $^\circ\text{C}$ |
| T_{max} | Max. assembly temperature (60 s max.) | | 310 | $^\circ\text{C}$ |

1. Operation in excess of any parameter limit (except T_{BS}) may cause permanent damage to the device.
2. $MTTF > 1 \times 10^6$ hours @ $T_{BS} \leq 85\text{ }^\circ\text{C}$. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.

DC Specifications/physical properties¹

($T_A = 25\text{ }^\circ\text{C}$, $V_{CC} - V_{EE} = 5.0$ volts, unless otherwise listed)

| Symbol | Parameters/conditions | Min | Typ | Max | Units |
|--------------------------------|---|-----------------|-----------------|-----------------|-------|
| $V_{CC} - V_{EE}$ | Operating bias supply difference ¹ | 4.5 | 5.0 | 6.5 | Volts |
| $ I_{CC} $ or $ I_{EE} $ | Bias supply current | 68 | 80 | 92 | mA |
| $V_{RFIn(q)}$, $V_{RFOut(q)}$ | Quiescent dc voltage appearing at all RF ports | | V_{CC} | | Volts |
| V_{Logic} | Nominal ECL Logic Level (V_{Logic} contact self-bias voltage, generated on-chip) | $V_{CC} - 1.45$ | $V_{CC} - 1.35$ | $V_{CC} - 1.25$ | Volts |

1. Prescaler will operate over full specified supply voltage range, V_{CC} or V_{EE} not to exceed limits specified in *Absolute maximum ratings* section.

RF specifications

($T_A = 25\text{ }^\circ\text{C}$, $Z_o = 50\ \Omega$, $V_{CC} - V_{EE} = 5.0\text{ volts}$)

| Symbol | Parameters/conditions | Min | Typ | Max | Units |
|--------------------|---|---|-------|-----|--------|
| $f_{in(max)}$ | Maximum input frequency of operation | 16 | 18 | | GHz |
| $f_{in(min)}$ | Minimum input frequency of operation ¹ ($P_{in} = -10\text{ dBm}$) | | 0.2 | 0.5 | GHz |
| $f_{Self-Osc.}$ | Output self-oscillation frequency ² | | 3.4 | | GHz |
| P_{in} | @ DC (Square-wave input) | -15 | > -25 | +10 | dBm |
| | @ $f_{in} = 500\text{ MHz}$ (Sine-wave input) | -15 | > -20 | +10 | dBm |
| | $f_{in} = 1\text{ to }10\text{ GHz}$ | -15 | > -25 | +10 | dBm |
| | $f_{in} = 10\text{ to }12\text{ GHz}$ | -10 | > -15 | +10 | dBm |
| P_{in} | $f_{in} = 12\text{ to }15\text{ GHz}$ | -4 | > -10 | +4 | dBm |
| | RL | Small-signal input/output return loss (@ $f_{in} < 12\text{ GHz}$) | | 15 | |
| S_{12} | Small-signal reverse isolation (@ $f_{in} < 12\text{ GHz}$) | | 30 | | dB |
| ϕ_N | SSB phase noise (@ $P_{in} = 0\text{ dBm}$, 100 kHz offset from a $f_{out} = 1.2\text{ GHz}$ carrier) | | -153 | | dBc/Hz |
| Jitter | Input signal time variation @ zero-crossing ($f_{in} = 10\text{ GHz}$, $P_{in} = -10\text{ dBm}$) | | 1 | | ps |
| T_r or T_f | Output transition time (10% to 90% rise/fall time) | | 70 | | ps |
| P_{out}^3 | @ $f_{out} < 1\text{ GHz}$ | 4 | 6 | | dBm |
| | @ $f_{out} = 2.5\text{ GHz}$ | 3.5 | 5.5 | | dBm |
| | @ $f_{out} = 3.5\text{ GHz}$ | 0 | 2.0 | | dBm |
| $ V_{out(p-p)} ^4$ | @ $f_{out} < 1\text{ GHz}$ | | 0.99 | | Volts |
| | @ $f_{out} = 2.5\text{ GHz}$ | | 0.94 | | Volts |
| | @ $f_{out} = 3.5\text{ GHz}$ | | 0.63 | | Volts |
| $P_{Spitback}$ | f_{out} power level appearing at RF_{in} or \overline{RF}_{in} (@ $f_{in} = 12\text{ GHz}$, unused RF_{out} or \overline{RF}_{out} unterminated) | | -40 | | dBm |
| | f_{out} power level appearing at RF_{in} or \overline{RF}_{in} (@ $f_{in} = 12\text{ GHz}$, both RF_{out} and \overline{RF}_{out} terminated) | | -47 | | dBm |
| $P_{feedthru}$ | Power level of f_{in} appearing at RF_{out} or \overline{RF}_{out} (@ $f_{in} = 10\text{ GHz}$, $P_{in} = 0\text{ dBm}$, referred to $P_{in}(f_{in})$) | | -23 | | dBc |
| H_2 | Second harmonic distortion output level (@ $f_{out} = 3.0\text{ GHz}$, referred to $P_{out}(f_{out})$) | | -25 | | dBc |

1. For sine-wave input signal. Prescaler will operate down to D.C. for square-wave input signal. Minimum divide frequency limited by input slew-rate.
2. Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the Input dc offset technique described on page 4.
3. Fundamental of output square wave's Fourier Series.
4. Square wave amplitude calculated from P_{out} .

Applications

The HMMC-3102 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broad-band frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 16 GHz bandwidth. Below 200 MHz the prescaler input is “slew-rate” limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to dc when driven with a square-wave.

Due to the presence of an off-chip RF-bypass capacitor inside the package (connected to the V_{CC} contact on the device), and the unique design of the device itself, the component may be biased from either a single positive or single negative supply bias. The backside of the package is not dc connected to any dc bias point on the device.

For positive supply operation, V_{CC} pins are nominally biased at any voltage in the +4.5 to +6.5 volt range with pin 8 (V_{EE}) grounded. For negative bias operation V_{CC} pins are typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to pin 8 (V_{EE}).

ac-Coupling and dc-Blocking

All RF ports are dc connected on-chip to the V_{CC} contact through on-chip $50\ \Omega$ resistors. Under any bias conditions where V_{CC} is not dc grounded the RF ports should be ac coupled via series capacitors mounted on the PC-board at each RF port. Only under bias conditions where V_{CC} is dc grounded (as is typical for negative bias supply operation) may the RF ports be direct coupled to adjacent circuitry or in some cases, such as level shifting to subsequent stages. In the latter case the package heat sink may be “floated” and bias applied as the difference between V_{CC} and V_{EE} .

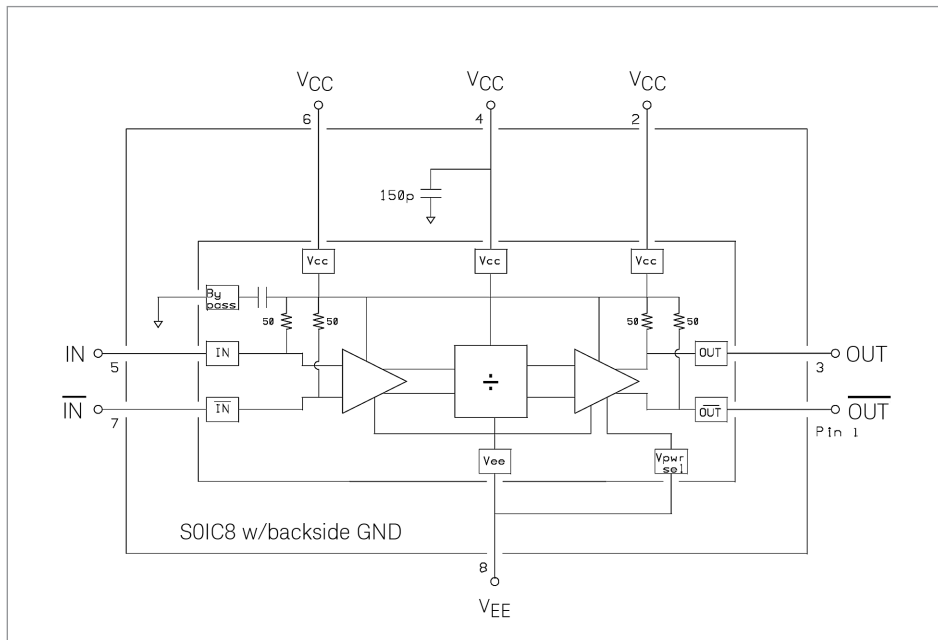


Figure 1. Simplified schematic diagram

Input dc Offset

If an RF signal with sufficient signal to noise ratio is present at the RF input lead, the prescaler will operate and provide a divided output equal the input frequency divided by the divide modulus. Under certain “ideal” conditions where the input is well matched at the right input frequency, the component may “self-oscillate”, especially under small signal input powers or with only noise present at the input. This “self-oscillation” will produce an undesired output signal also known as a false trigger. To prevent false triggers or self-oscillation conditions, apply a 20 to 100 mV dc offset voltage between the RF_{in} and RF_{in} ports. This prevents noise or spurious low level signals from triggering the divider.

Adding a 10 k Ω resistor between the unused RF input to a contact point at the V_{EE} potential will result in an offset of \approx 25 mV between the RF inputs. Note however, that the input sensitivity will be reduced slightly due to the presence of this offset.

Assembly Notes

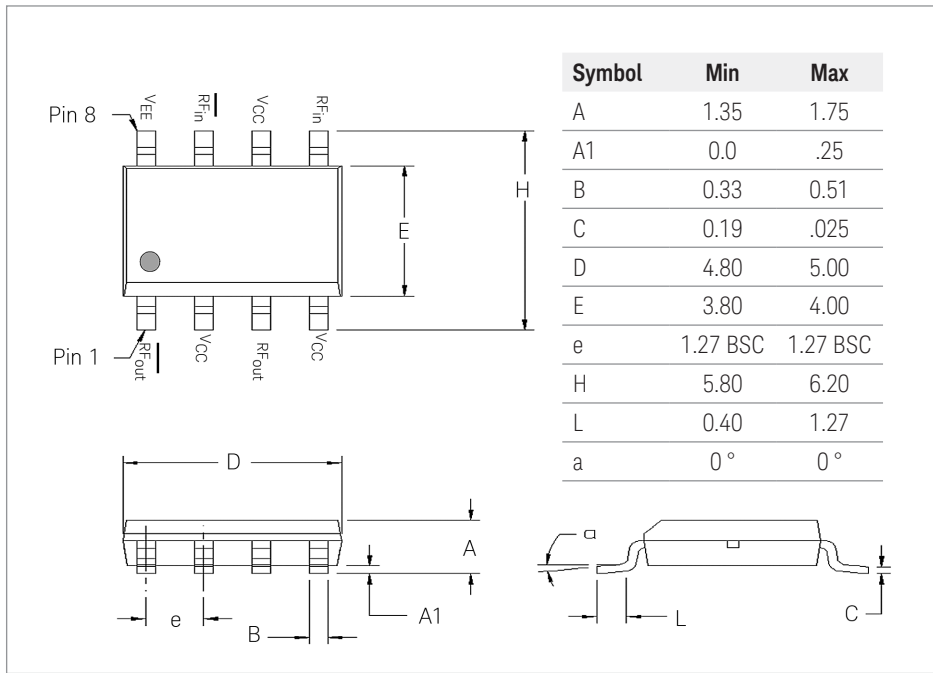
Independent of the bias applied to the package, the backside of the package should always be connected to both a good RF ground plane and a good thermal heat sinking region on the PC board to optimize performance. For single-ended output operation the unused RF output lead should be terminated into 50 Ω to a contact point at the VCC potential or to RF ground through a dc blocking capacitor.

A minimum RF and thermal PC board contact area equal to or greater than 2.67 \times 1.65 mm (0.105” \times 0.065”) with eight 0.020” diameter plated-wall thermal vias is recommended.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Keysight Technologies application note 5991-3484EN, *GaAs MMIC ESD, Die Attach and Bonding Guidelines* provides basic information on these subjects.

Moisture Sensitivity Classification: Class 5A, per JESD22-A112-A.



Notes

- All dimensions in millimeters.
- Refer to JEDEC Outline MS-012 for additional tolerances.
- Exposed heat slug area on package bottom = 2.67 × 1.65.
- Exposed heat sink on package bottom must be soldered to PCB rf ground plane.

Figure 2. Package and dimensions

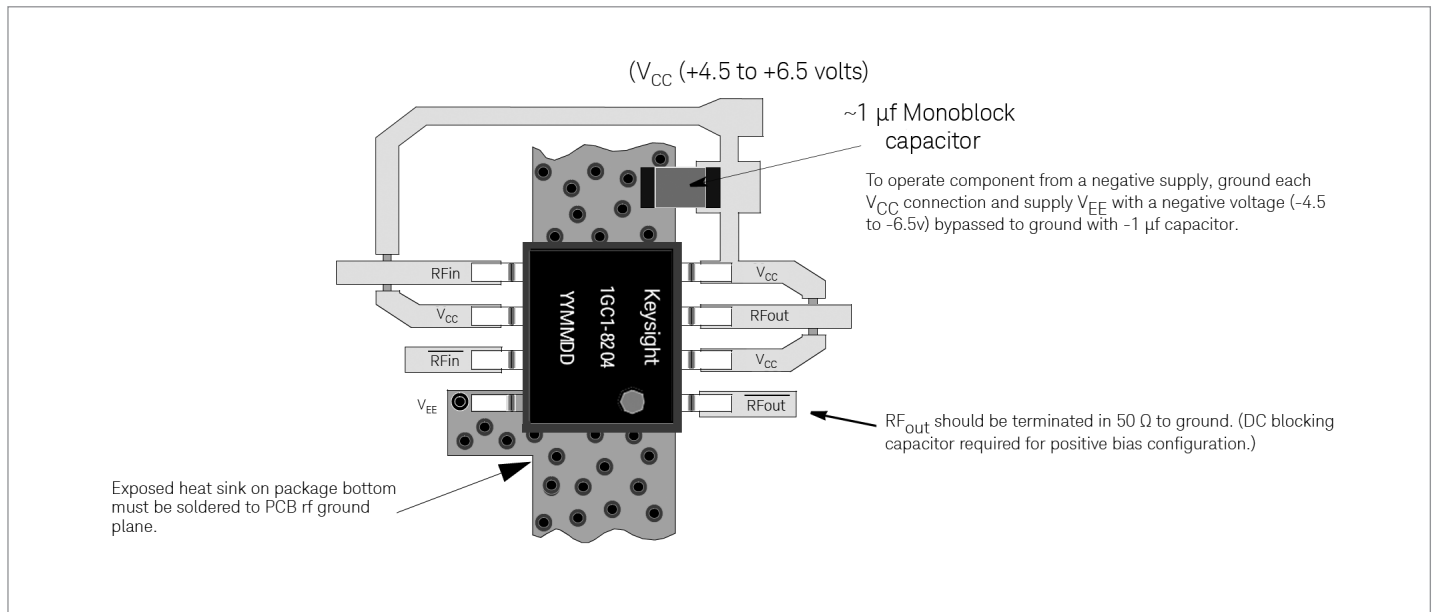


Figure 3. Assembly diagram (single-supply, positive-bias configuration shown)

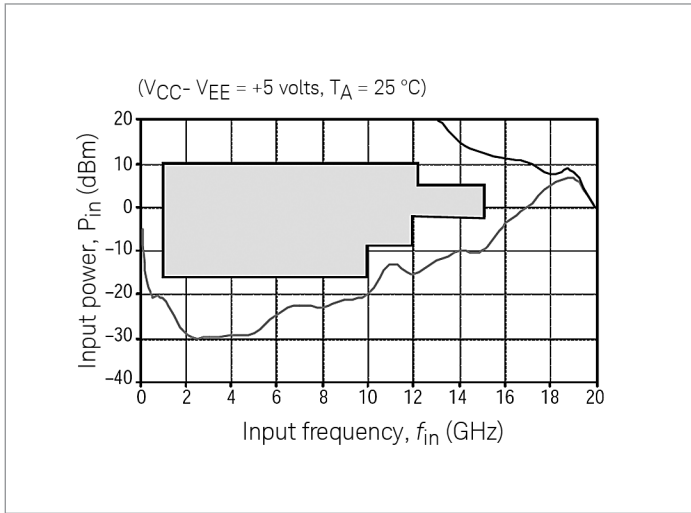


Figure 4. Typical input sensitivity window

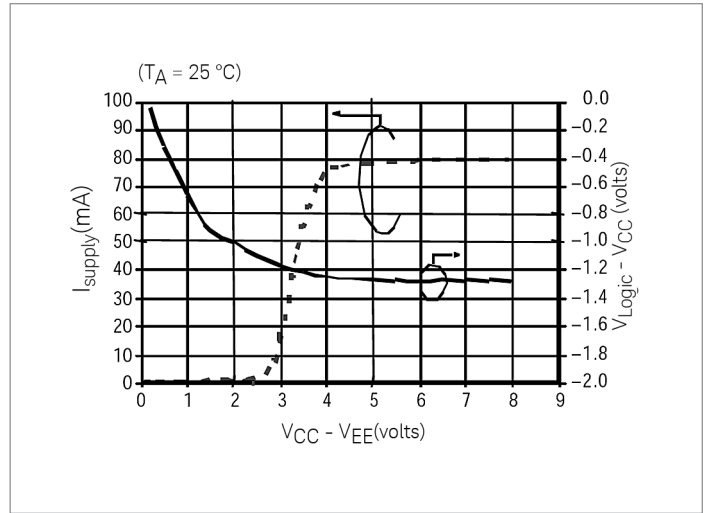


Figure 5. Typical supply current & V_{Logic} vs. supply voltage

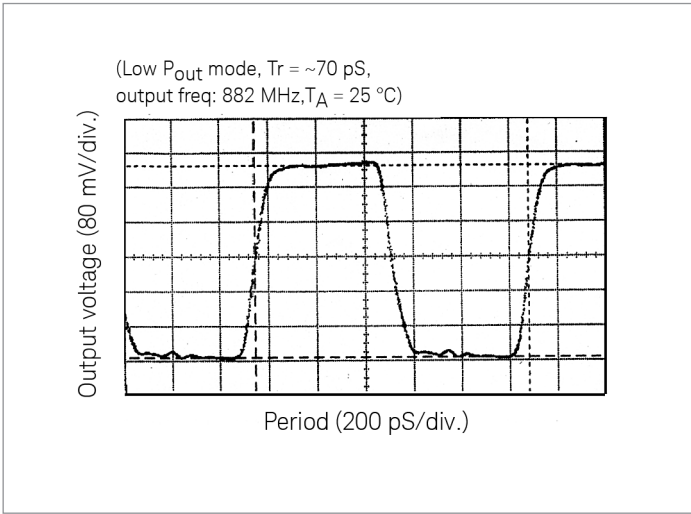


Figure 6. Typical output voltage waveform

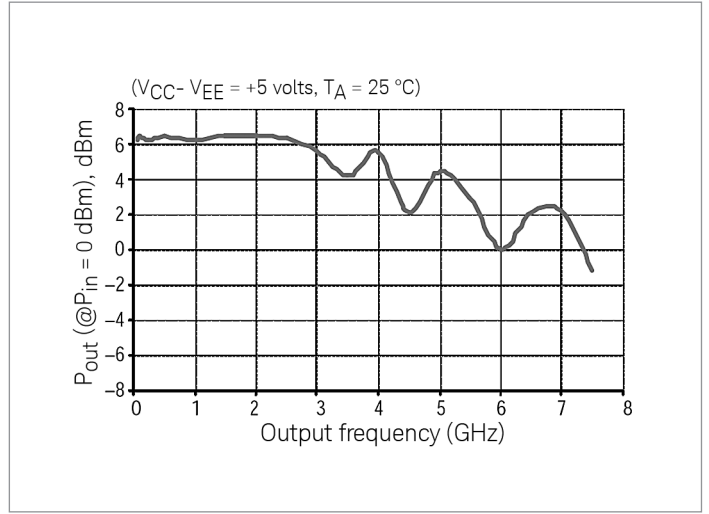


Figure 7. Typical output power vs. output frequency, f_{out} (GHz)

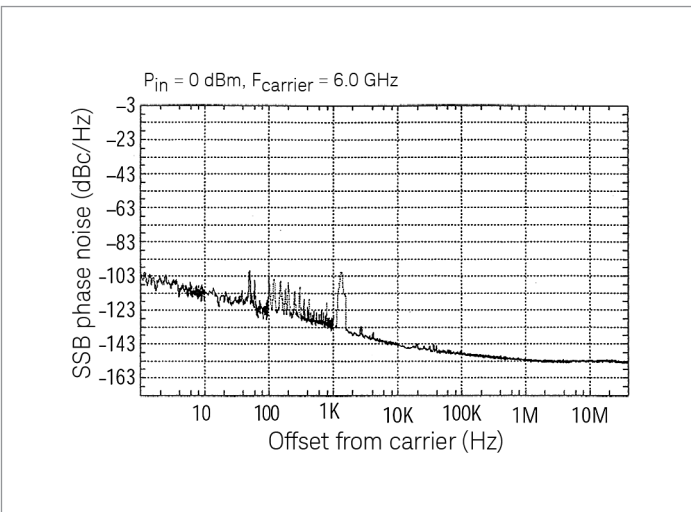


Figure 8. Typical phase noise performance

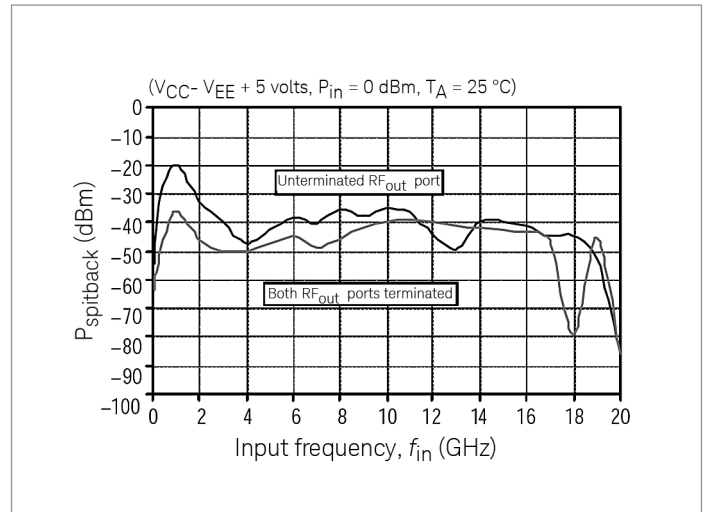
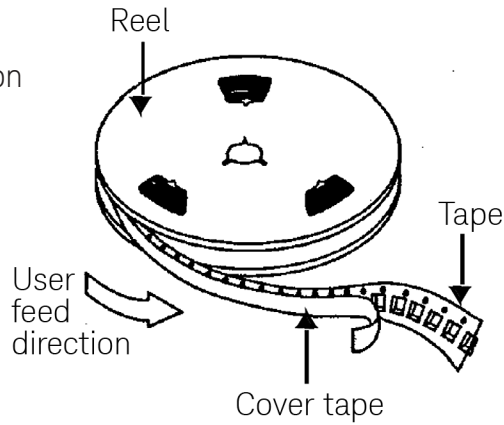


Figure 9. Typical HMMC-3102 "Spitback" power $P(f_{out})$ appearing at RF input port

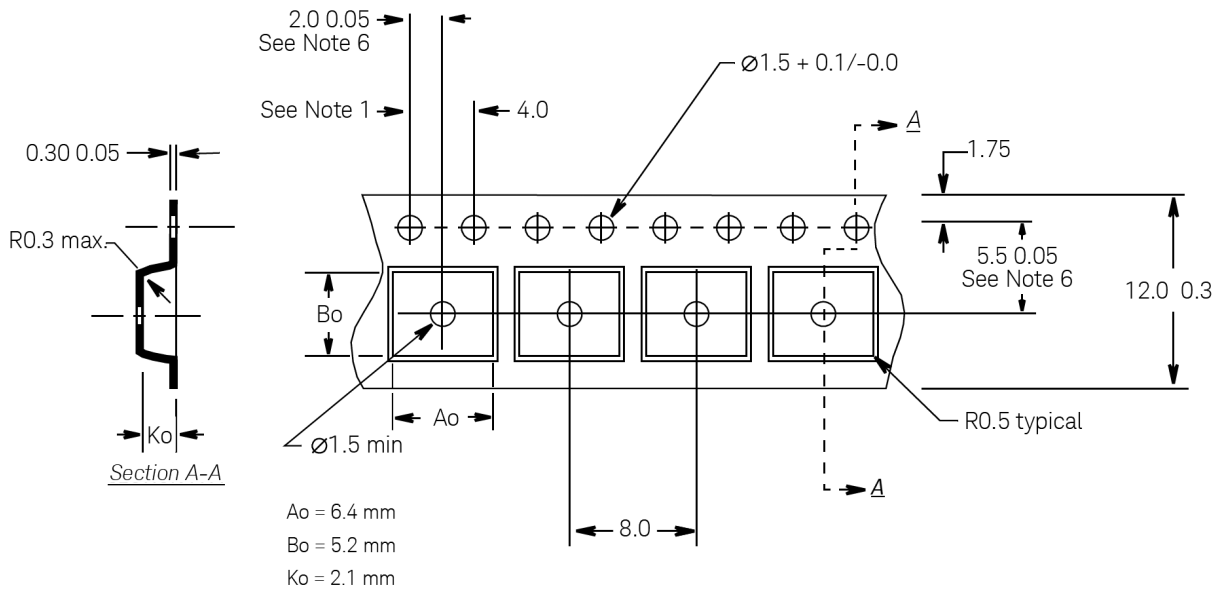
Device orientation



Notes

1. 10 sprocket hole pitch cumulative tolerance: 0.2 mm.
2. Camber not to exceed 1 mm in 100 mm.
3. Material: Black Conductive Advantek Polystyrene.
4. A_o and B_o measured on a plane 0.3 mm above the bottom of the pocket.
5. K_o measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Tape dimensions and product orientation



This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. Customers considering the use of this, or other Keysight Technologies GaAs ICs, for their design should obtain the current production specifications from Keysight. In this data sheet the term typical refers to the 50th percentile performance. For additional information contact Keysight at MMIC_Helpline@keysight.com.

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