

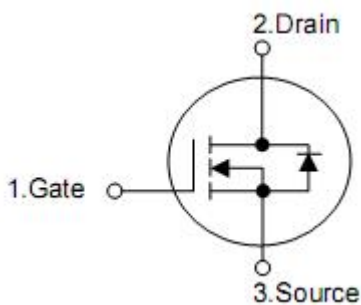
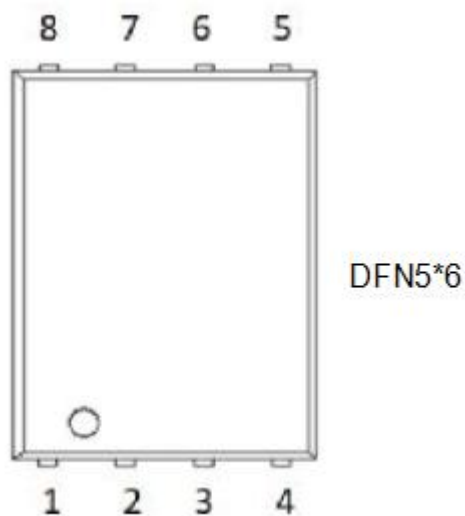
## 1. Features

- n  $R_{DS(on)}=1.5m\Omega(\text{typ.})@ V_{GS}=10V$
- n Advanced Trench Technology
- n Low Gate Charge
- n High Current Capability
- n RoHS and Halogen-Free Compliant

## 2. Description

- n SMPS Synchronous Rectification
- n DC/DC Converters
- n Or-ing

## 3. Symbol



Pin	Function
4	Gate
5,6,7,8	Drain
1,2,3	Source

#### 4. Ordering Information

Part Number	Package	Brand
KCY3104S	DFN5*6	KIA

#### 5. Absolute maximum ratings

Parameter	Symbol	Rating	Units
Drain-source voltage	$V_{DS}$	40	V
Gate-source voltage	$V_{GS}$	$\pm 20$	V
Continuous drain current $V_{GS}@10V^{1,6}$	$I_D$	$T_C=25^\circ C$	110
		$T_C=100^\circ C$	93
Pulsed drain current <sup>2</sup>	$I_{DM}$	400	A
Single pulse avalanche energy <sup>3</sup>	EAS	400	mJ
Avalanche current	$I_{AS}$	40	A
Total power dissipation <sup>4</sup>	$P_D$	125	W
Junction and storage temperature range	$T_J, T_{STG}$	-55 to 150	$^\circ C$

#### 6. Thermal Data

Parameter	Symbol	Ratings	Units
Thermal resistance, junction-ambient <sup>1</sup>	$R_{\theta JA}$	50	$^\circ C/W$
Thermal resistance, Junction-case <sup>1</sup>	$R_{\theta Jc}$	1	

## 7. Electrical characteristics

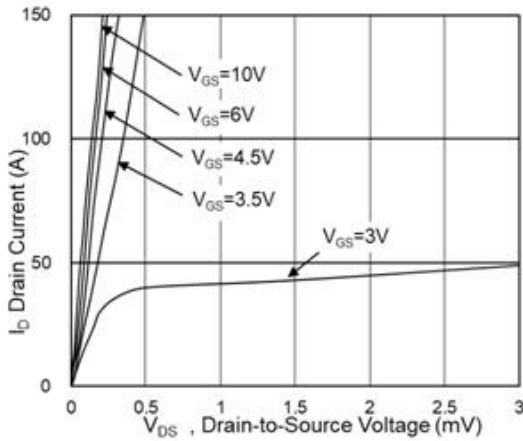
(T<sub>J</sub>=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source breakdown voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	40	-	-	V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =32V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	-	-	1	μA
		V <sub>DS</sub> =32V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	-	-	5	
Gate-source leakage current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Gate threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.6	2.5	V
Static drain-source on- resistance <sup>2</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	1.5	2.0	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A	-	2.0	2.8	
Forward transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =20A	-	50	-	S
Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V F=1MHZ	-	1.0	-	Ω
Total gate charge(4.5V)	Q <sub>g</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =10V I <sub>D</sub> =20A	-	45	-	nC
Gate-source charge	Q <sub>gs</sub>		-	12	-	
Gate-drain charge	Q <sub>gd</sub>		-	18	-	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> =15V, R <sub>G</sub> =3.3Ω, V <sub>GS</sub> =10V I <sub>D</sub> =20A	-	19	-	ns
Rise time	t <sub>r</sub>		-	10	-	
Turn-off delay time	t <sub>d(off)</sub>		-	58	-	
Fall time	t <sub>f</sub>		-	32	-	
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =20V F=1.0MHZ	-	3950	-	pF
Output capacitance	C <sub>oss</sub>		-	1100	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	80	-	
Diode characteristics						
Continuous source current <sup>1,6</sup>	I <sub>S</sub>	V <sub>G</sub> =V <sub>D</sub> =0V, Force current	-	-	110	A
Diode forward voltage <sup>2</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =1A, T <sub>J</sub> =25°C	-	-	1.4	V

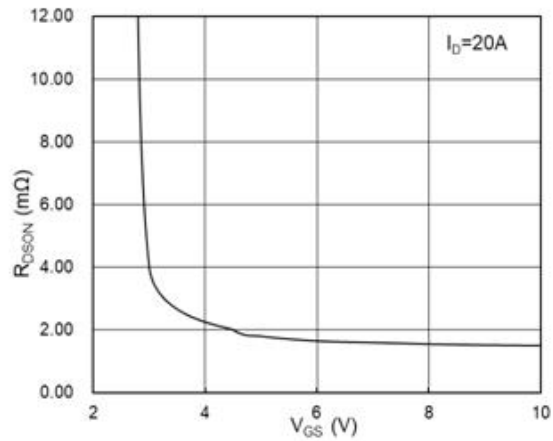
Note :

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width ≅ 300us , duty cycle ≅ 2%
3. The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=25V, V<sub>GS</sub>=10V, L=0.5mH, I<sub>AS</sub>=40A
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.
6. Package limitation current is 100A.

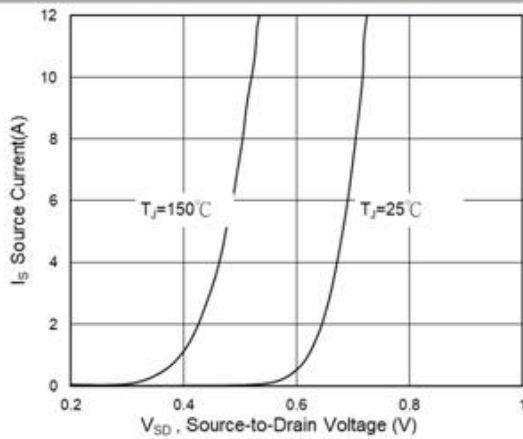
**8. Test circuits and waveforms**



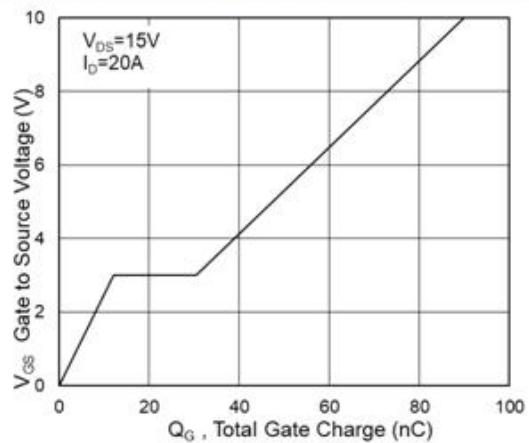
**Fig.1 Typical Output Characteristics**



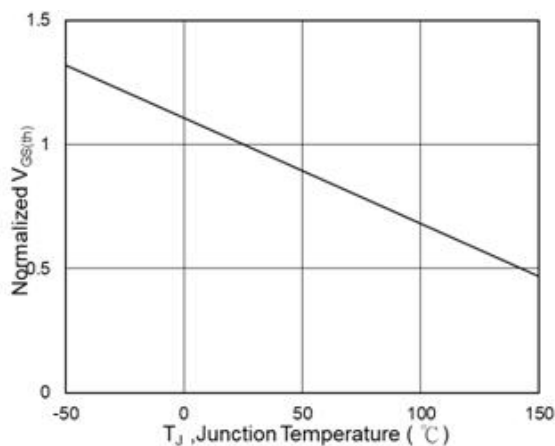
**Fig.2 On-Resistance vs G-S Voltage**



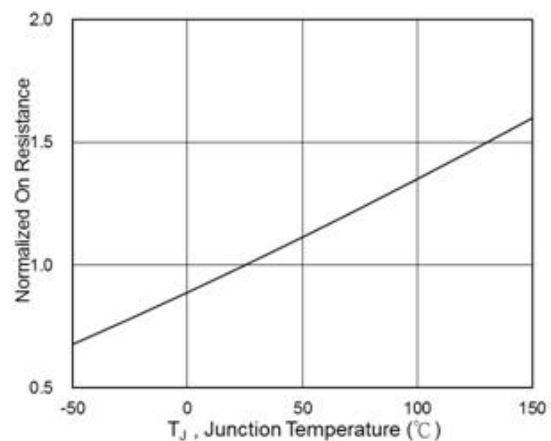
**Fig.3 Source Drain Forward Characteristics**



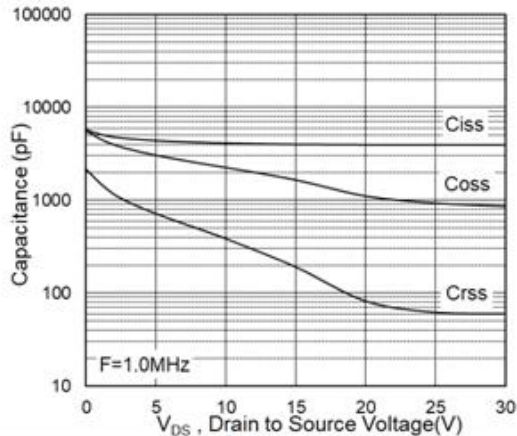
**Fig.4 Gate-Charge Characteristics**



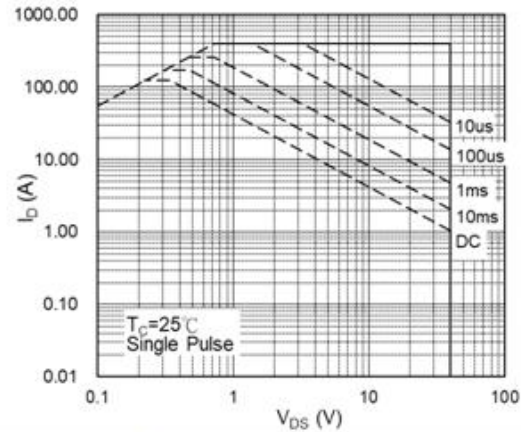
**Fig.5 Normalized  $V_{GS(th)}$  vs  $T_J$**



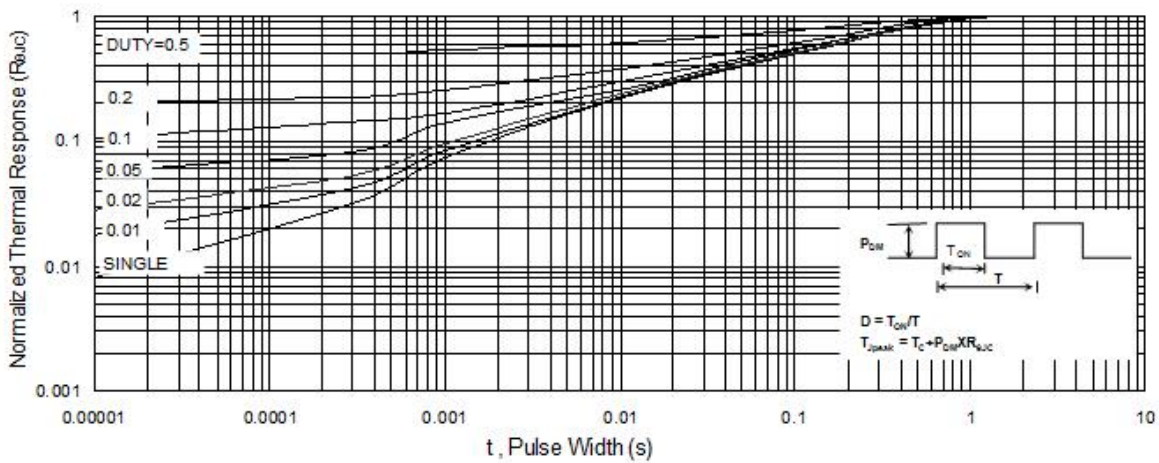
**Fig.6 Normalized  $R_{DS(on)}$  vs  $T_J$**



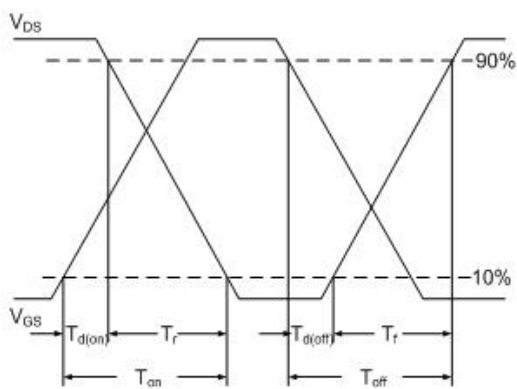
**Fig.7 Capacitance**



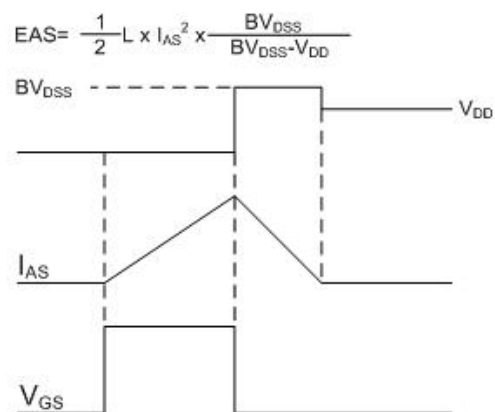
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**

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