

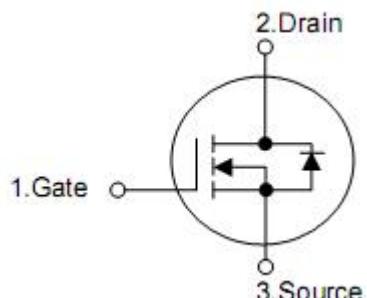
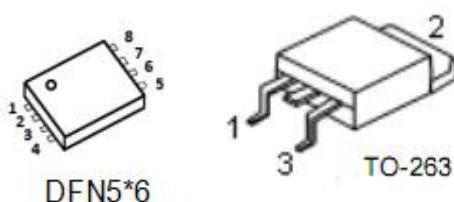
1. Features

- Low RDS(on) & FOM
- Extremely low switching loss
- Uses advanced SGT technology
- Excellent stability and uniformity
- Fast switching and soft recovery

2. Features

- Power switching application
- Low On-Resistance (typ.) RDS(on)=5.0mΩ
- Hard switched and high frequency circuits
- Uninterruptible power supply

3. Pin configuration



Pin DFN5*6	Pin TO-263	Function
4	1	Gate
5,6,7,8	2	Drain
1,2,3	3	Source

4. Ordering Information

Part Number	Package	Brand
KCB3310A	TO-263	KIA
KCY3310A	DFN5*6	KIA

5. Absolute maximum ratings

TC=25 °C unless otherwise specified

Parameter	Symbol	Ratings		Unit
		TO-263	DFN5*6	
Drain-to-Source Voltage	V _{DSS}	100		V
Continuous Drain Current	T _C =25 °C	I _D	90	A
	T _C =100 °C		57	
Pulsed drain current ^(note1)	I _{DM}	360	340	
Avalanche energy ^(note2)	E _{AS}	529		mJ
Gate-Source voltage	V _{GS}	±20		V
Power dissipation ^(note3)	T _C =25 °C	P _D	166	W
	T _C =100 °C		66.4	
Junction & Storage Temperature Range	T _J & T _{STG}	-55 to 150		°C

6. Thermal characteristics

Parameter	Symbol	Ratings		Units
		TO-263	DFN5*6	
Thermal resistance, junction-ambient ^(note4)	t≤10S	R _{θJA}	15	°C/W
Thermal resistance, junction-ambient ^(note4)	Steady-State		60	
Thermal resistance, Junction-case	Steady-State		0.75	
			1.38	

7. Electrical characteristics

($T_J=25^\circ\text{C}$, unless otherwise notes)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static characteristics						
Drain-source breakdown voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=100\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate threshold voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	2	2.8	4	V
Gate leakage current	I_{GSS}	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=20\text{A}$	-	5.0	5.8	$\text{m}\Omega$
Dynamic characteristics						
Gate Resistance	R_{G}	Frequency=1MHz, open drain	-	0.9	-	Ω
Input capacitance	C_{iss}	$V_{\text{DS}}=50\text{V}, V_{\text{GS}}=0\text{V}, F=1\text{MHz}$	-	4600	-	pF
Output capacitance	C_{oss}		-	1250	-	pF
Reverse transfer capacitance	C_{rss}		-	43	-	pF
Turn-on delay time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}}=50\text{V}, I_{\text{D}}=20\text{A}, V_{\text{GS}}=10\text{V}, R_{\text{G}}=2.2\Omega$	-	17.6	-	ns
Rise time	t_r		-	30.2	-	ns
Turn-off delay time	$t_{\text{d}(\text{off})}$		-	33.6	-	ns
Fall time	t_f		-	39.6	-	ns
Gate Charge Characteristics						
Total gate charge	Q_g	$V_{\text{DS}}=50\text{V}, I_{\text{D}}=20\text{A}, V_{\text{GS}}=10\text{V}, F=1\text{MHz}$	-	66	-	nC
Gate-source charge	Q_{gs}		-	23	-	nC
Gate-drain charge	Q_{gd}		-	6.6	-	nC
Diode characteristics						
Diode forward voltage	V_{SD}	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=20\text{A}$	-	-	1.3	V
Body Diode Continuous Forward Current	I_{S}		-	-	90	A
Reverse recovery time	t_{rr}	$I_F=20\text{A}$ $DI_F/dt=100\text{A}/\mu\text{s}$	-	65	-	ns
Reverse recovery charge	Q_{rr}		-	90	-	nC

NOTE:

1. Repetitive rating; pulse width limited by max. junction temperature.
2. $V_{\text{DD}}=50\text{V}, R_{\text{G}}=25\Omega, L=0.5\text{mH}, I_{\text{AS}}=46\text{A}$.
3. P_d is based on max. junction temperature, using junction-case thermal resistance.
4. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with $TA = 25^\circ\text{C}$. The Power dissipation PDSM is based on $R_{\theta JA} \leq 10\text{s}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.

8. Typical Characteristics

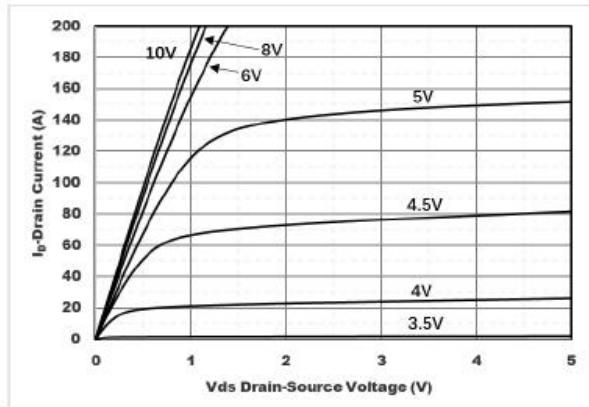


Figure1. Output Characteristics

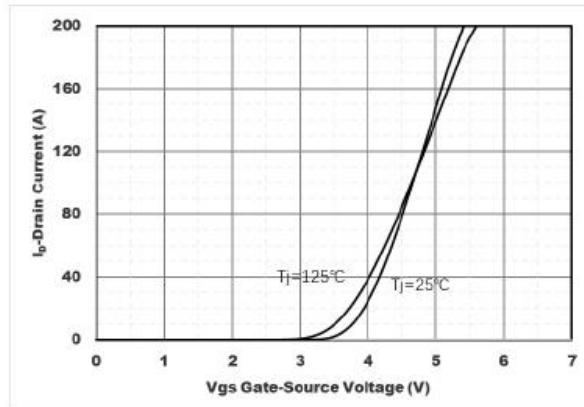


Figure2. Transfer Characteristics

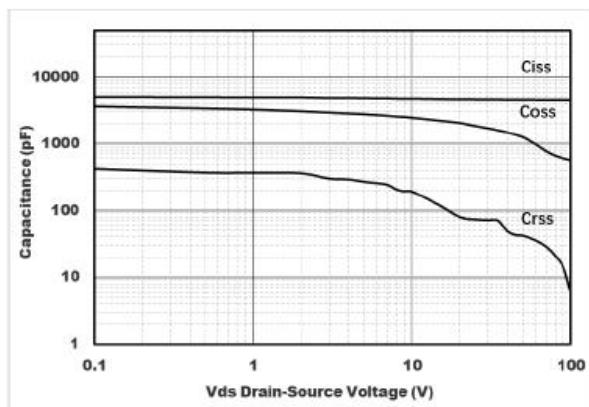


Figure3. Capacitance Characteristics

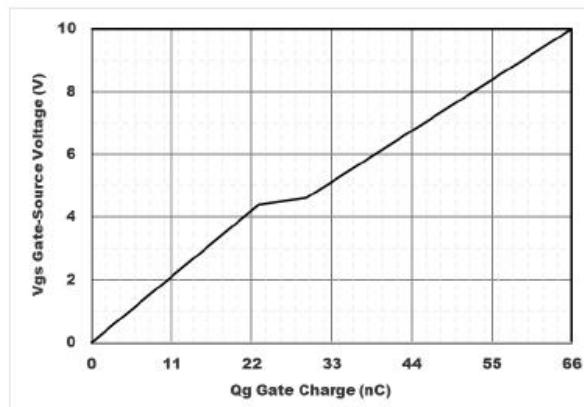


Figure4. Gate Charge

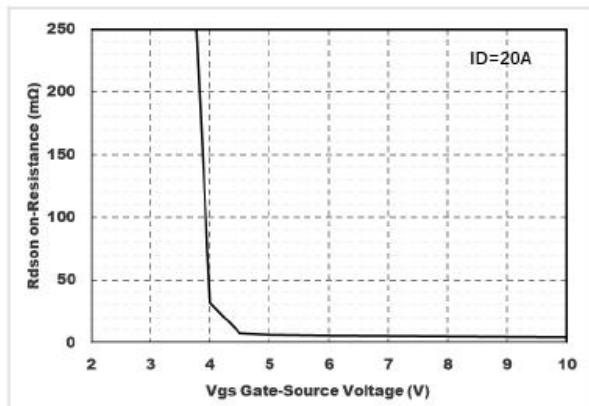


Figure5. : On-Resistance vs. Drain Current and Gate Voltage

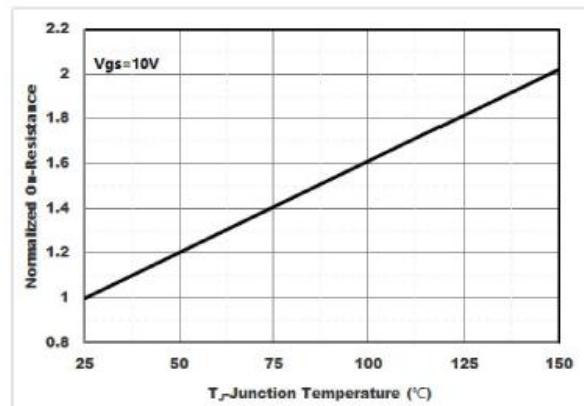


Figure6. Normalized On-Resistance

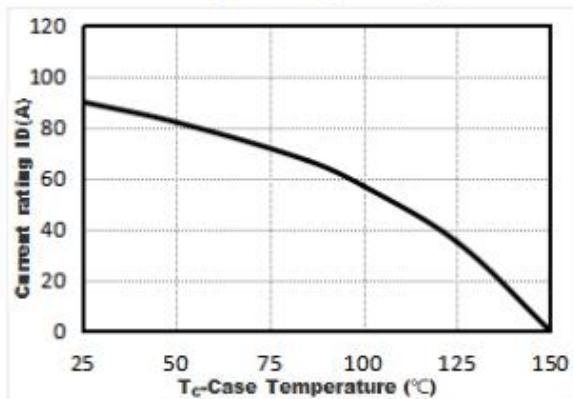
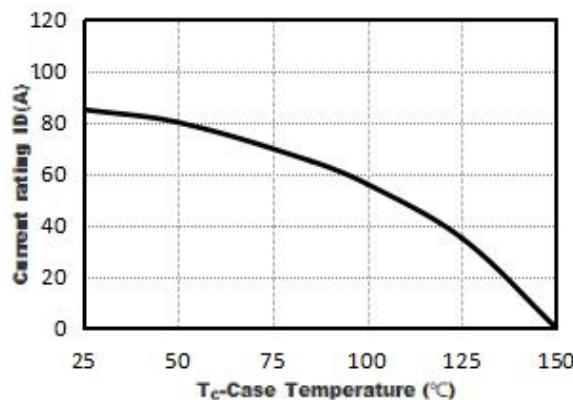


Figure7. Drain current

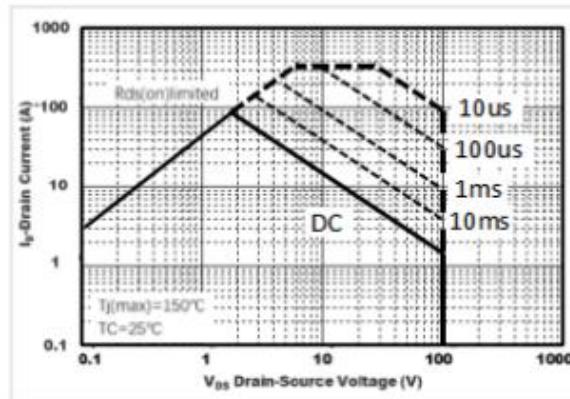
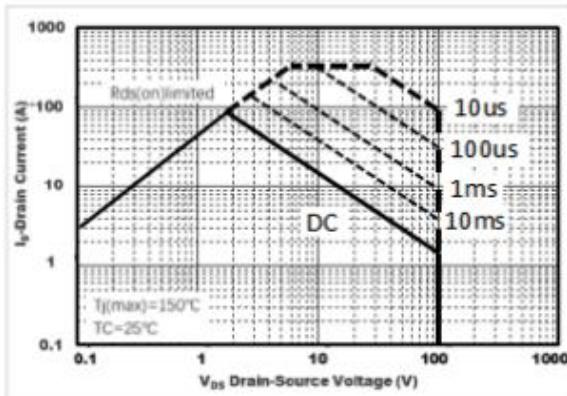


Figure8.Safe Operation Area

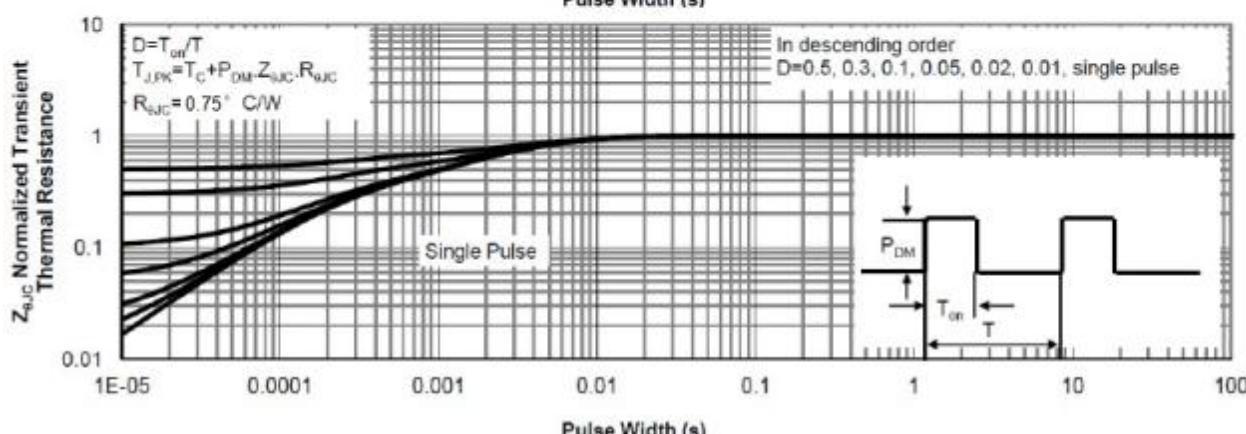
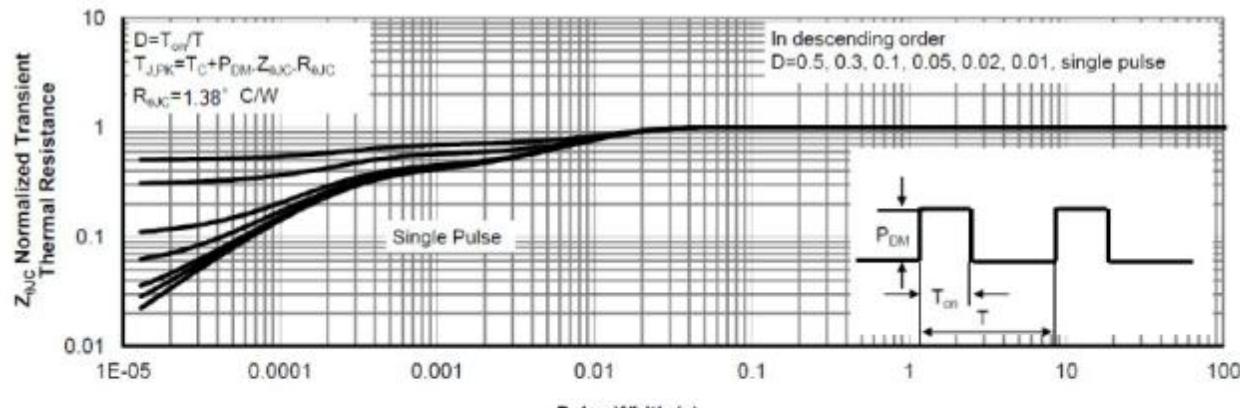


Figure9.Normalized Maximum Transient thermal impedance

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