

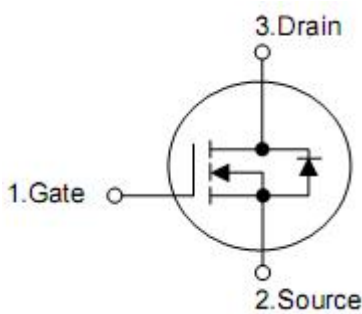
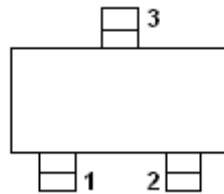
1. Description

The KIA3414 uses advanced trench technology to provide excellent $R_{DS(on)}$, low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch or in PWM applications. Standard Product KIA3414 is Pb-free (meets ROHS & Sony 259 specifications). KIA3414 is a Green Product ordering option. KIA3414 is electrically identical.

2. Features

- n $V_{DS}(V)=20V$
- n $I_D=4.2A$
- n $R_{DS(on)}<50m\Omega(V_{GS}=4.5V, I_D=4.2A)$
- n $R_{DS(on)}<63m\Omega(V_{GS}=2.5V, I_D=3.7A)$

3. Symbol



Pin	Function
1	Gate
2	Source
3	Drain

4. Absolute maximum ratings

($T_A=25^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Rating	Units
Drain-source voltage	V_{DS}	20	V
Gate-source voltage	V_{GS}	± 12	V
Continuous drain current ^A	I_D	$T_A=25^{\circ}\text{C}$	4.2
		$T_A=70^{\circ}\text{C}$	3.2
Pulsed drain current ^B	I_{DM}	15	A
Total power dissipation ^A	P_D	$T_A=25^{\circ}\text{C}$	1.4
		$T_A=70^{\circ}\text{C}$	0.9
Junction and storage temperature range	T_J, T_{STG}	-55 to 150	$^{\circ}\text{C}$

5. Thermal characteristics

Parameter	Symbol	Typ	Max	Unit
Maximum junction-ambient ^A ($t \leq 10\text{s}$)	$R_{\theta JA}$	70	90	$^{\circ}\text{C/W}$
Maximum junction-ambient ^A	$R_{\theta JA}$	100	125	$^{\circ}\text{C/W}$
Maximum junction-Lead ^C	$R_{\theta JL}$	63	80	$^{\circ}\text{C/W}$

6. Electrical characteristics

($T_A=25^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
Zero gate voltage drain current	I_{DSS}	$V_{DS}=16V, V_{GS}=0V$	-	-	1	μA
Gate- body leakage current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	100	nA
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.4	0.6	1	V
On state drain current	$I_{D(on)}$	$V_{GS}=4.5V, V_{DS}=5V$	15	-	-	A
Static drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=4.2A$	-	41	50	m Ω
		$V_{GS}=2.5V, I_D=3.7A$	-	52	63	
Forward transconductance	g_{fs}	$V_{DS}=5.0V, I_D=4.2A$	-	8.0	-	S
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_S=1A$	-	0.76	1.2	V
Maximum body-diode continuous current	I_S		-	-	2	A
Input capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V,$ $f=1\text{MHz}$	-	436	-	pF
Output capacitance	C_{oss}		-	66	-	
Reverse transfer capacitance	C_{rss}		-	44	-	
Gate resistance	R_g	$V_{DS}=0V,$ $V_{GS}=0V, f=1\text{MHz}$	-	3	-	Ω
Total gate charge	Q_g	$V_{DS}=10V, V_{GS}=4.5V$ $I_D=4.2A$	-	6.2	-	nC
Gate-source charge	Q_{gs}		-	1.6	-	
Gate-drain charge	Q_{gd}		-	0.5	-	
Turn-on delay time	$t_{d(on)}$	$V_{DS}=10V, R_L=2.7\Omega,$ $R_G=6\Omega, V_{GS}=5V$	-	5.5	-	ns
Rise time	t_r		-	6.3	-	
Turn-off delay time	$t_{d(off)}$		-	40	-	
Fall time	t_f		-	12.7	-	
Reverse recovery time	t_{rr}	$I_F=4.0A, di/dt=100A/\mu s,$	-	12.3	-	nS
Reverse recovery charge	Q_{rr}		-	3.5	-	nC

Note: A. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10s$ thermal resistance rating.

B. Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6, 12, 14 are obtained using 80 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The SOA curve provides a single pulse rating.

7. Test circuits and waveforms

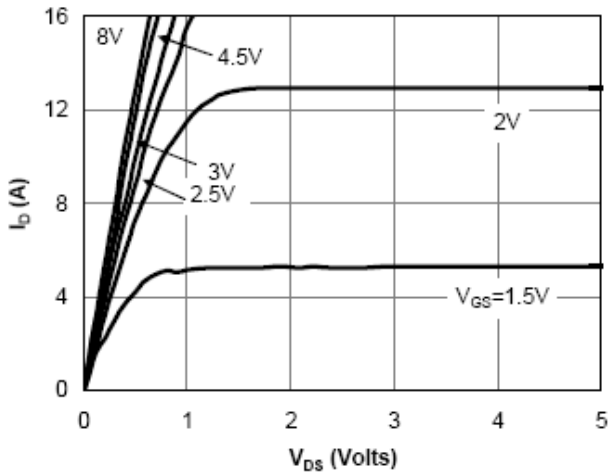


Fig 1: On-Region Characteristics

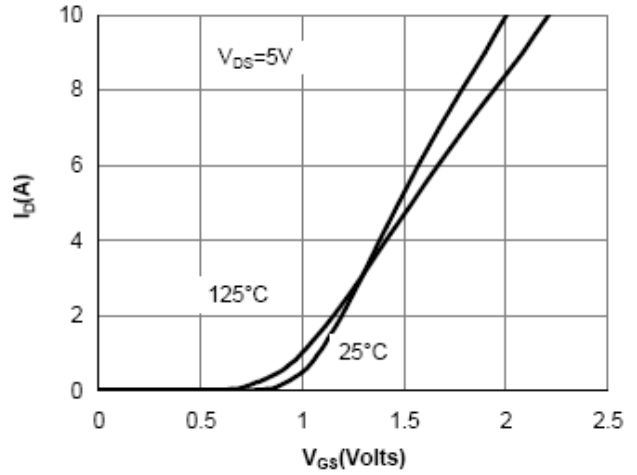


Figure 2: Transfer Characteristics

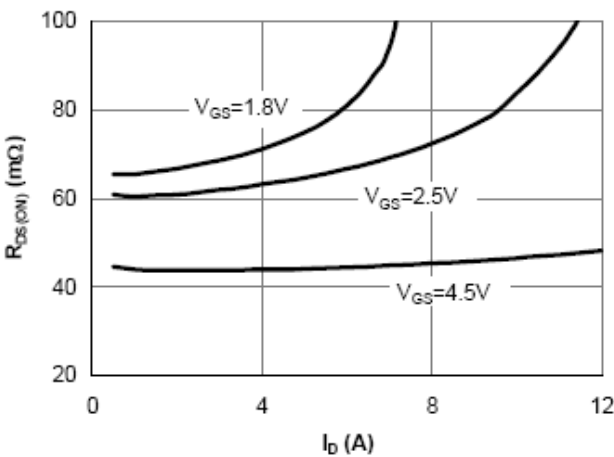


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

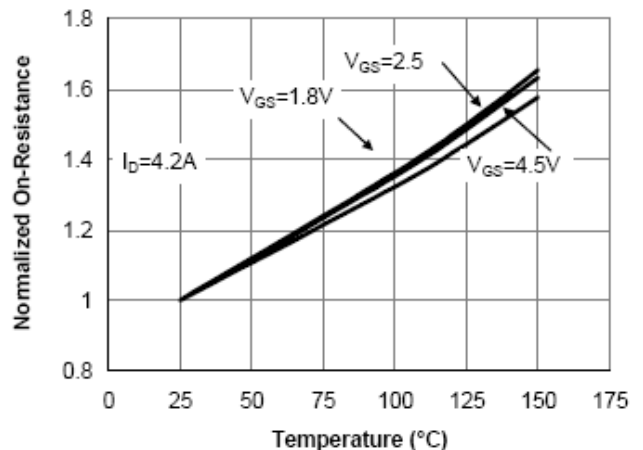


Figure 4: On-Resistance vs. Junction Temperature

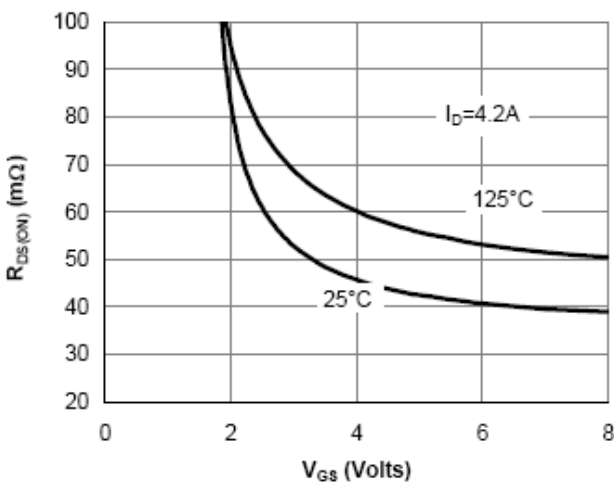


Figure 5: On-Resistance vs. Gate-Source Voltage

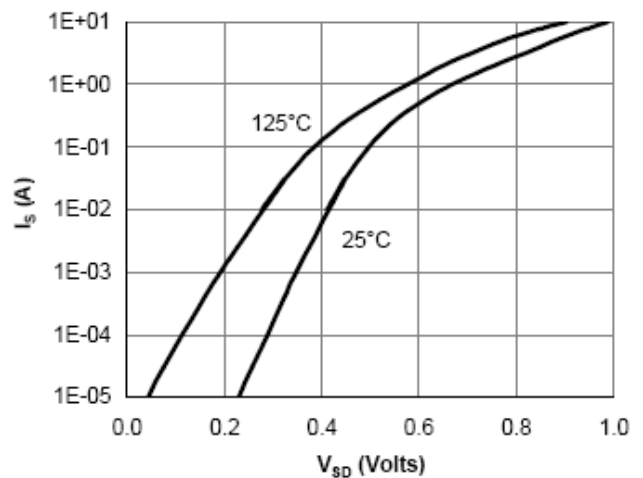


Figure 6: Body-Diode Characteristics

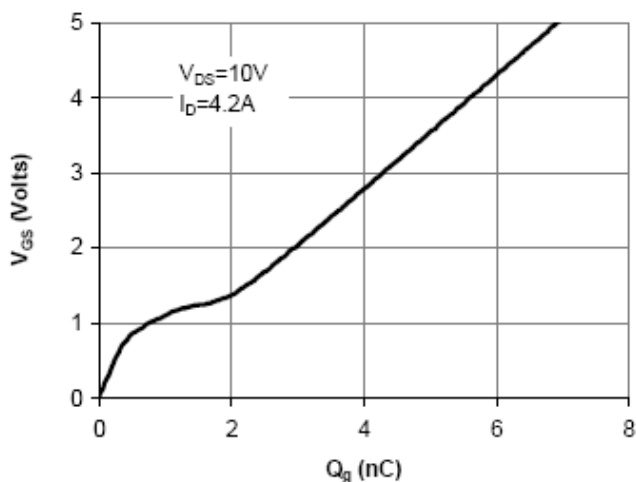


Figure 7: Gate-Charge Characteristics

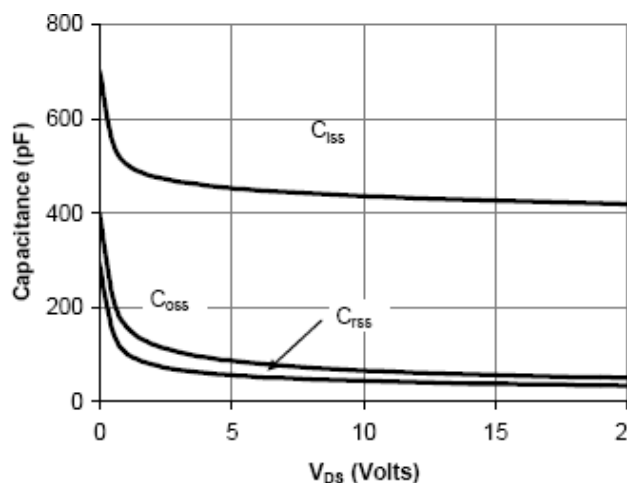


Figure 8: Capacitance Characteristics

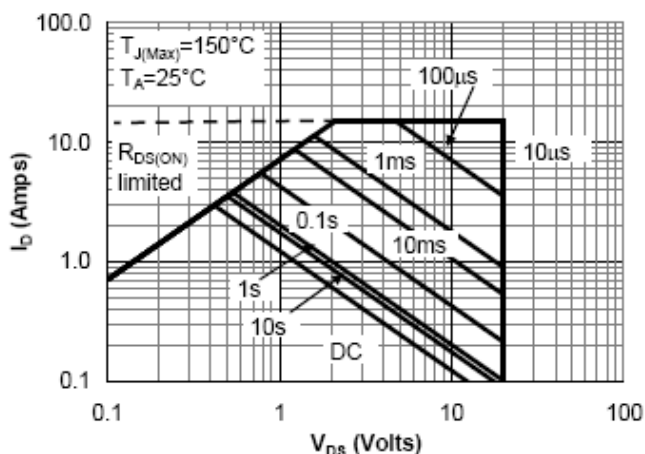


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

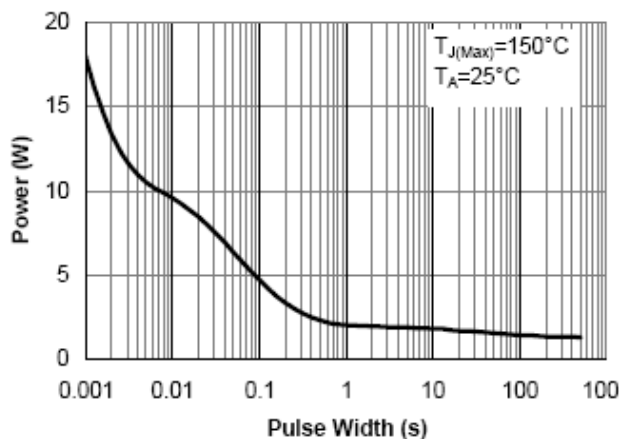


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

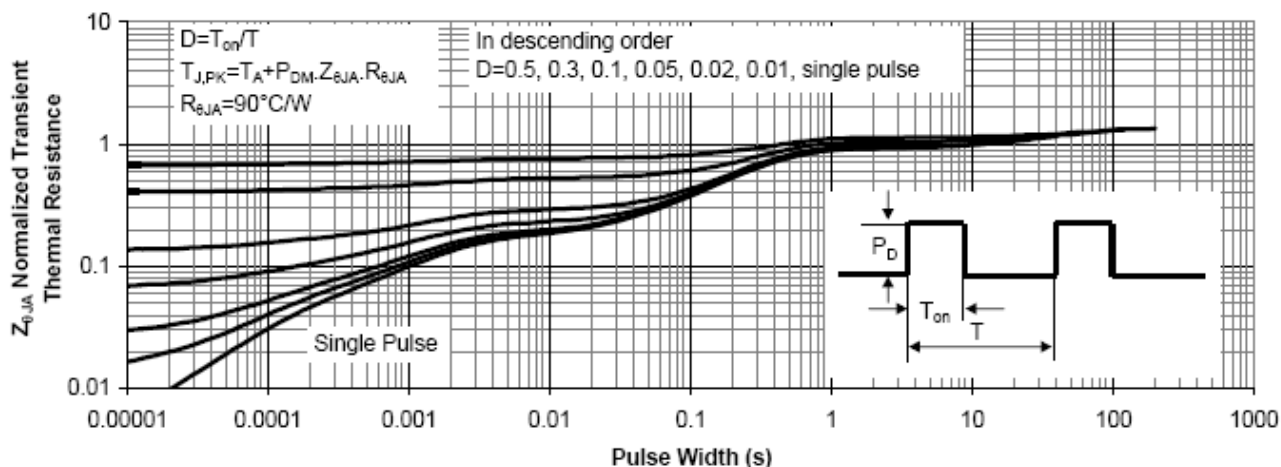


Figure 11: Normalized Maximum Transient Thermal Impedance

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