

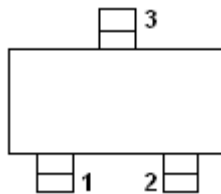
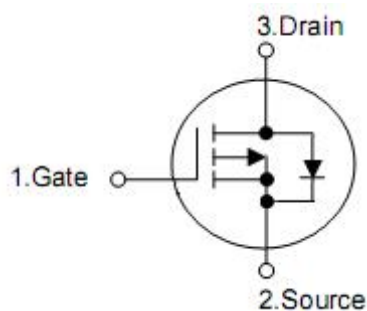
1. Description

The KIA3415 uses advanced trench technology to provide excellent $R_{DS(on)}$, low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch or in PWM applications. Standard Product KIA3415 is Pb-free (meets ROHS & Sony 259 specifications). KIA3415 is a Green Product ordering option. KIA3415 is electrically identical.

2. Features

- n $V_{DS}(V) = -16V$
- n $I_D = -4.0A$
- n $R_{DS(on)} < 45m\Omega (V_{GS} = -4.5V, I_D = -4.0A)$
- n $R_{DS(on)} < 54m\Omega (V_{GS} = -2.5V, I_D = -2.5A)$
- n $R_{DS(on)} < 75m\Omega (V_{GS} = -1.8V, I_D = -2.0A)$

3. Symbol



Pin	Function
1	Gate
2	Source
3	Drain

4. Absolute maximum ratings

(T_A=25°C, unless otherwise noted)

Parameter	Symbol	Rating	Units
Drain-source voltage	V _{DS}	-16	V
Gate-source voltage	V _{GS}	±8	V
Continuous drain current ^A	I _D	T _A =25°C	-4.0
		T _A =70°C	-3.5
Pulsed drain current ^B	I _{DM}	-30	A
Total power dissipation ^A	P _D	T _A =25 °C	1.4
		T _A =70°C	0.9
Junction and storage temperature range	T _J , T _{STG}	-55 to 150	°C

5. Thermal characteristics

Parameter	Symbol	Typ	Max	Unit
Maximum junction-ambient ^A (t≤10s)	R _{θJA}	65	90	°C/W
Maximum junction-ambient ^A	R _{θJA}	85	125	°C/W
Maximum junction-Lead ^C	R _{θJL}	43	60	°C/W

6. Electrical characteristics

(T_A=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-16	-	-	V
Zero gate voltage drain current	I _{DSS}	V _{DS} =-12V, V _{GS} =0V	-	-	-50	nA
Gate- body leakage current	I _{GSS}	V _{GS} =±8V, V _{DS} =0V	-	-	±100	nA
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-0.4	-0.55	-0.8	V
On state drain current	I _{D(on)}	V _{GS} =-4.5V, V _{DS} =-5V	-25	-	-	A
Static drain-source on-resistance	R _{DS(on)}	V _{GS} =-4.5V, I _D =-4.0A	-	40	45	mΩ
		V _{GS} =-2.5V, I _D =-2.5A	-	50	54	
		V _{GS} =-1.8V, I _D =-2.0A	-	70	75	
Forward transconductance	g _{fs}	V _{DS} =-5.0V, I _D =-4A	8	16	-	S
Diode forward voltage	V _{SD}	V _{GS} =0V, I _S =-1A	-	-0.78	-1.28	V
Maximum body-diode continuous current	I _S		-	-	-2.2	A
Input capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V, f=1MHz	-	1450	-	pF
Output capacitance	C _{oss}		-	205	-	
Reverse transfer capacitance	C _{rss}		-	160	-	
Gate resistance	R _g	V _{DS} =0V, V _{GS} =0V, f=1MHz	-	6.5	-	Ω
Total gate charge	Q _g	V _{DS} =-10V, V _{GS} =-4.5V I _D =-4.0A	-	17.2	-	nC
Gate-source charge	Q _{gs}		-	1.3	-	
Gate-drain charge	Q _{gd}		-	4.5	-	
Turn-on delay time	t _{d(on)}	V _{DS} =-10V, R _L =2.5Ω,, R _G =3Ω, V _{GS} =-4.5V	-	9.5	-	ns
Rise time	t _r		-	17	-	
Turn-off delay time	t _{d(off)}		-	94	-	
Fall time	t _f		-	35	-	
Reverse recovery time	t _{rr}	I _F =-4A, dI/dt=100A/μs,	-	31	-	nS
Reverse recovery charge	Q _{rr}		-	13.8	-	nC

Note: A. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t_{≤10s} thermal resistance rating.

B. Repetitive rating, pulse width limited by junction temperature.

C. The R_{θJA} the sum of the thermal impedance from junction to lead R_{θJA} and lead to ambient.

D. The static characteristics in Figures 1 to 6, 12, 14 are obtained using 80μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

7. Test circuits and waveforms

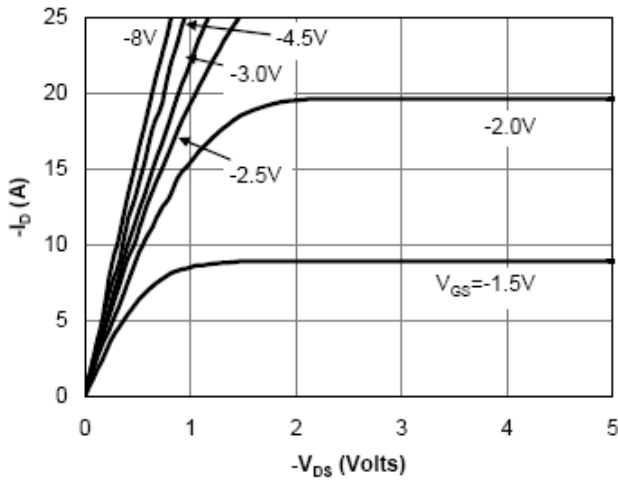


Fig 1: On-Region Characteristics

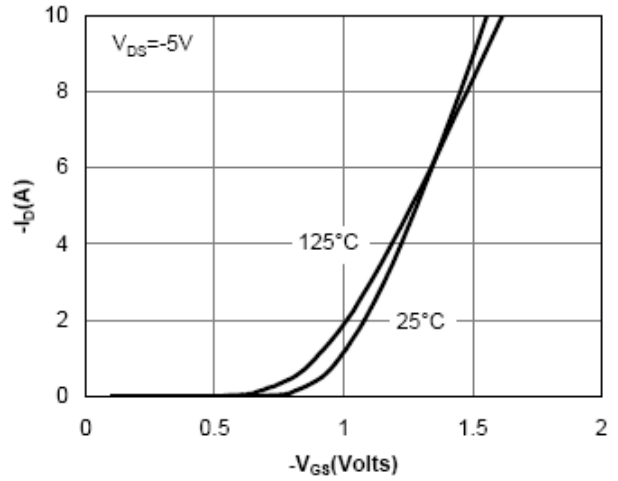


Figure 2: Transfer Characteristics

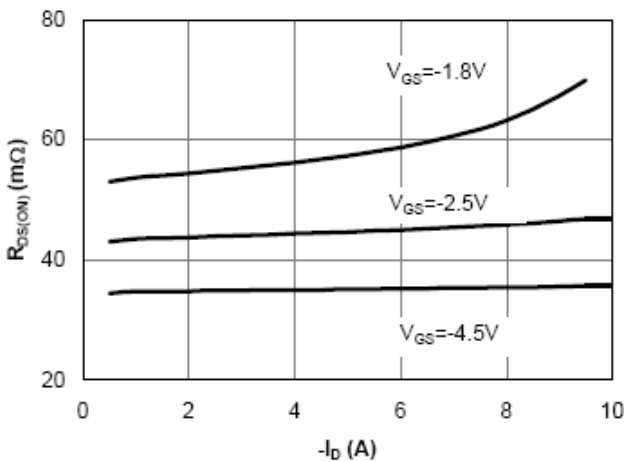


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

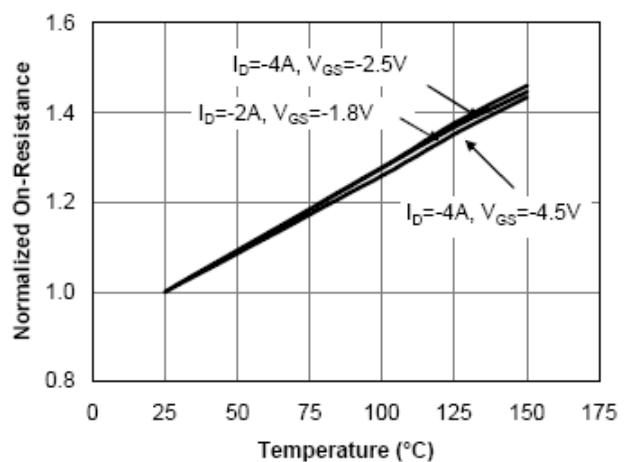


Figure 4: On-Resistance vs. Junction Temperature

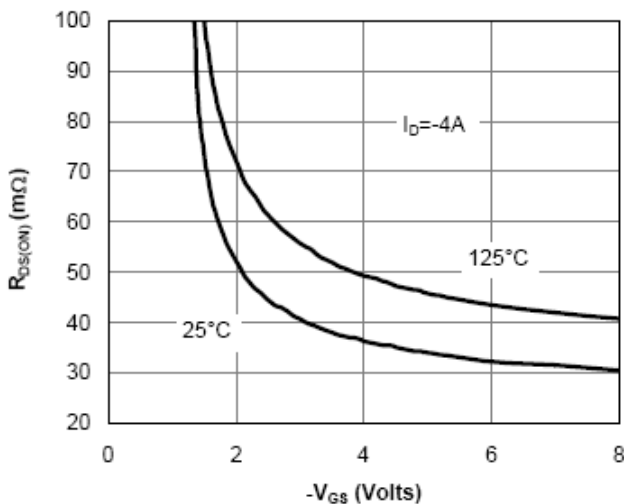


Figure 5: On-Resistance vs. Gate-Source Voltage

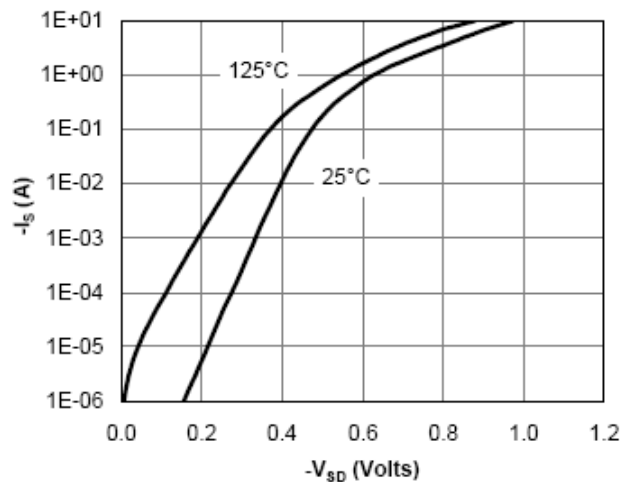


Figure 6: Body-Diode Characteristics

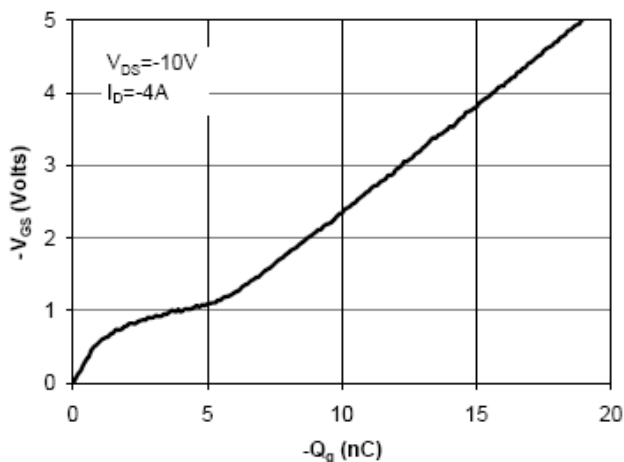


Figure 7: Gate-Charge Characteristics

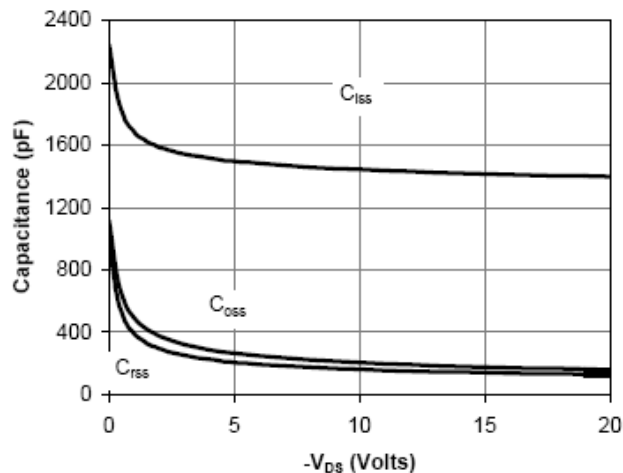


Figure 8: Capacitance Characteristics

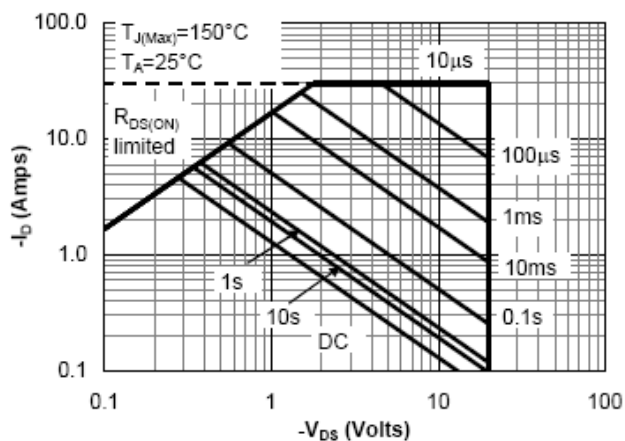


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

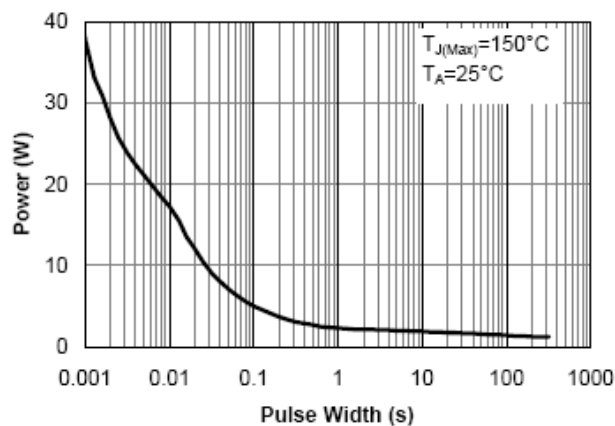


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

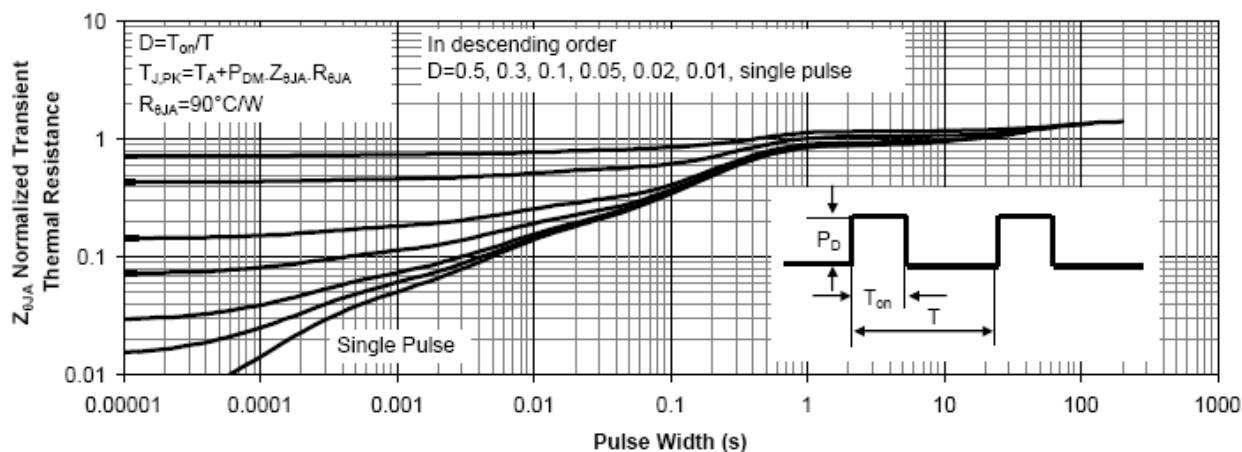


Figure 11: Normalized Maximum Transient Thermal Impedance

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