

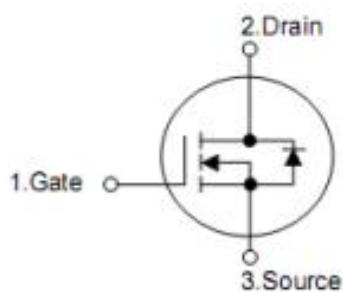
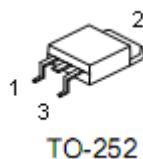
1. Features

- $R_{DS(on)}=1.25\Omega(\text{typ})$ @ $V_{GS}=10V$
- RoHS compliant
- Low on resistance
- Low gate charge
- Peak current vs pulse width curve

2. Applications

- Adaptor
- Charger
- SMPS standby power

3. Symbol



| Pin | Function |
|-----|----------|
| 1 | Gate |
| 2 | Drain |
| 3 | Source |

4. Absolute maximum ratings

| Parameter | Symbol | Rating | Units |
|--|------------------------------------|------------|-------|
| Drain-source voltage (note*1) | V _{DSS} | 500 | V |
| Continuous drain current | I _D | 5.0* | A |
| | I _D @100°C | Figure 3 | A |
| Pulsed drain current, V _{GS} @10V (note*2) | I _{DM} | Figure 6 | A |
| Power dissipation | P _D | 100 | W |
| Derating factor above 25°C | | 0.8 | W/°C |
| Gate-source voltage | V _{GS} | +20 | V |
| Single pulse Avalanche Energy | E _{AS} | 260 | mJ |
| Pulse avalanche rating | I _{AS} | Figure 8 | A |
| Peak diode recovery dv/dt (note*3) | dv/dt | 5.0 | V/ns |
| Maximum temperature for soldering Leads at 0.063 in (1.6mm) from case for 10 seconds package body for 10 seconds | T _L T _{PKG} | 300 260 | °C |
| Operating junction and storage temperature range | T _J , T _{STG} | -55 to150 | °C |

*Drain current limited by maximum junction temperature

Caution: Stresses greater than those listed in the "Absolute maximum ratings" table may cause permanent damage to the device

5. Thermal characteristics

| Parameter | Symbol | Rating | Unit | Test condition |
|------------------|------------------|--------|------|---|
| Junction-ambient | R _{θJA} | 62 | °C/W | 1 cubic foot chamber, free air |
| Junction-case | R _{θJC} | 1.25 | °C/W | Drain lead soldered to water cooled heatsink, P _D adjusted for a peak junction temperature of +150°C |

6. Electrical characteristics

($T_J=25^\circ\text{C}$, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|--|---|-----|------|-----|---------------------------|
| Drain-source breakdown voltage | BV_{DSS} | $V_{\text{GS}}=0\text{V}, I_{\text{DS}}=250\mu\text{A}$ | 500 | - | - | V |
| Breakdown voltage temperature coefficient, Figure 11 | $\Delta \text{BV}_{\text{DSS}}/\Delta T_J$ | Reference to 25°C $I_D=250\mu\text{A}$ | | 0.61 | | $\text{V}/^\circ\text{C}$ |
| Drain-source leakage current | I_{DSS} | $V_{\text{DS}}=500\text{V}, V_{\text{GS}}=0\text{V}$ | - | - | 1 | μA |
| | | $V_{\text{DS}}=400\text{V}, V_{\text{GS}}=0\text{V}$ $T_J=125^\circ\text{C}$ | - | - | 100 | |
| Gate threshold voltage, Figure 12 | $V_{\text{GS}(\text{th})}$ | $V_{\text{DS}}=V_{\text{GS}}, I_D=250\mu\text{A}$ | 2.0 | - | 4.0 | V |
| Gate-source forward leakage | I_{GSS} | $V_{\text{GS}}=20\text{V}$ | - | - | 1 | uA |
| Gate-source reverse leakage | | $V_{\text{GS}}=-20\text{V}$ | - | - | -1 | |
| Static drain-source on-resistance Figure 9 and 10 | $R_{\text{DS}(\text{on})}$ | $V_{\text{GS}}=10\text{V}, I_D=2.5\text{A}$ (note*4) | - | 1.25 | 1.5 | Ω |
| Forward transconductance | g_{fs} | $V_{\text{DS}}=15\text{V}, I_D=2.5\text{A}$ (note*4) | - | 6 | - | S |
| Input capacitance | C_{iss} | $V_{\text{DS}}=25\text{V}, V_{\text{GS}}=0\text{V}$ $f=1\text{MHz}$ Figure 14 | - | 525 | - | pF |
| Output capacitance | C_{oss} | | - | 64 | - | |
| Reverse transfer capacitance | C_{rss} | | - | 12 | - | |
| Turn-on delay time | $t_{\text{d}(\text{on})}$ | $V_{\text{DD}}=250\text{V}, I_D=5\text{A},$ $R_G=12\Omega, V_{\text{GS}}=10\text{V}$ | - | 9.0 | - | ns |
| Rise time | t_r | | - | 11 | - | |
| Turn-off delay time | $t_{\text{d}(\text{off})}$ | | - | 30 | - | |
| Fall time | t_f | | - | 16 | - | |
| Total gate charge | Q_g | $V_{\text{DD}}=250\text{V}, I_D=5\text{A},$ Figure 15 | - | 14 | - | nC |
| Gate-source charge | Q_{gs} | | - | 3.0 | - | |
| Gate-drain charge | Q_{gd} | | - | 6.0 | - | |
| Continuous source current (body diode) | I_s | Integral pn-diode in MOSFET | - | - | 5 | A |
| Maximum pulsed current (body diode) | I_{SM} | | - | - | 20 | |
| Diode forward voltage | V_{SD} | $I_s=5\text{A}, V_{\text{GS}}=0\text{V}$ | - | - | 1.5 | V |
| Reverse recovery time | t_{rr} | $I_F=5\text{A}, V_{\text{GS}}=0\text{V}$ $di/dt=100\text{A}/\mu\text{s}$ | - | 400 | - | nS |
| Reverse recovery charge | Q_{rr} | | - | 1700 | - | nC |

Note: 1. $T_J=25^\circ\text{C}$ to 150°C .

2. Repetitive rating; pulse width limited by maximum junction temperature

3. $I_{\text{SD}}=5\text{A}$ $di/dt \leq 100\text{A}/\mu\text{s}$, $V_{\text{DD}} \leq \text{BV}_{\text{DSS}}$, $T_J=150^\circ\text{C}$.

4. pulse width $\leq 380\text{us}$; duty cycle $\leq 2\%$.

7. Typical operating characteristics

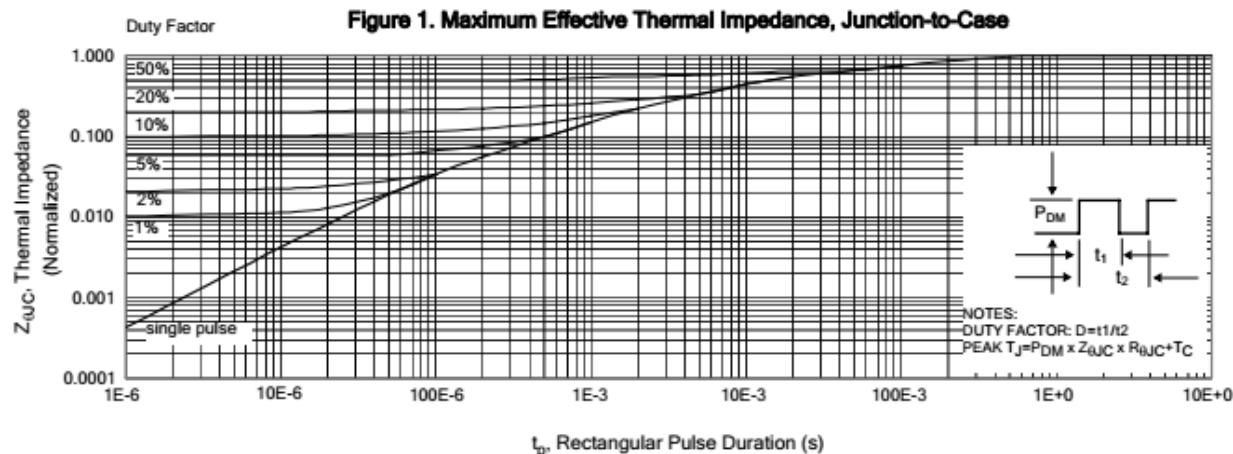


Figure 2. Maximum Power Dissipation vs Case Temperature

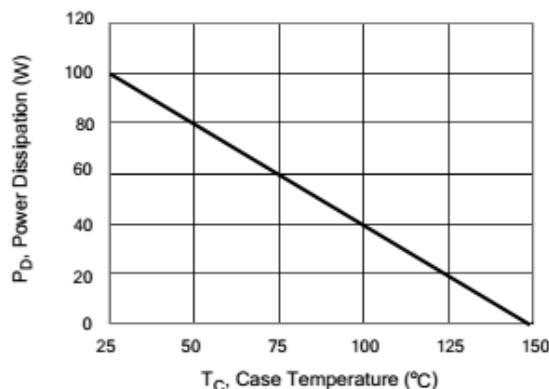


Figure 4. Typical Output Characteristics

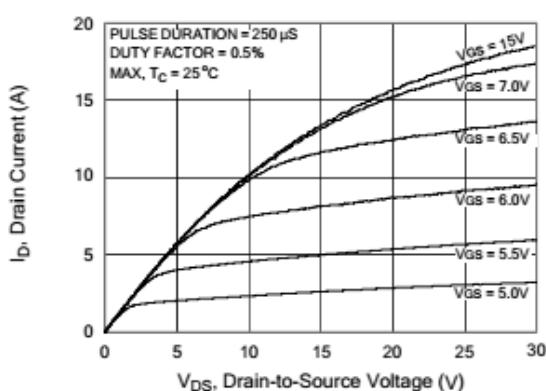


Figure 3. Maximum Continuous Drain Current vs Case Temperature

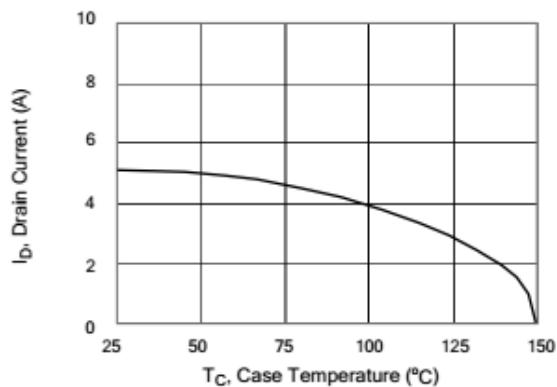


Figure 5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

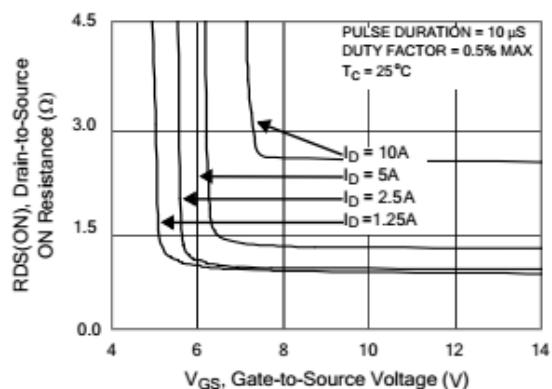


Figure 6. Maximum Peak Current Capability

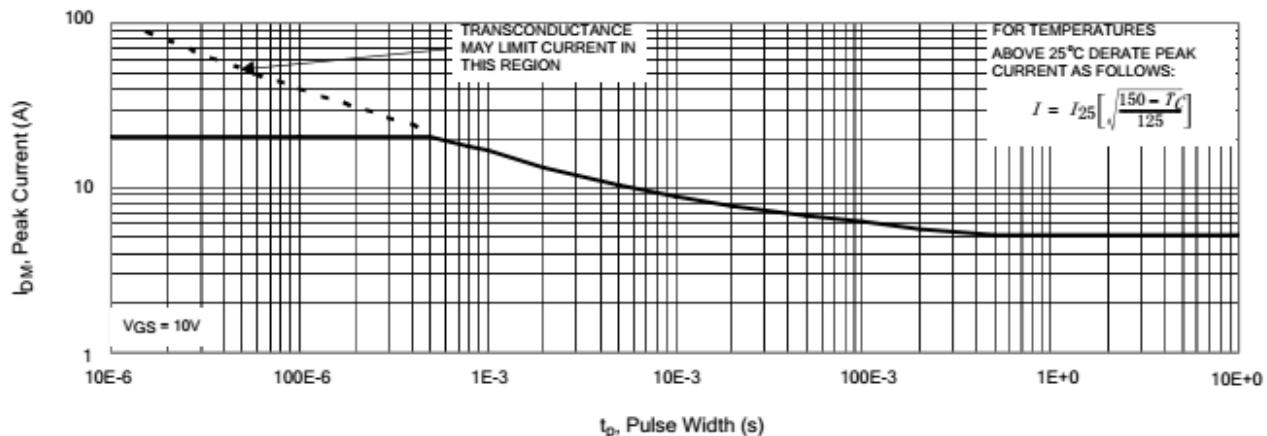


Figure 7. Typical Transfer Characteristics

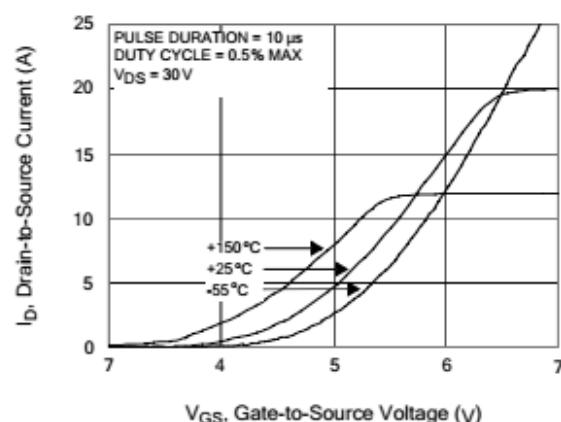


Figure 8. Unclamped Inductive Switching Capability

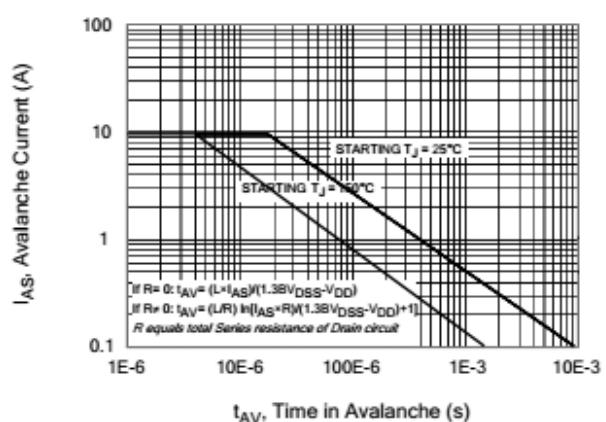


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

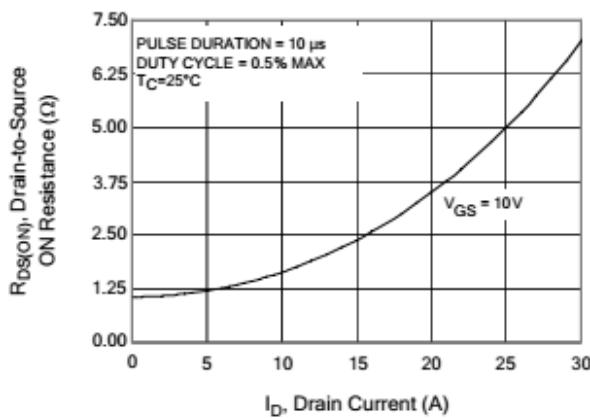


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

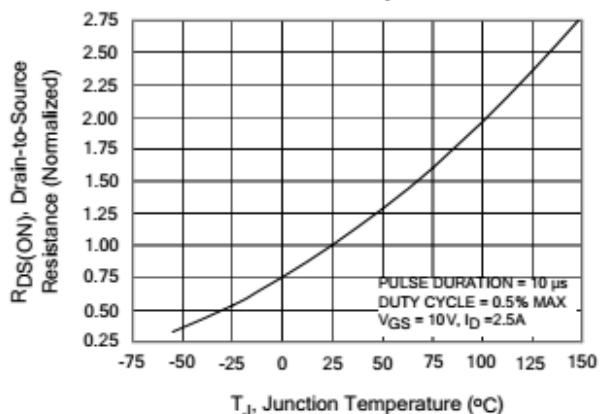


Figure 11. Typical Breakdown Voltage vs Junction Temperature

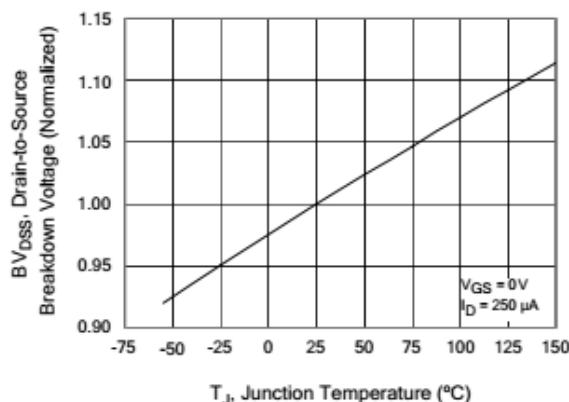


Figure 12. Typical Threshold Voltage vs Junction Temperature

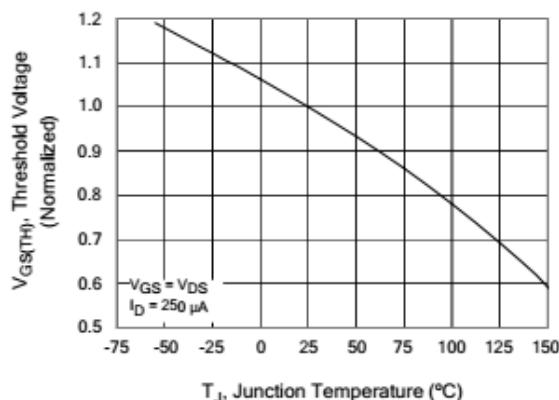


Figure 13. Maximum Forward Bias Safe Operating Area

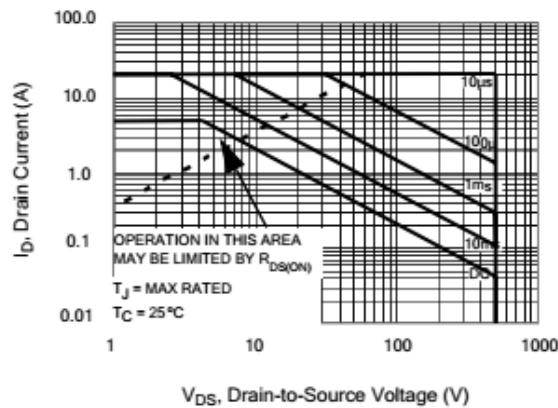


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

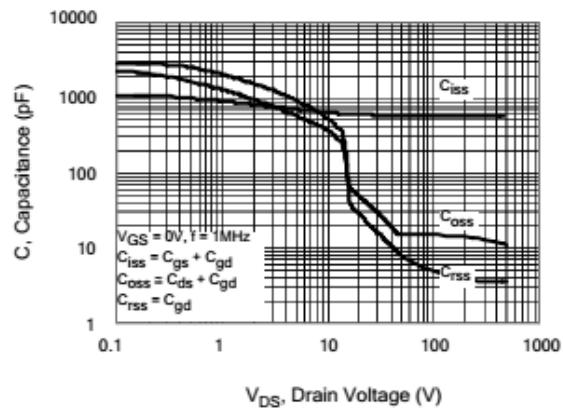


Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

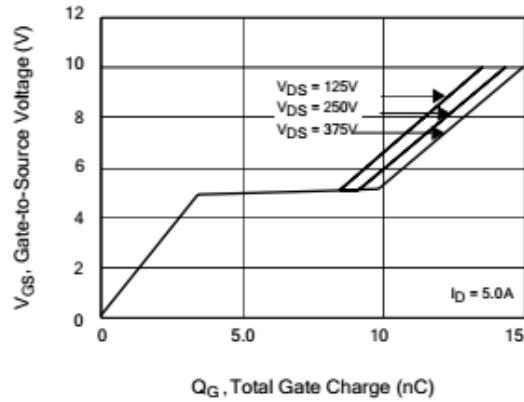
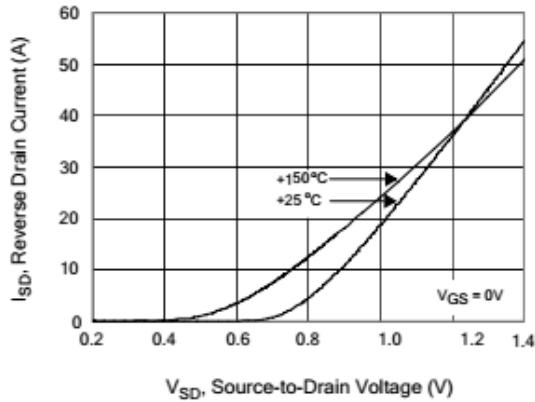


Figure 16. Typical Body Diode Transfer Characteristics



8. Test Circuits and Waveforms

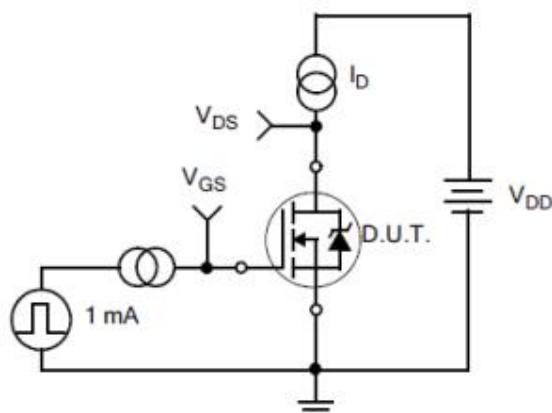


Figure 17. Gate Charge Test Circuit

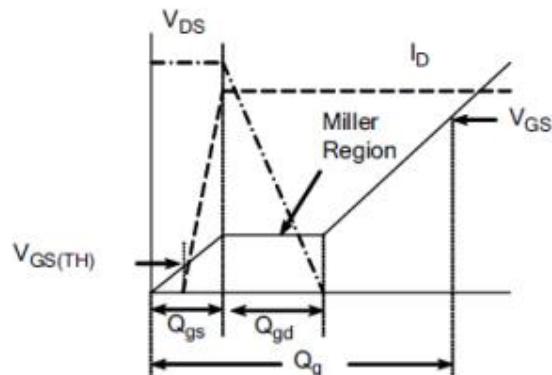


Figure 18. Gate Charge Waveform

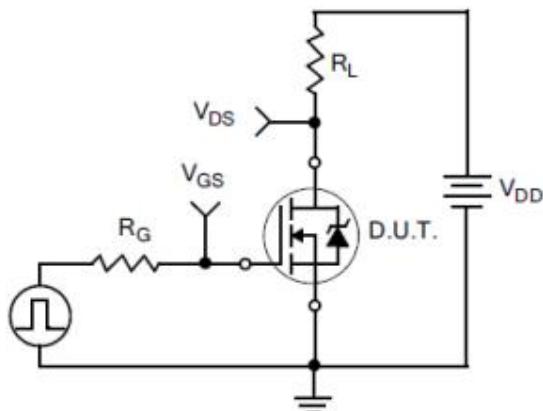


Figure 19. Resistive Switching Test Circuit

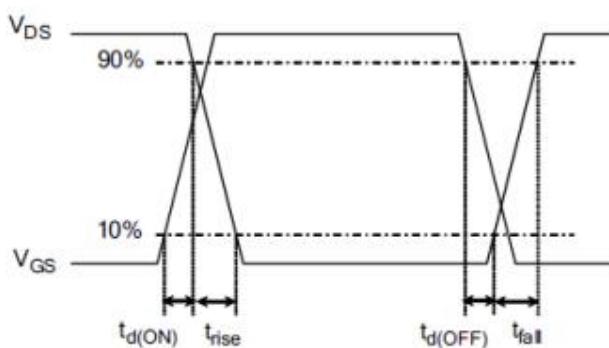


Figure 20. Resistive Switching Waveforms

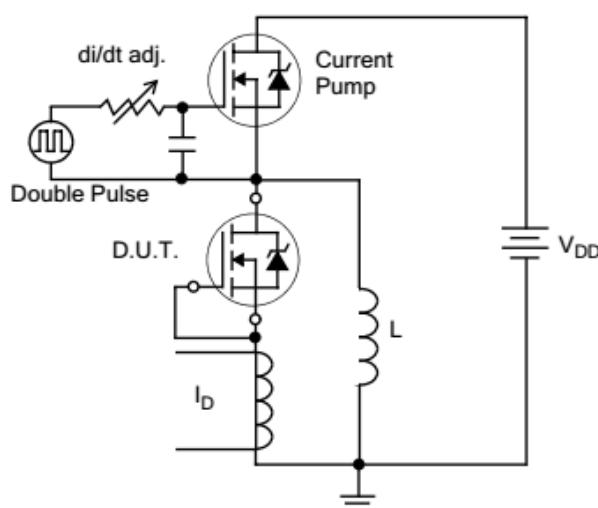


Figure 21. Diode Reverse Recovery Test Circuit

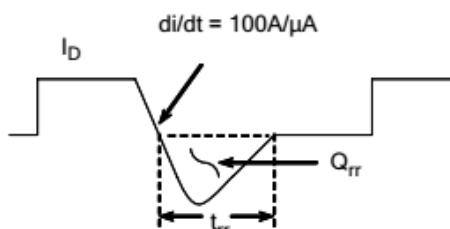


Figure 22. Diode Reverse Recovery Waveform

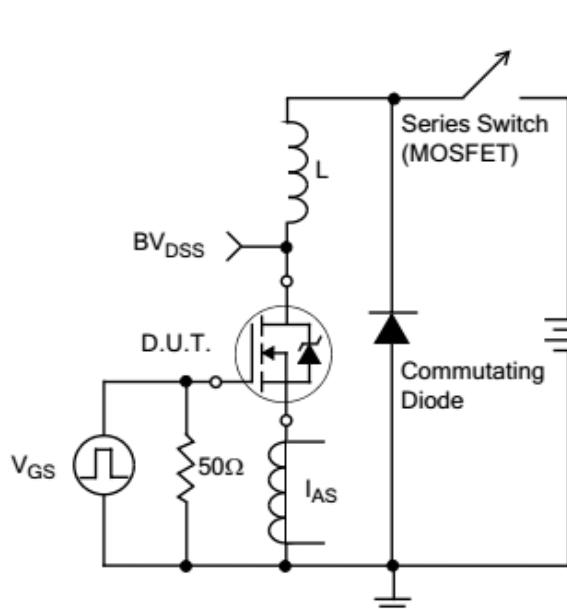


Figure 23. Unclamped Inductive Switching Test Circuit

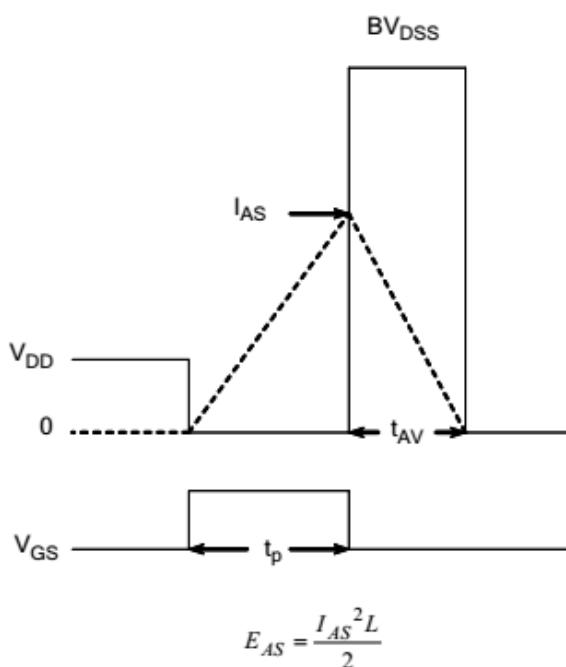


Figure 24. Unclamped Inductive Switching Waveforms

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