

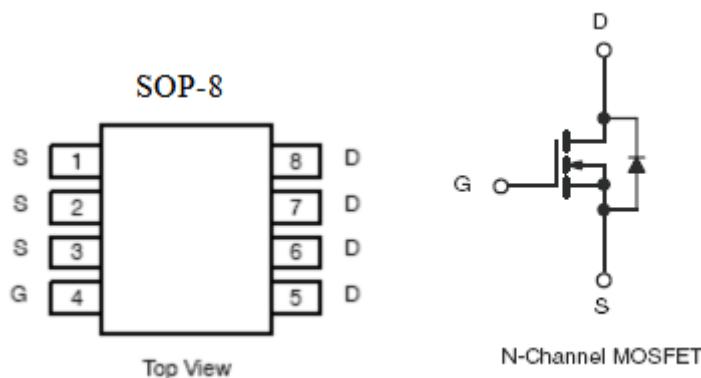
1. Features

- $R_{DS(on)}=5.5\text{m}\Omega(\text{typ}) @ V_{GS}=10 \text{ V}$
- Super low gate charge
- Green device available
- Excellent Cdv/dt effect decline
- Advanced high cell density trench technology

2. Description

The KNE7306A is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The KNE7306A meet the RoHs and Green Product requirement.

3. Symbol



4. Absolute maximum ratings

($T_A=25^\circ\text{C}$,unless otherwise noted)

Parameter	Symbol	Rating	Units
Drain-source voltage	V_{DSS}	60	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current $V_{GS}@10\text{V}^1$	I_D	22	A
		14	
Pulsed drain current ²	I_{DM}	130	A
Single pulse avalanche energy ³	EAS	125	mJ
Avalanche current	I_{AS}	50	A
Total power dissipation ⁴	P_D	3.1	W
Junction and storage temperature range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Thermal resistance-junction to ambient ¹ ($t \leq 10\text{s}$)	$R_{\theta JA}$	45	$^\circ\text{C/W}$
Thermal resistance-junction to ambient ¹ (steady state)	$R_{\theta JA}$	80	$^\circ\text{C/W}$

5.Electrical characteristics

($T_J=25^\circ\text{C}$,unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source breakdown voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=-250\mu\text{A}$	60	-	-	V
Drain-Source Leakage Current	I_{DSS}	$V_{\text{DS}}=60\text{V}, V_{\text{GS}}=0\text{V}, T_J=25^\circ\text{C}$	-	-	1	μA
		$V_{\text{DS}}=60\text{V}, V_{\text{GS}}=0\text{V}, T_J=55^\circ\text{C}$	-	-	5	
Gate-source leakage current	I_{GSS}	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.2	-	2.5	V
Static drain-source on- resistance ²	$R_{\text{DS(on)}}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=10\text{A}$	-	5.5	6.5	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=5\text{A}$	-	7.0	8.5	
Forward transconductance	g_{FS}	$V_{\text{DS}}=5\text{V}, I_{\text{D}}=18\text{A}$	-	65	-	S
Diode forward voltage ²	V_{SD}	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=1\text{A}, T_J=25^\circ\text{C}$	-	-	1.2	V
Total gate charge(10V)	Q_g	$V_{\text{DS}}=48\text{V}, V_{\text{GS}}=10\text{V}, I_{\text{D}}=18\text{A}$	-	75	-	nC
Gate-source charge	Q_{gs}		-	15.5	-	
Gate-drain charge	Q_{gd}		-	20.3	-	
Turn-on delay time	$t_{\text{d(on)}}$	$V_{\text{DD}}=30\text{V}, R_{\text{G}}=3.3\Omega, V_{\text{GS}}=10\text{V}, I_{\text{D}}=18\text{A}$	-	18.5	-	ns
Rise time	t_r		-	8.8	-	
Turn-off delay time	$t_{\text{d(off)}}$		-	58.8	-	
Fall time	t_f		-	15.8	-	
Input capacitance	C_{iss}	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=25\text{V}, F=1.0\text{MHZ}$	-	4006	-	pF
Output capacitance	C_{oss}		-	320	-	
Reverse transfer capacitance	C_{rss}		-	222	-	
Diode characteristics						
Continuous source current ^{1,5}	I_s	$V_G=V_D=0\text{V}, \text{Force current}$	-	-	22	A
Pulsed source current ^{2,5}	I_{SM}		-	-	130	A
Reverse recovery time	t_{rr}	$I_F=18\text{A}, dI/dt=100\text{A/us}, T_J=25^\circ\text{C}$	-	22.9	-	nS
Reverse recovery charge	Q_{rr}		-	11.6	-	nC

Note:1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

2. The data tested by pulsed, pulse width $\leq 300\text{us}$,duty cycle $\leq 2\%$.
3. The EAS data shows Max.rating. The test condition is $V_{\text{DD}}=50\text{V}, V_{\text{GS}}=10\text{V}, L=0.1\text{mH}, I_{\text{AS}}=50\text{A}$.
4. The power dissipation is limited by 150°C junction temperature.
5. The data is theoretically the same as I_{D} and I_{DM} , in real applications, should be limited by total power dissipation.

6. Test circuits and waveforms

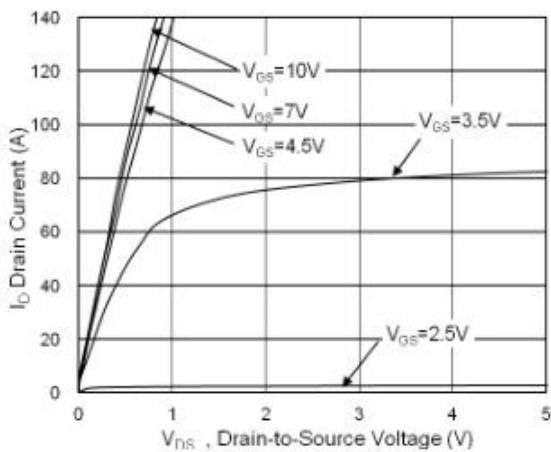


Fig.1 Typical Output Characteristics

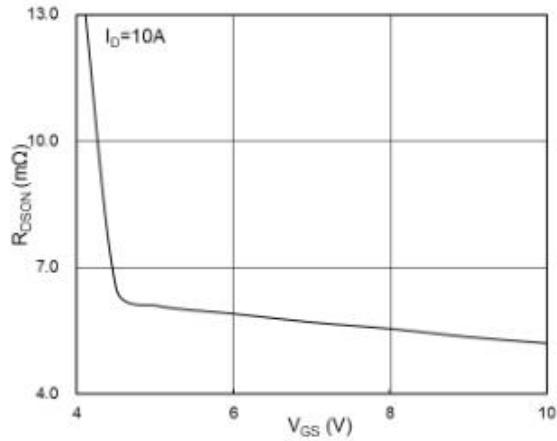


Fig.2 On-Resistance vs. Gate-Source Voltage

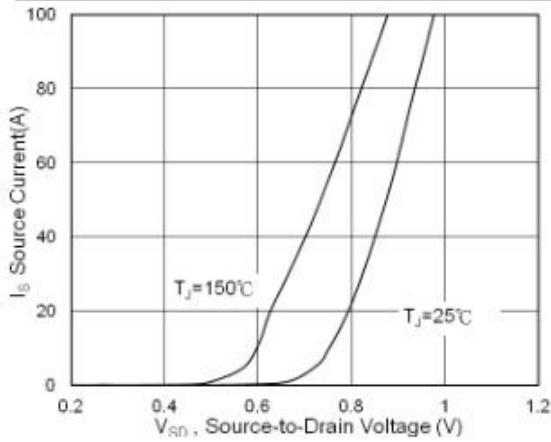


Fig.3 Forward Characteristics of Reverse

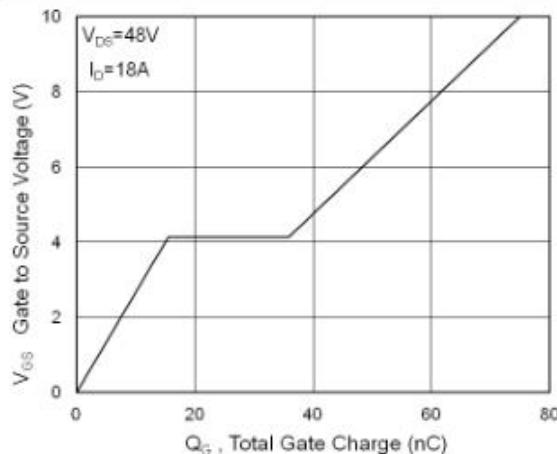


Fig.4 Gate-Charge Characteristics

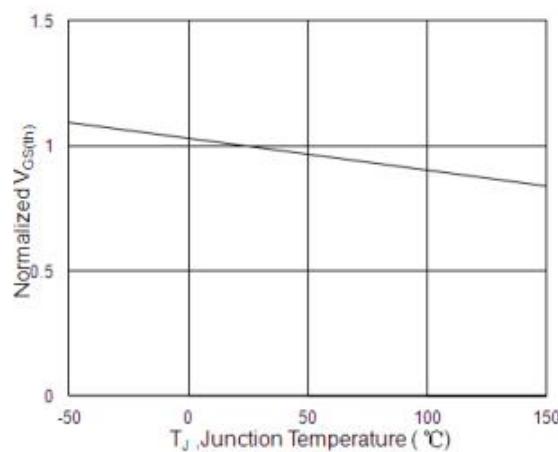


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

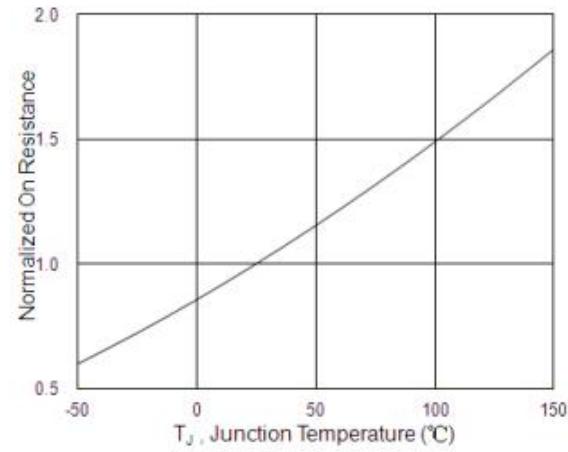


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

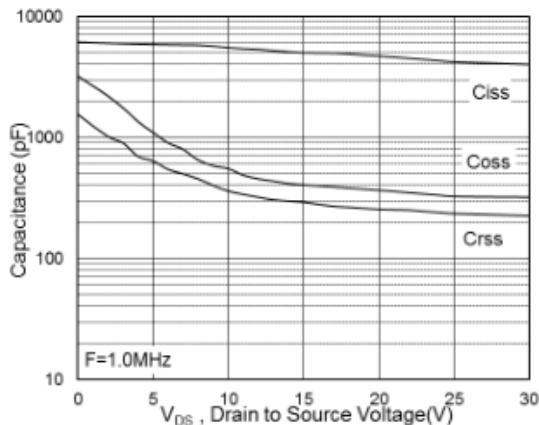


Fig.7 Capacitance

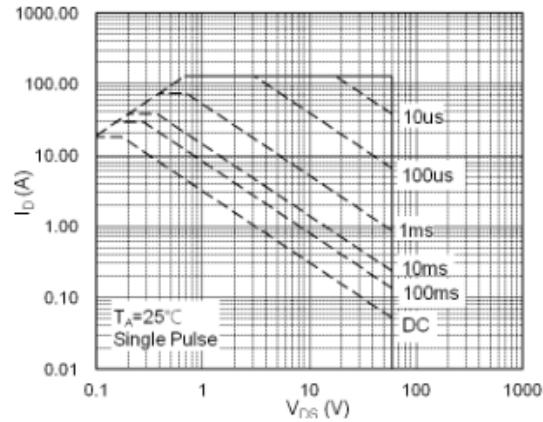


Fig.8 Safe Operating Area

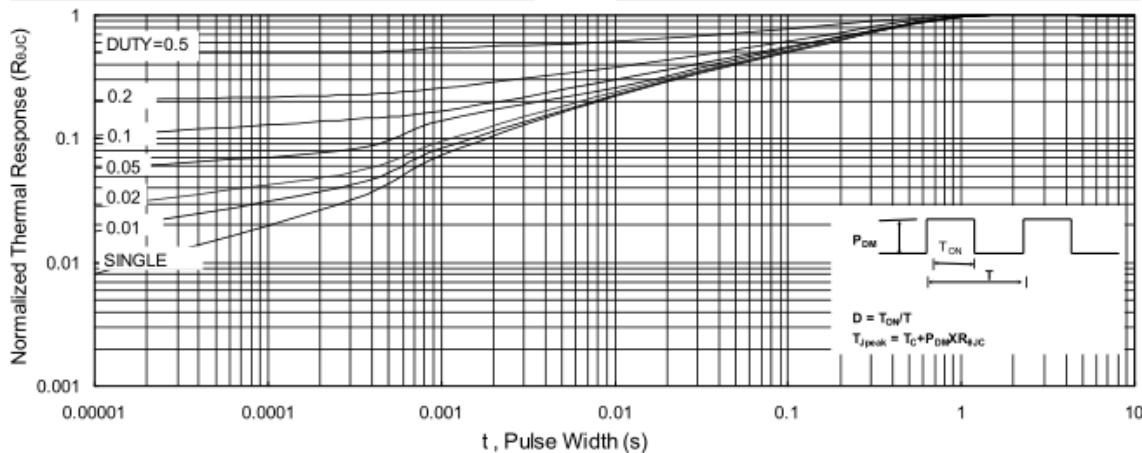


Fig.9 Normalized Maximum Transient Thermal Impedance

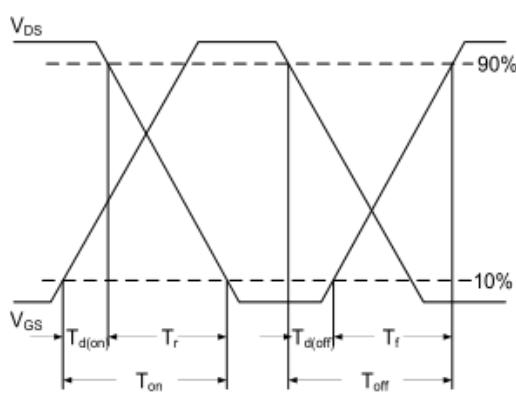


Fig.10 Switching Time Waveform

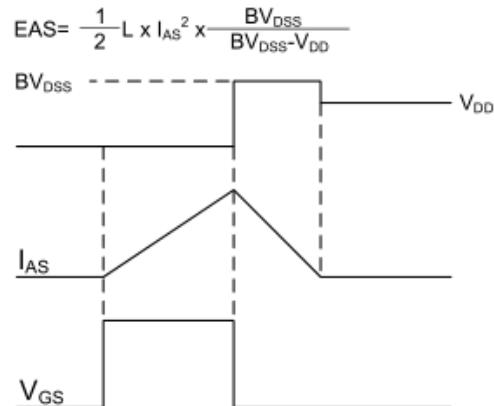


Fig.11 Unclamped Inductive Switching Waveform

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