

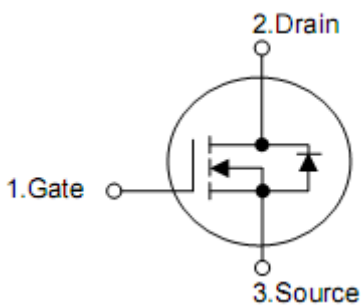
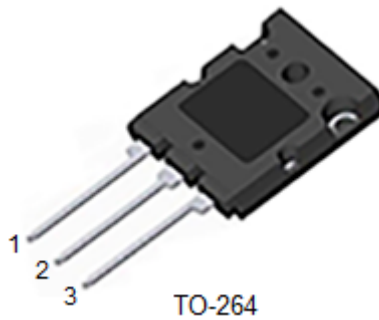
1. Features

- Advanced Planar Process
- $R_{DS(ON)}=280m\Omega(\text{typ.})@V_{GS}=10V$
- Low Gate Charge Minimize Switching Loss
- Rugged Poly silicon Gate Structure

2. Applications

- BLDC Motor Driver
- Electric Welder
- High Efficiency SMPS

3. Pin configuration



Pin	Function
1	Gate
2	Drain
3	Source

4. Ordering Information

Part Number	Package	Brand
KNK7880A	TO-264	KIA

5. Absolute maximum ratings

(T_c= 25 °C , unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-to-Source Voltage	V _{DSS}	800	V
Gate-to-Source Voltage	V _{GSS}	±30	
Continuous Drain Current	I _D	27	A
Continuous Drain Current @ T _c =100 °C		17	A
Pulsed Drain Current at V _{GS} =10V ^{2),4)}	I _{DM}	108	A
Single Pulse Avalanche Energy	EAS	4200	mJ
Peak Diode Recovery dv/dt ³⁾	dv/dt	5	V/ns
Power Dissipation	P _D	650	W
Derating Factor above 25 °C		5.2	W/°C
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	T _L T _{PAK}	300 260	°C
Storage Temperature Range	T _J & T _{STG}	-55 to 150	°C

6. Thermal characteristics

Parameter	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	R _{θJC}	0.192	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	55	°C/W

7. Electrical characteristics

(T_J=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	800	-	-	V
Drain-to-Source Leakage Current	I _{DSS}	V _{DS} =800V, V _{GS} =0V	-	-	5	uA
		V _{DS} =640V, V _{GS} =0V, T _J =125°C	-	-	125	
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	-	-	±100	nA
Drain-to-Source ON Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =13.5A	-	280	350	mΩ
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250uA	2.5	-	4.5	V
Forward Transconductance	g _{FS}	V _{DS} =25V, I _D =12A	-	18	-	S
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =25V, f=1.0MHZ	-	7280	-	pF
Reverse Transfer Capacitance	C _{rss}		-	35	-	
Output Capacitance	C _{oss}		-	660	-	
Total Gate Charge	Q _g	V _{DD} =400V, I _D =13A, V _{GS} =0~10V	-	185	-	nC
Gate-to-Source Charge	Q _{gs}		-	42	-	
Gate-to-Drain (Miller) Charge	Q _{gd}		-	62	-	
Turn-on Delay Time	t _{d(ON)}	V _{DD} =400V, I _D =13A, R _G =10Ω, V _{GS} =10V	-	56	-	nS
Rise Time	t _{rise}		-	105	-	
Turn-Off Delay Time	t _{d(OFF)}		-	82	-	
Fall Time	t _{fall}		-	96	-	
Continuous Source Current ²⁾	I _{SD}	Integral PN-diode in MOSFET	-	-	27	A
Pulsed Source Current ²⁾	I _{SM}		-	-	108	A
Forward Voltage	V _{SD}	I _S =27A, V _{GS} =0V	-	-	1.5	V
Reverse recovery time	t _{rr}	V _{GS} =0V, I _F =27A, diF/dt=-100A/μs	-	900	-	ns
Reverse recovery charge	Q _{rr}		-	2.0	-	uC

Note:

- 1) T_J=+25 to +150
- 2) Silicon limited current only.
- 3) Package limited current.
- 4) Repetitive rating; pulse width limited by maximum junction temperature.
- 5) Pulse width≤380μs; duty cycle≤2%.

8. Typical Characteristics

Figure 1. Maximum Transient Thermal Impedance

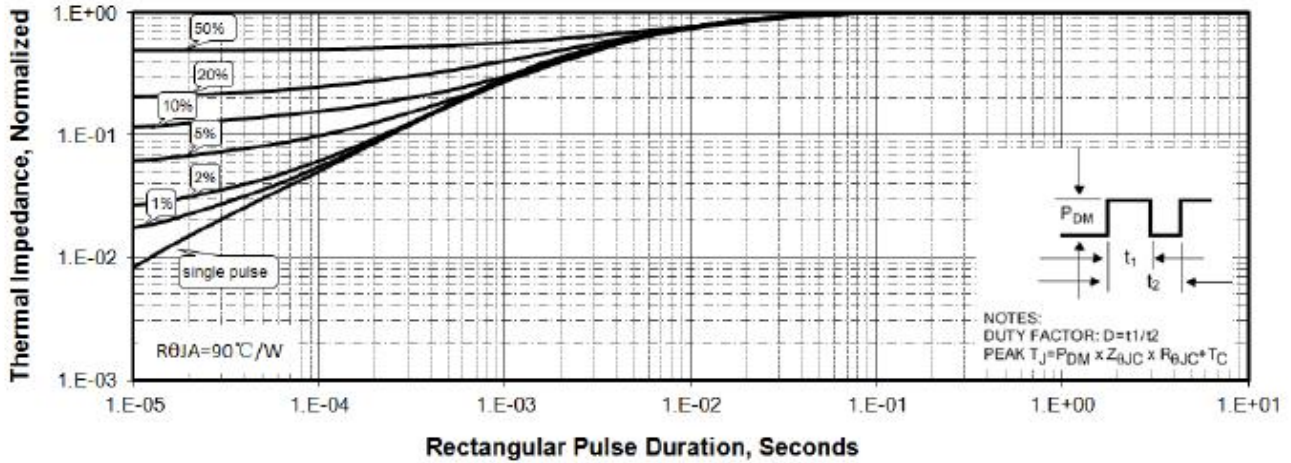


Figure 2 . Max. Power Dissipation vs Case Temperature

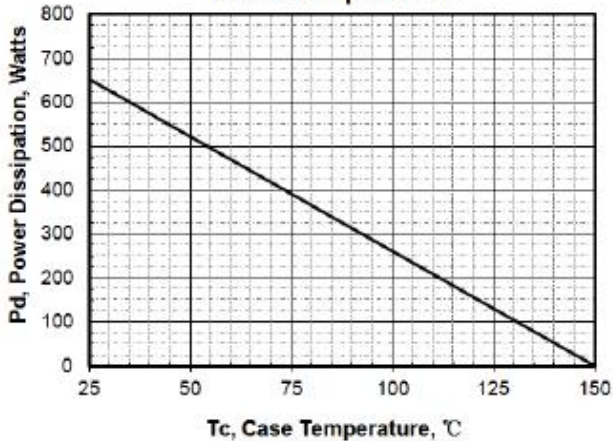


Figure 3 .Maximum Continuous Drain Current vs Tc

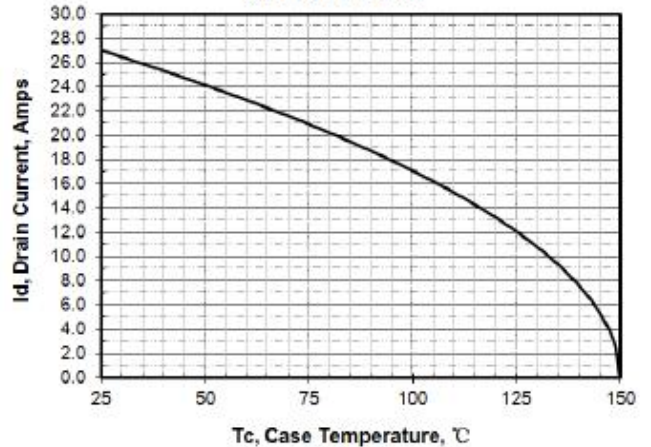


Figure 4. Output Characteristics

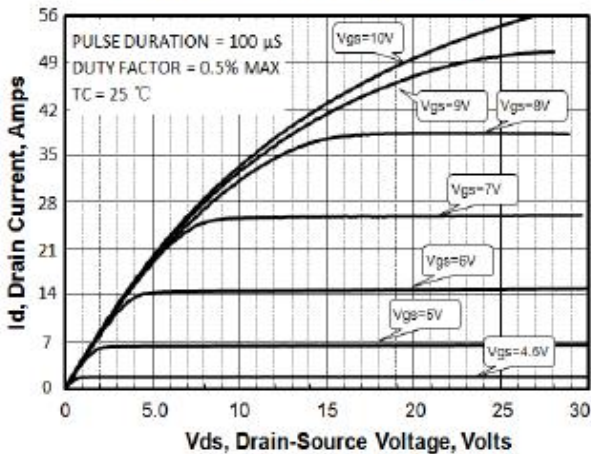


Figure 5. Rds(on) vs Gate Voltage

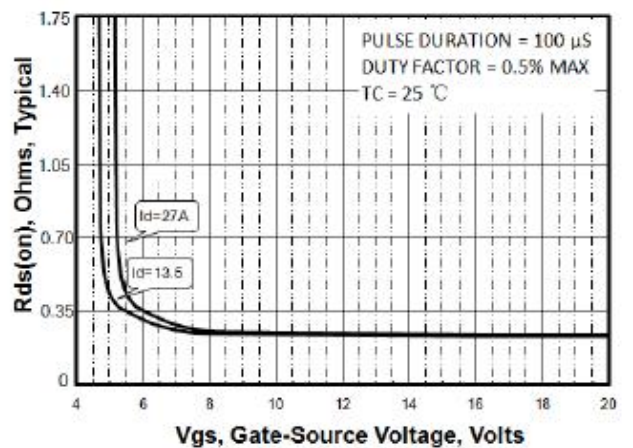


Figure 6. Peak Current Capability

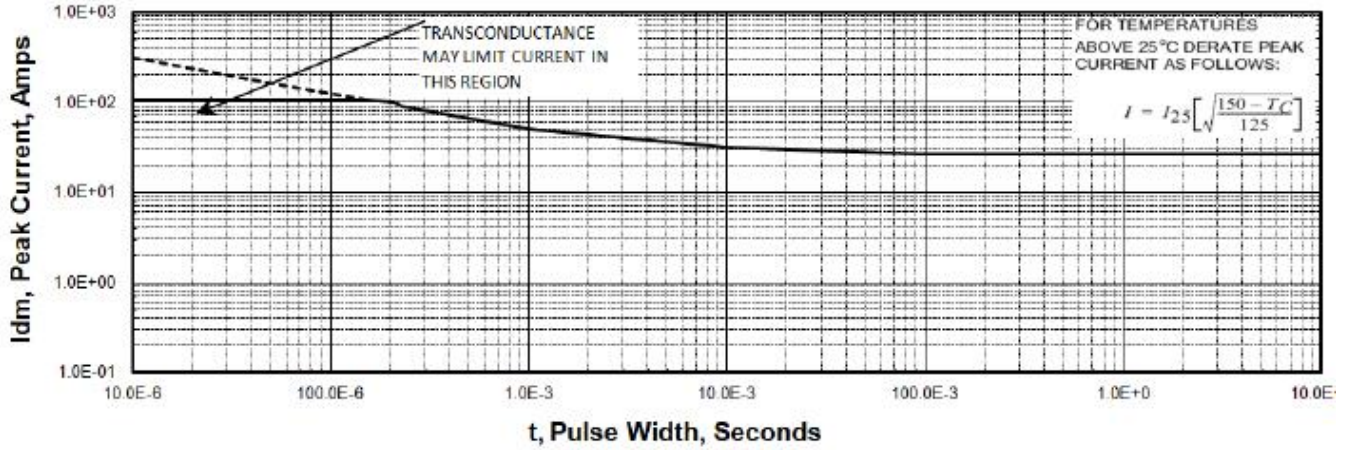


Figure 7. Transfer Characteristics

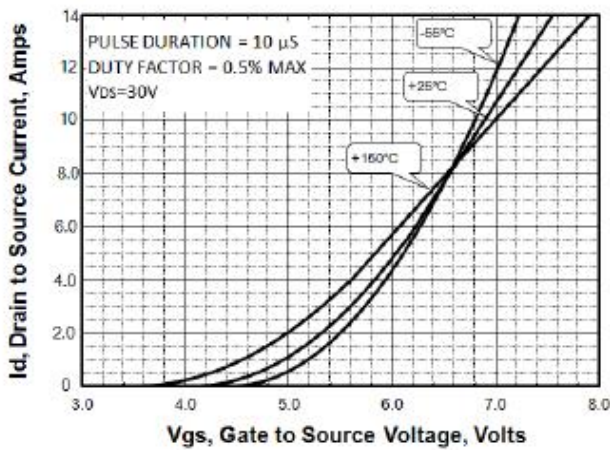


Figure 8. Unclamped Inductive Switching Capability

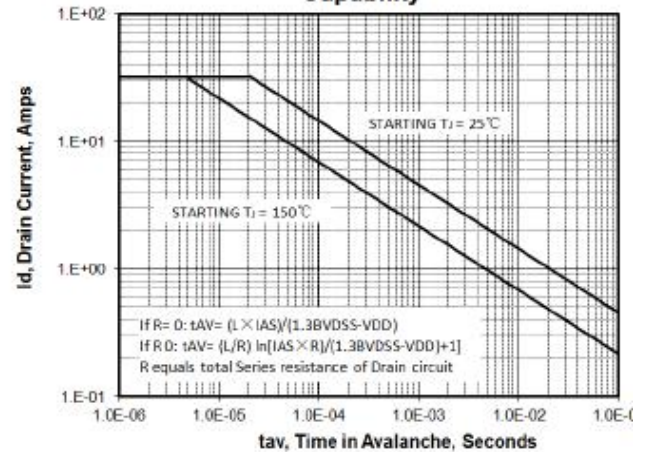


Figure 9. Drain to Source ON Resistance vs Drain Current

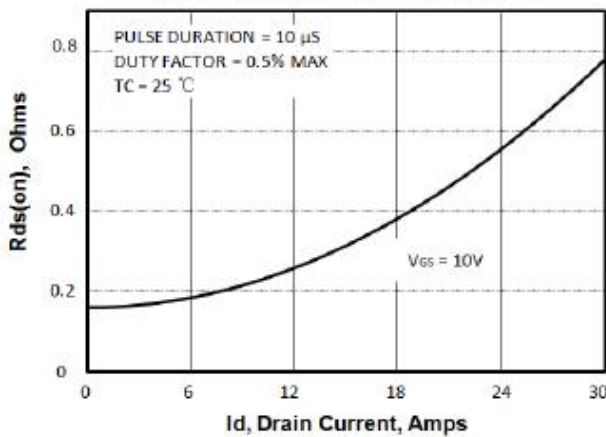


Figure 10. Rds(on) vs Junction Temperature

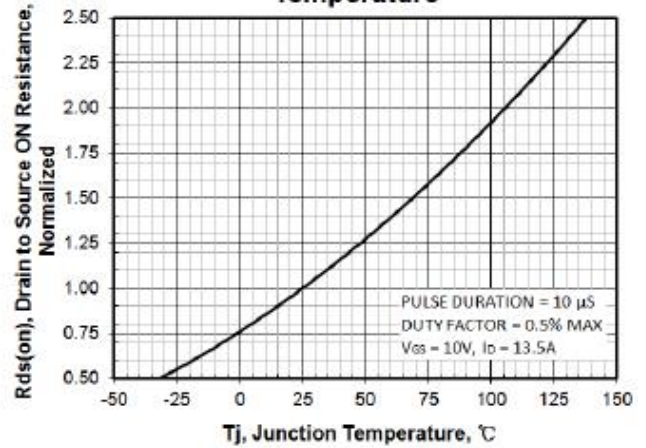


Figure 11. Breakdown Voltage vs Temperature

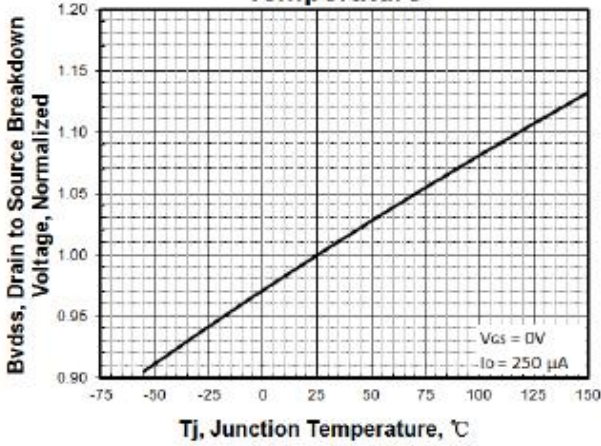


Figure 12. Threshold Voltage vs Temperature

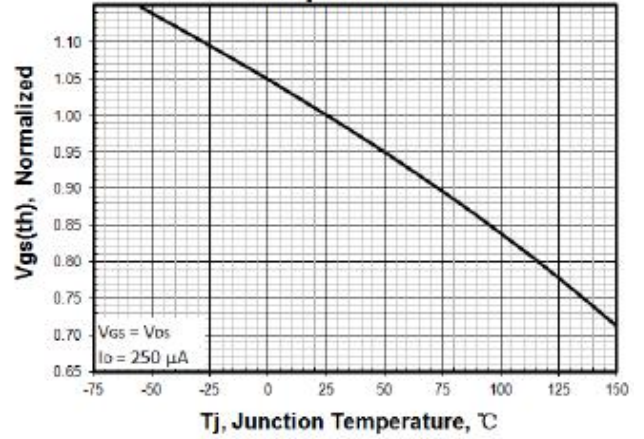


Figure 13. Maximum Safe Operating Area (TO-247)

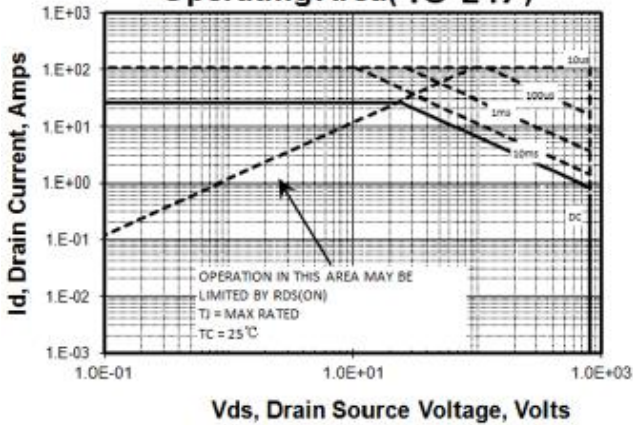


Figure 14. Capacitance vs Vds

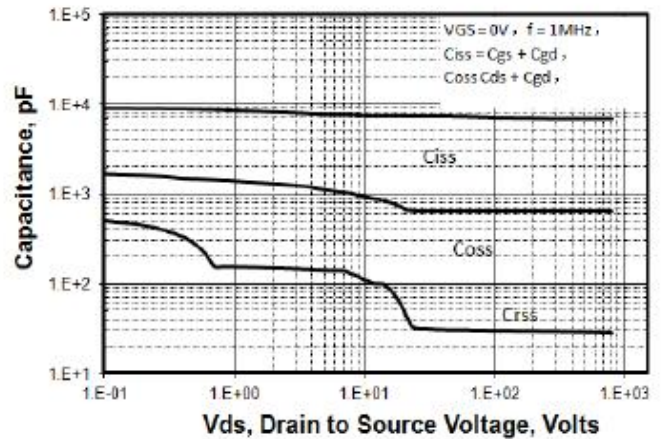


Figure 15. Typical Gate Charge

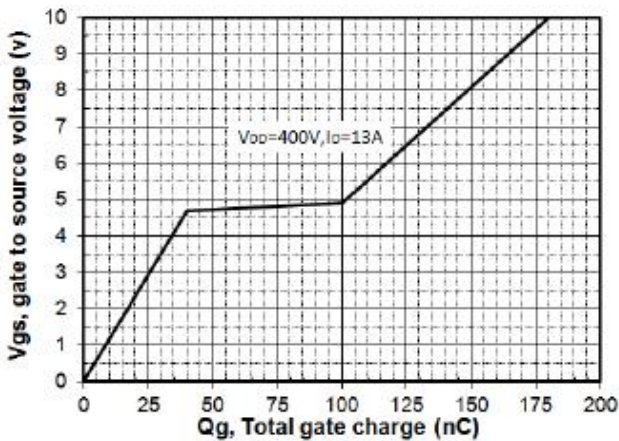
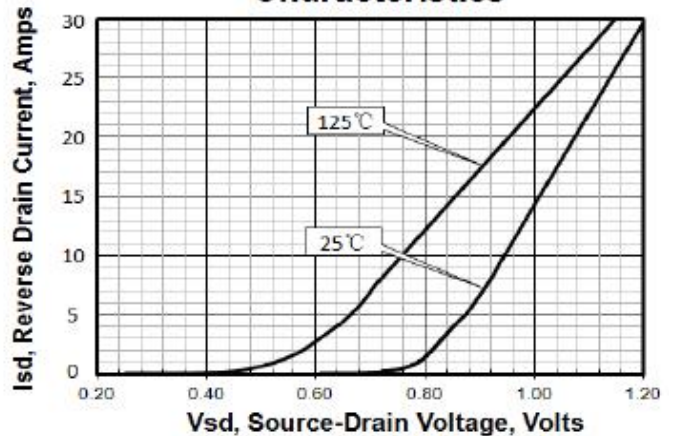


Figure 16. Body Diode Transfer Characteristics



9. Test Circuits and Waveforms

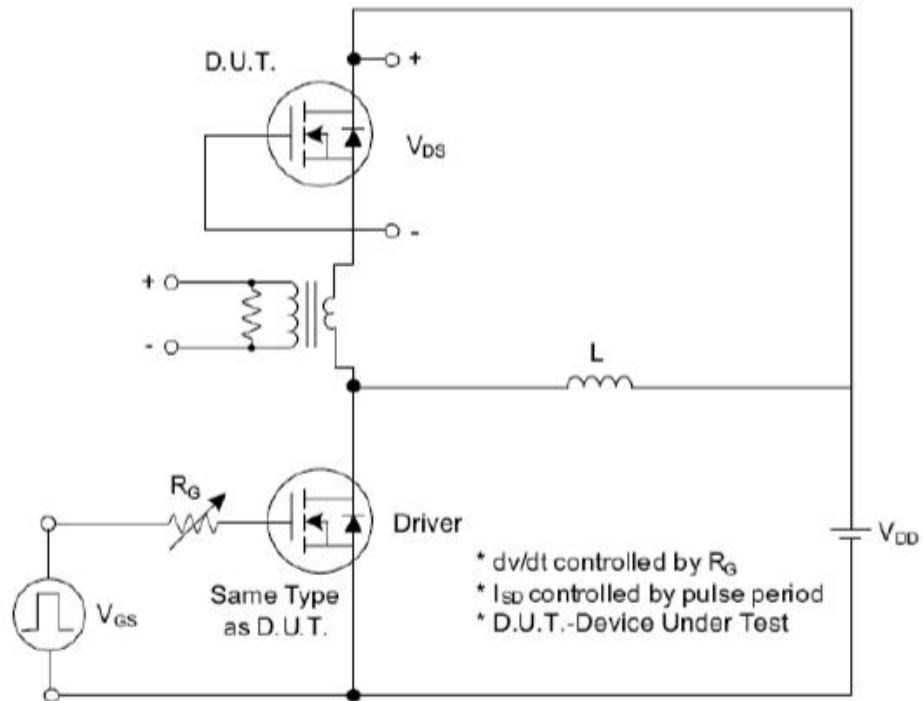


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

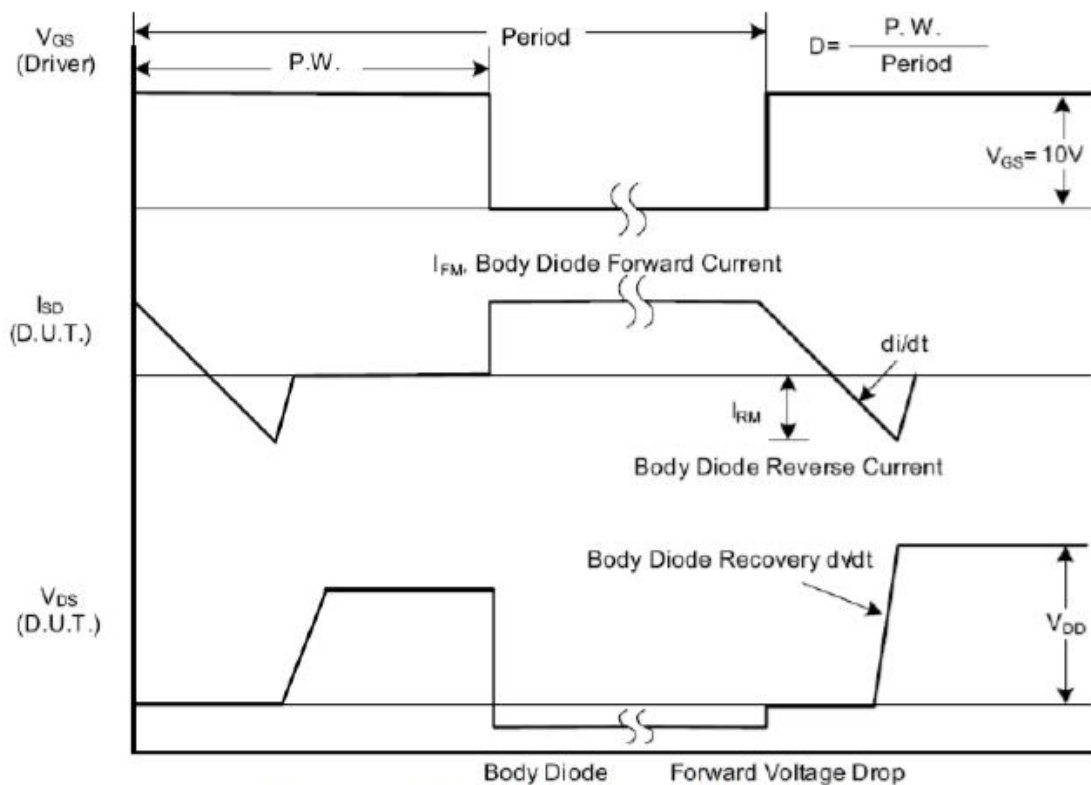


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

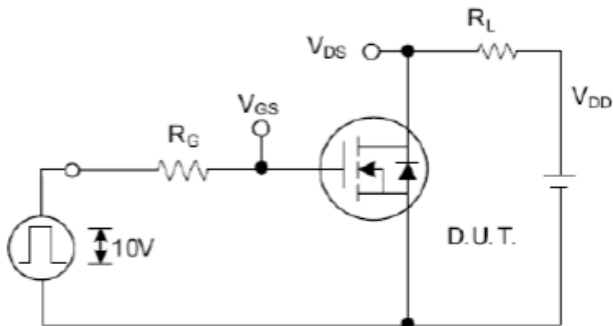


Fig. 2.1 Switching Test Circuit

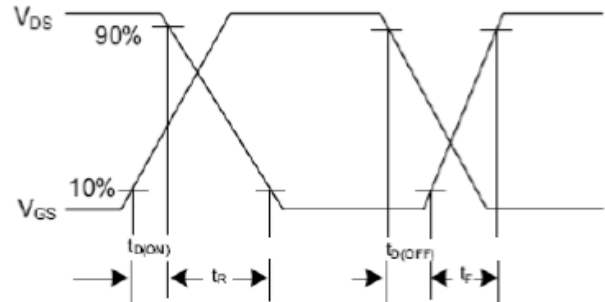


Fig. 2.2 Switching Waveforms

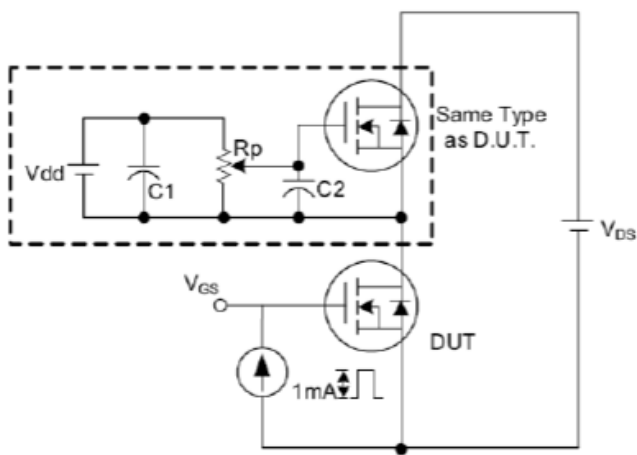


Fig. 3.1 Gate Charge Test Circuit

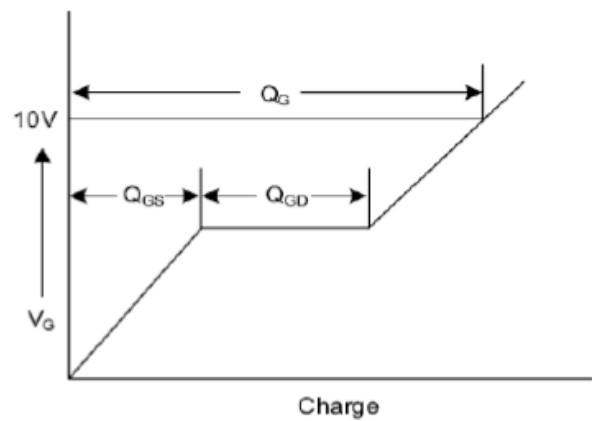


Fig. 3.2 Gate Charge Waveform

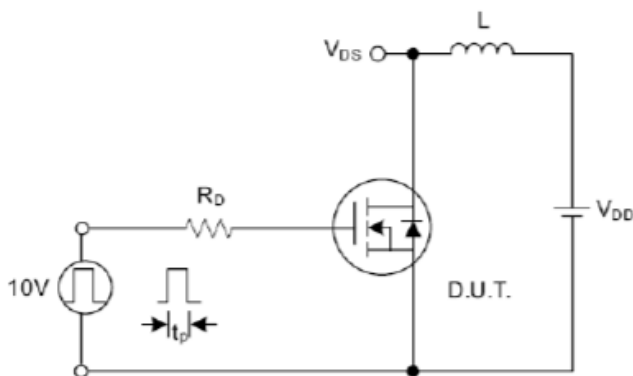


Fig. 4.1 Unclamped Inductive Switching Test Circuit

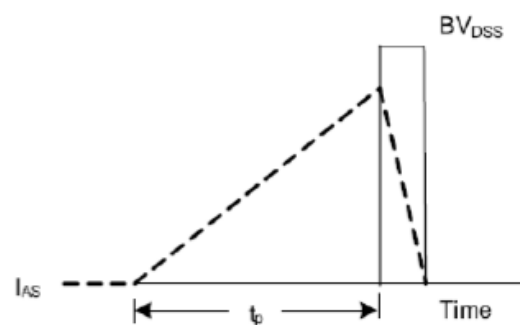


Fig. 4.2 Unclamped Inductive Switching Waveforms

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