# AS1138

## 30W PoE PD and DC-DC Controller

## FEATURES

- Full support of both IEEE® Std. 802.3af-2005 and IEEE® Std. 802.3at-2009 power requirements
- "2-Event" classification for 802.3at higher power PDs
- Robust Type 2 PSE detector with proprietary digital filtering for line noise to eliminate false positives
- IEC 61000-4-2/3/4/5/6 requirements for EMC Compliance
- Integrated Surge Protection for 15kV/8kV System level ESD Compliance
- Integrated DC-DC controller for exceptional EMI performance
- Programmable DC current limit up to 720mA for 30W applications
- Seamless support for local power, down to 9.5V
- Implemented in robust 100V automotive process
- Low Rds-on Hot-Swap FET (typical 0.8Ω)
- Integrated Short-Circuit Protection
- Over temperature protection
- Industrial temperature range, -40°C to +85°C
- 5x5 mm, 20 lead QFN Package, RoHS compliant

## GENERAL DESCRIPTION

The AS1138 is a single-chip, highly integrated CMOS solution for Power over Ethernet (PoE) Powered Devices requiring input power of up to 30Watts. Applications include Voice over IP (VoIP) Phones, Wireless LAN Access Point, Security Cameras, WiMAX Terminals, Point-of-Sales Terminals, RFID Readers, Thin Clients and Notebook computers.

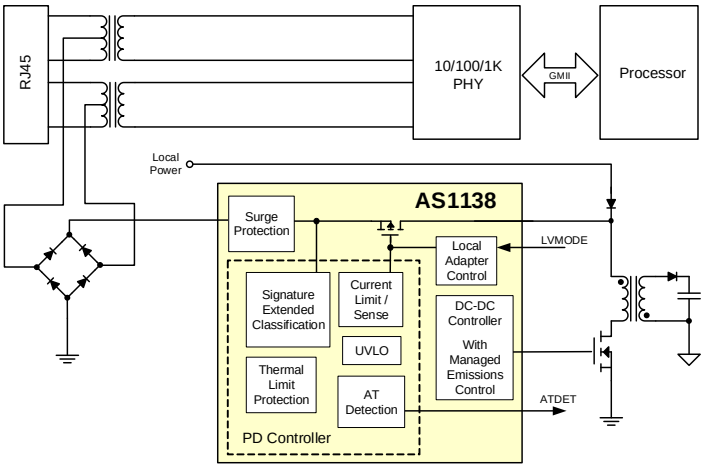
The AS1138 integrates input surge protection, a PD controller and a low-emission DC-DC controller. The AS1138 implements all of the physical layer Powered Device (PD) functionality, as required by IEEE® 802.3af-2005 and IEEE® 802.3at-2009 standards. This includes 2-event classification, Type 2 PSE detection indicator (ATDET), PD detection, under-voltage lock out (UVLO), and Hot-Swap FET integration.

The AS1138 has been architected to address both EM emission concerns and surge/over-voltage protection in PoE applications. The chip implements many design features that minimize transmission of system common-mode noise onto the Unshielded Twisted Pair (UTP). On-chip integration of surge protection provides faster response to surge events and limits stray surge current from passing through sensitive circuits, such as the Ethernet PHY. The device is designed to provide safe, low-impedance discharge paths directly to the earth ground, resulting in superior reliability and circuit protection.

## TYPICAL APPLICATIONS

- Pan, tilt and zoom (PTZ), security and web cameras
- Voice over IP (VoIP) phones
- Wireless LAN access points, WiMAX terminals
- Point-of-sale (PoS) terminals, RFID terminals
- Thin clients and notebook computers
- Fiber-to-the-home (FTTH) terminals

## SIMPLIFIED APPLICATION DIAGRAM



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## PIN ASSIGNMENTS AND DESCRIPTIONS

**Figure 1 - AS1138 Pin Diagram**

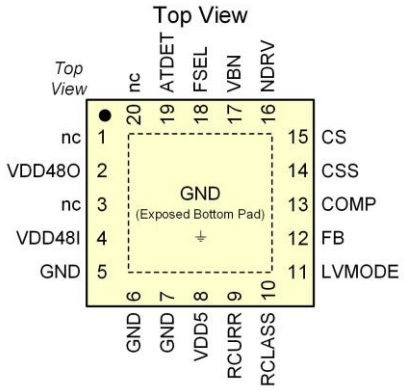



**Table 1 - Pin Assignments**

| Pin | I/O | Name | Description |
|---|---|---|---|
| 1 | - | nc | No Connect |
| 2 | P | VDD48O | Switched 48V supply output |
| 3 | - | nc | No Connect |
| 4 | P | VDD48I | 48 V positive bus pin, fed by the output of the external diode bridge. This bus requires the connection of a detection signature capacitor and resistor. Refer to Detection Mode section. |
| 5 | A | GND | Must be connected to paddle ground (GND) |
| 6 | A | GND | Must be connected to paddle ground (GND) |
| 7 | A | GND | Must be connected to paddle ground (GND) |
| 8 | O | VDD5 | Internal 5 volts bus decoupling point |
| 9 | A | RCURR | Current limit pin. Connection to paddle ground sets the current limit to ILIM-AF (for 13W applications). Open circuit sets the current limit to ILIM-AT (for 30W applications). |
| 10 | A | RCLASS | Classification resistor connection |
| 11 | A | LVMODE | Local Voltage Mode. When pulled high, LVMODE opens the internal FET switch and keeps the DC-DC controller active. This is a current-mode input pin. It should be pulled to GND when not in use. |
| 12 | A | FB | DC-DC Controller feedback point |
| 13 | A | COMP | DC-DC Controller error amplifier compensation network connection |
| 14 | A | CSS | DC-DC Controller soft-start capacitor connection point (required). |
| 15 | A | CS | DC-DC Controller peak-current sense input (low side) |
| 16 | O | NDRV | DC-DC Controller N-MOSFET gate drive |
| 17 | O | VBN | DC-DC Controller low-side supply decoupling |
| 18 | I | FSEL | Frequency Select. This pin sets the switching frequency of the DC-DC converter. |
| 19 | O | ATDET | IEEE® 802.3at-2009 PSE detects. High level output indicates availability of higher system power, either via connection to a Type 2 PSE, or via a local power supply. |
| 20 | - | nc | No Connect |
| Paddle | P | GND | Local analog ground. This is the negative output from the external diode bridge and is not isolated from the line input. |

Key: I = Input O = Output A = Analog signal P = Power

**Table 2 - Absolute Maximum Ratings**

| Description | Max Value[1] | Units |
|---|---|---|
| High-voltage pins (4—VDD48I; 2—VDD48O) under Transient conditions[4] | 100 | Volts |
| High-voltage pins (4—VDD48I; 2—VDD48O) Steady-state with internal Surge Clamp | 80 | Volts |
| Low-voltage pins (8—VDD5; 9-RCURR; 10—RCLASS; 11—LVMODE; 12—FB; 13—COMP; 14—CSS; 15—CS; 16—NDRV; 17—VBN; 18—FSEL; 19—ATDET) | 6 | Volts |
| **ESD Ratings** | | |
| Human body model[2] | 2 | kV |
| ESD charged device model | 500 | V |
| ESD machine model | 200 | V |
| System level (contact/air) at RJ-45[3] | 8/15 | kV |
| **Temperature** | | |
| Storage temperature | 165 | °C |
| Junction temperature | 150 | °C |

[1] Absolute maximum ratings are limits beyond which damage to the device may occur.
[2] The human body model is as described in JESD22-A114.
[3] System ESD testing done per IEC61000-4-2.
[4] Transient conditions like system startup and other noise conditions. Device must not be exposed to sustained over-voltage condition at this level. See section on Rectification and Protection for further details on Integrated Surge Protection.

**Table 3 - Normal Operating Conditions**

Unless otherwise noted, specifications are for $V_{in}$ = 48V.

| Description | Min | Typical[1] | Max |
|---|---|---|---|
| $V_{IN-AF\ (Type\ 1\ PD)}$ | 37V | 48V | 57V |
| $V_{IN-AT\ (Type\ 2\ PD)}$ | 42.5V | 48V | 57V |
| Operating temperature range, | -40ºC | | +85°C |

[1] Typical specification; not 100% tested. Performance guaranteed by design and/or other correlation methods.

**Table 4 - Electrical Characteristics**

Unless otherwise noted, specifications are for $T_A$ = -40°C to +85°C and VIN = 48V (at RJ45 input).

| Description | Min | Typical[1] | Max | Units | Comments |
|---|---|---|---|---|---|
| **PD (all PD voltage limits specified at the RJ45 interface)** | | | | | |
| Inrush current limit (af) – Type 1 PD | 50 | 150 | 200 | mA | For VDD48O ≤ 16V during startup, Cin = 10µF |
| Inrush current limit (at) – Type 2 PD | 100 | 295 | 350 | mA | For VDD48O ≤ 16V during startup, Cin = 10µF |
| Operating current – Type 1 | | | 350 | mA | Pin 9 (RCURR) pulled to GND; device configured for 13W operation |
| Operating current – Type 2 | | | 720 | mA | Pin 9 (RCURR) left open; device configured for 30W operation |
| PoE current limit – Type 1 ($I_{LIM-AF}$) | 350 | 400 | 500 | mA | Pin 9 (RCURR) pulled to GND; device configured for 13W operation |
| PoE Current limit – Type 2 ($I_{LIM-AT}$) | 720 | 800 | 925 | mA | Pin 9 (RCURR) left open; device configured for 30W operation |
| Switch on resistance, $R_{DS-ON}$ | | 0.8 | 1 | Ω | measured at 350mA input |
| Min Detection Signature voltage | | | 2.7 | V | |
| Max Detection Signature voltage | 10.1 | 12.5 | 13 | V | |
| Classification lower threshold | 11 | 12.5 | 14.5 | V | During Classification, the AS1138 sinks current as defined Table 7. |
| Classification upper threshold | 20.5 | 22 | 24 | V | During Classification, the AS1138 sinks current as defined Table 7. |
| Min Mark Event voltage | | | 6.9 | V | |
| Max Mark Event voltage | 10 | 12.5 | 13 | V | |
| Mark Event current | 0.25 | | 4 | mA | When the input voltage is less than $V_{MARK\_TH}$ Min (IEEE® 802.3at-2009) during the Classification signature, a Type 2 PD must draw Mark Event current. |
| Classification-Mark hysteresis | | 1 | | V | |
| Classification reset voltage | 2.81 | | 6.9 | V | |
| ATDET high ($V_{OH}$) | 4.7 | 4.9 | 5.1 | V | Under 2mA output |
| ATDET low ($V_{OL}$) | 0.0 | 0.02 | 0.1 | V | 2mA input current |
| UVLO threshold, $V_{IN\_RISING}$ | 37 | 38 | 42 | V | |
| UVLO threshold, $V_{IN\_FALLING}$ | 30 | 32 | 34 | V | |
| **DC-DC Controller** | | | | | |
| $F_{OSC}$ (SMPS) switching frequency | 80<br>200<br>315<br>450 | 100<br>225<br>350<br>500 | 120<br>250<br>385<br>550 | kHz | Rosc = 178kΩ<br>Rosc = 100kΩ<br>Rosc = 53.6kΩ<br>Rosc = 36.8kΩ<br>DC-DC Controller operating frequency, selected by using Rosc (1%) resistor on FSEL pin |
| $F_{OSC}$ temperature coefficient | | 0.12 | | %/°C | |
| NDRV $R_{OUT}$ | | 1.2 | 3 | Ω | Output drive resistance |
| NDRV voltage | | 4.7 | | V | NDRV voltage follows VBN power supply voltage |
| Gate drive dynamic response<br>NDRV $T_R$, $T_F$ | | 2.2<br>2 | | ns<br>ns | 10% - 90% with $C_{LOAD}$ = 1 nF |
| Max. NDRV duty cycle | | 80 | | % | Measured at 350kHz |
| Min. NDRV duty cycle | | 6 | 10 | % | Measured at 350kHz |
| VBN | | 4.7 | | V | Internal supply voltage; sets $V_{OH}$ of NDRV. |
| Error amplifier reference voltage | 1.45 | 1.5 | 1.55 | V | Compared to input of the FB pin |
| $V_{PK}$, peak current sense threshold voltage at CS | 500 | 600 | 700 | mV | $I_{PEAK} = V_{PK}/R_{SENSE}$ |
| Soft start ramp time | | 2 | | ms | Conditions: CSS = 100nF |
| COMP source current | | 80 | | µA | FB = 0V, COMP = 0V |
| COMP sink current | | 80 | | µA | FB = 5V, COMP = 5V |

| Description | Min | Typical[1] | Max | Units | Comments |
|---|---|---|---|---|---|
| Open loop voltage gain (Error amplifier) | | 80 | | dB | |
| Small signal unity-gain bandwidth | | 5 | | MHz | COMP connected to FB. |
| FB leakage (source or sink) | | 1 | | µA | |
| **Local Power Mode** | | | | | |
| LVMODE threshold low ($I_{IL}$) | | | 20 | µA | |
| LVMODE threshold high ($I_{IH}$) | 60 | | | µA | |
| Local power operating voltage range | 9.5 | | 57 | V | Local power voltage is specified between VDD48O and GND, using LVMODE feature. Note that power transformer must be capable of handling that full voltage range |
| **Thermal Protection** | | | | | |
| Thermal shutdown temperature | | 165 | | °C | Above this Temp., the AS1138 is disabled. |
| Thermal shutdown hysteresis | | 40 | | °C | Temperature change required to restore full operation after thermal shutdown |
| Current reduction temperature threshold | | 145 | | °C | Temperature at which thermal current reduction is applied |
| Thermal current reduction | | 50 | | % | |
| Thermal current reduction hysteresis | | 20 | | °C | Temperature change required to restore full operation after thermal current reduction |
| **Power Dissipation** | | | | | |
| Power dissipation, Type 1, $P_{DISS}$ | | 0.3 | 0.5 | W | Measured at 13W input |
| Power dissipation, Type 2, $P_{DISS}$ | | 0.8 | 1.3 | W | Measured at 30W input |
| Max. on-die operating temperature | | | 140 | °C | Maximum recommended operating temperature for normal operation |

[1] Typical specification is not 100% tested. Performance guaranteed by design and/or other correlation methods

**Table 5 - Package Thermal Characteristic**

| Description | Min | Typical[1] | Max | Units | Comments |
|---|---|---|---|---|---|
| Thermal Resistance, Junction to Ambient, $\theta_{JA}$ | | 31 | | ºC/W | 20 lead QFN package |
| Thermal Resistance, Junction to Case, $\theta_{JC}$ | | 3.4 | | ºC/W | 20 lead QFN package |

[1] Typical specification is not 100% tested. Performance guaranteed by design and/or other correlation methods.

## TYPICAL PERFORMANCE CHARACTERISTICS

**Figure 2 - Feedback Error Amplifier $V_{REF}$ vs. Junction Temperature**

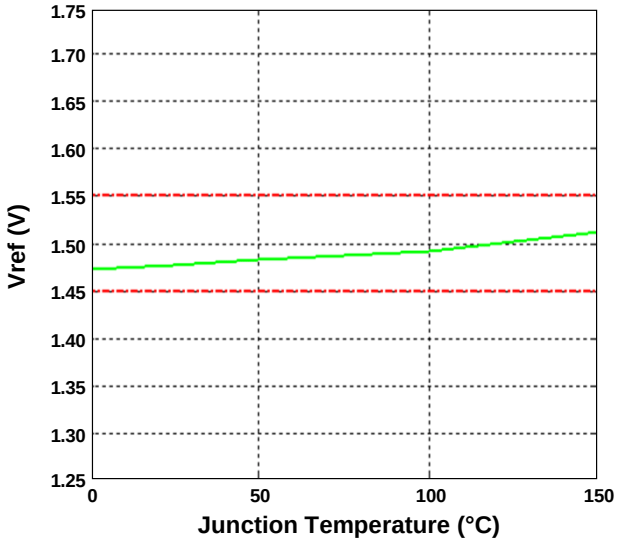



**Figure 3 - VDD5 vs. Junction Temperature**

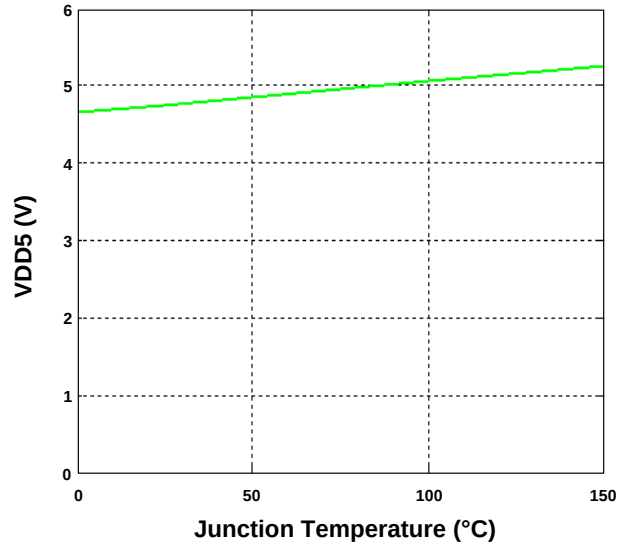



**Figure 4 - VDD5 vs. $V_{IN}$**

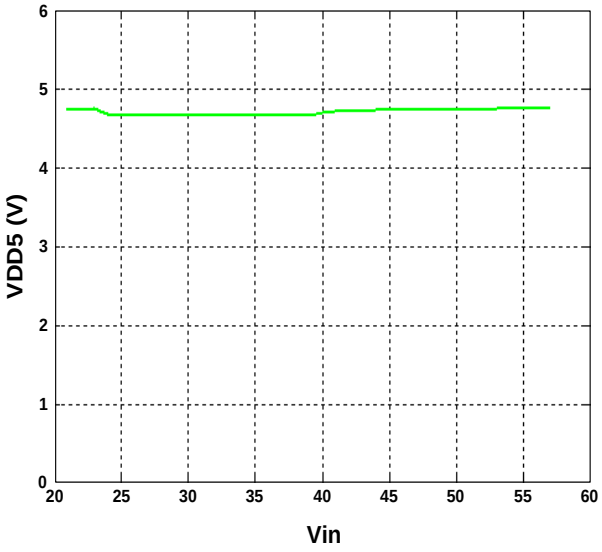



**Figure 5 - DC Current Limit vs. Junction Temperature**

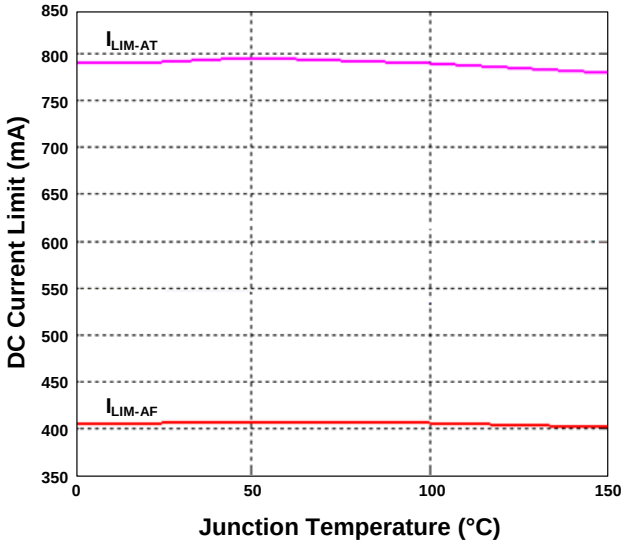


**Figure 6 - $R_{DSON}$ vs. Temperature @ 350mA, 48V**

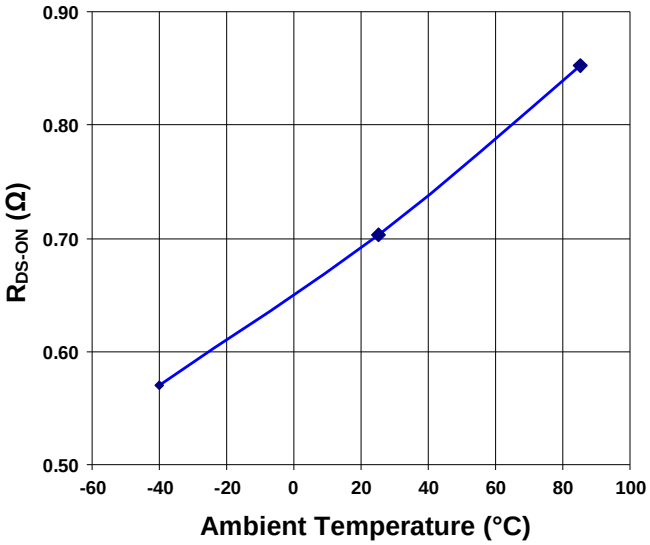



**Figure 7 - OSC vs. Temperature**

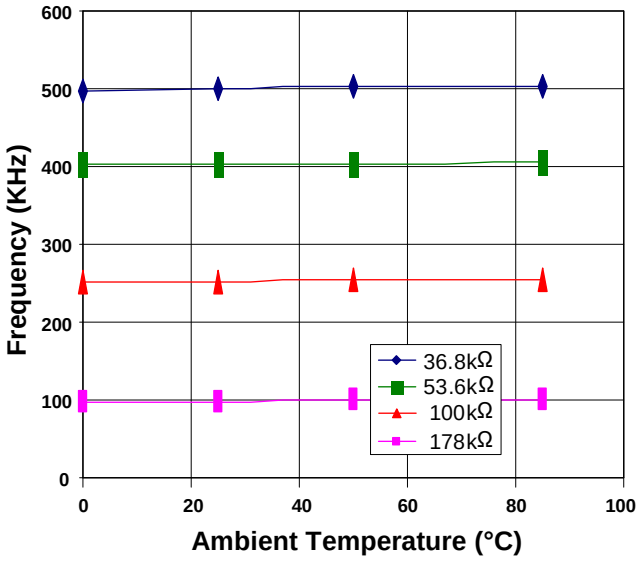



**Figure 8 - 48V $V_{DD}$ Load Regulation vs. Temperature**

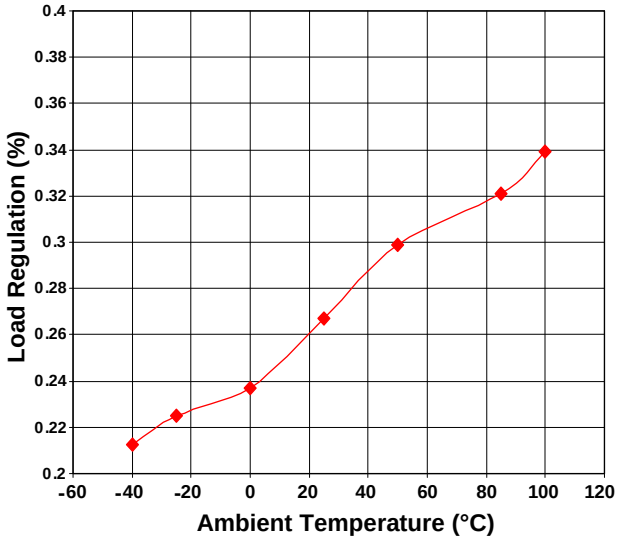



**Figure 9 - Inrush Current vs. Temperature**

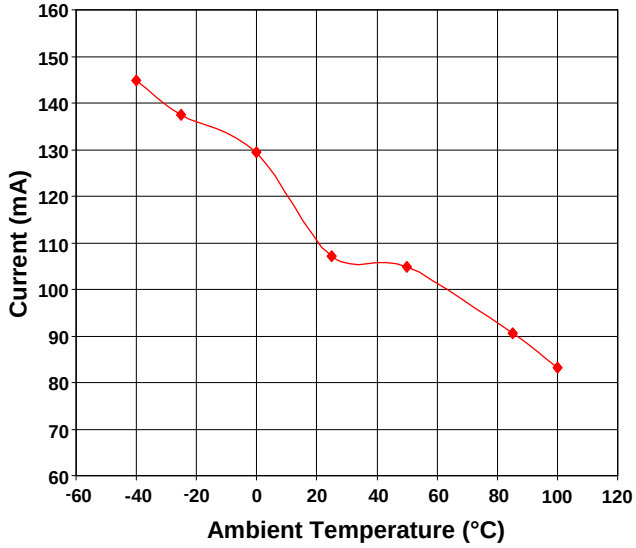


**Figure 10 - 48V $V_{DD}$ NDRV vs. Temperature**

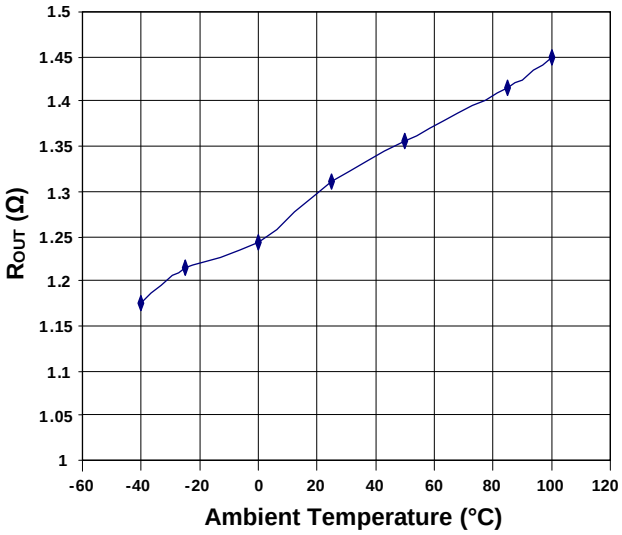



**Figure 11 - Comp Source vs. Temperature**

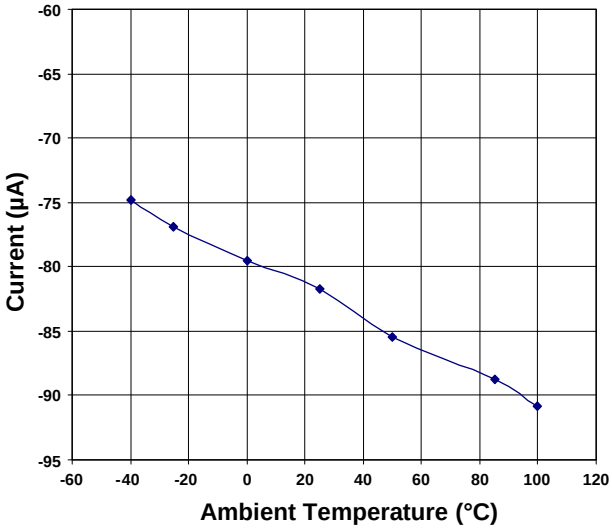



**Figure 12 - Comp Sink vs. Temperature**

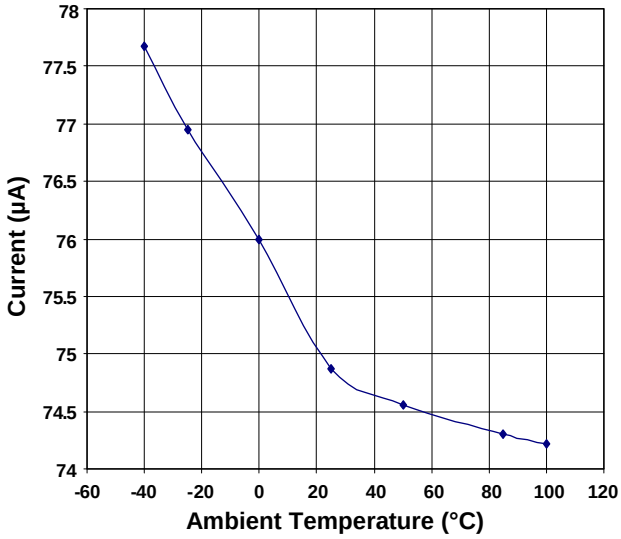



**Figure 13 - Example of VDD48I / VDD48O / Converter**

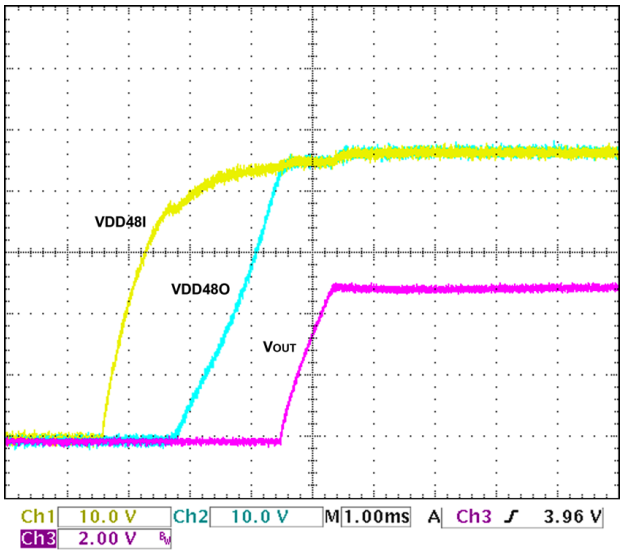


**Figure 14 - PI Input Voltage and Current / ATDET**

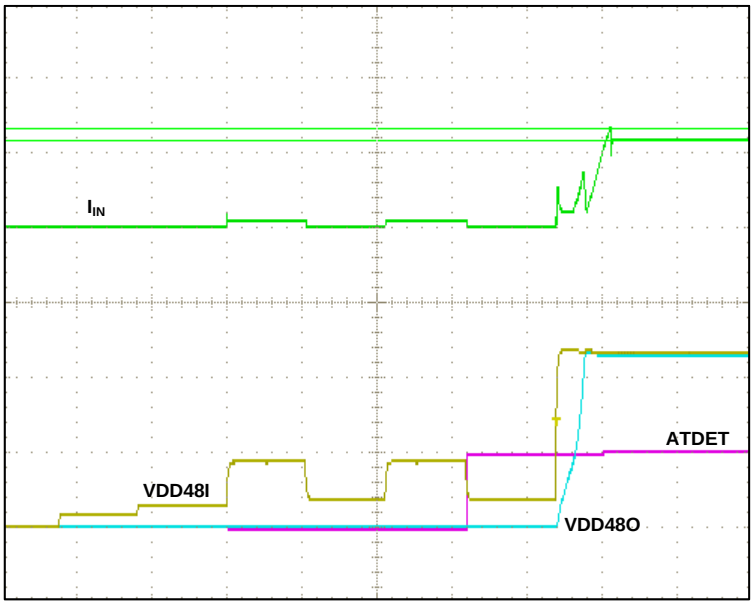



**Figure 15 - 3.3V 30W DC-DC Efficiency vs. Load**

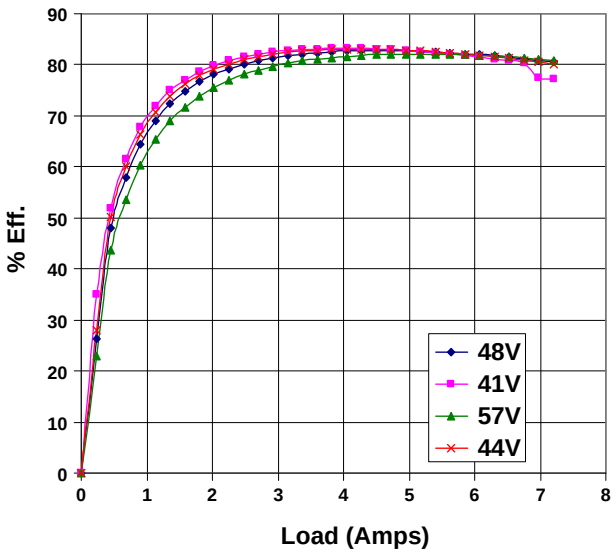



**Figure 16 - 3.3V 30W End-End Efficiency vs. Load**

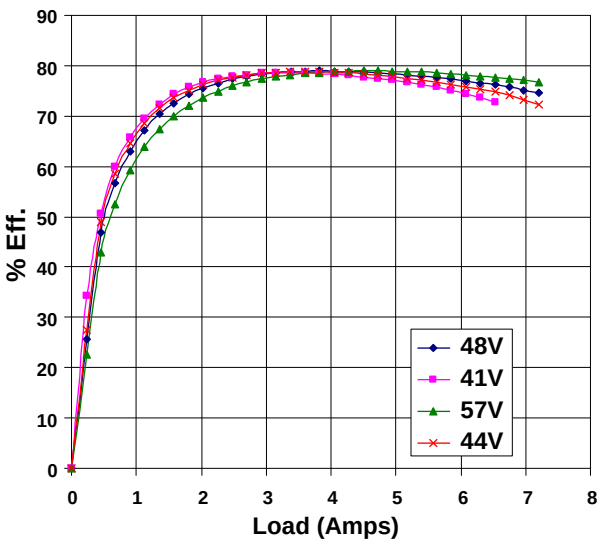


**Figure 17 - 3.3V 30W Load Regulation**

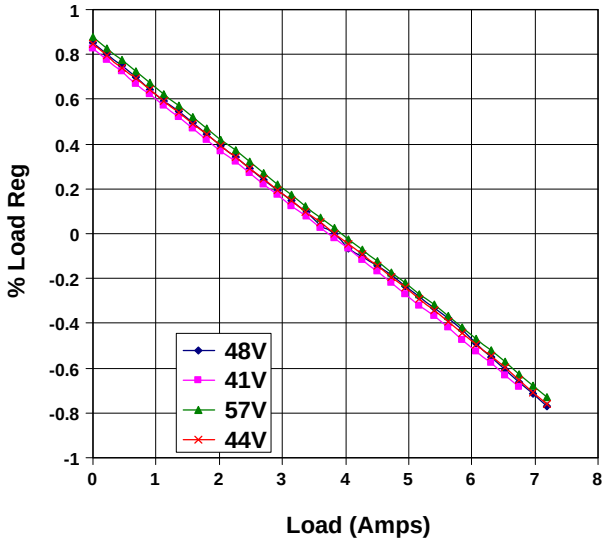



**Figure 18 - 3.3V 30W Line Regulation**

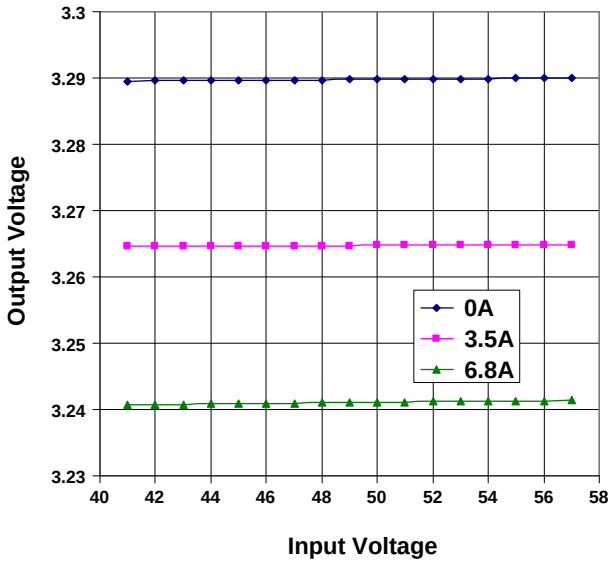



**Figure 19 - 5V 30W DC-DC Efficiency vs. Load**

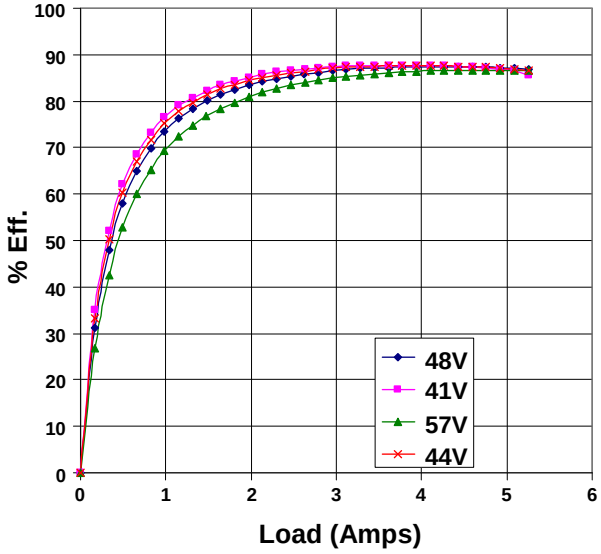



**Figure 20 - 5V 30W End-End Efficiency vs. Load**

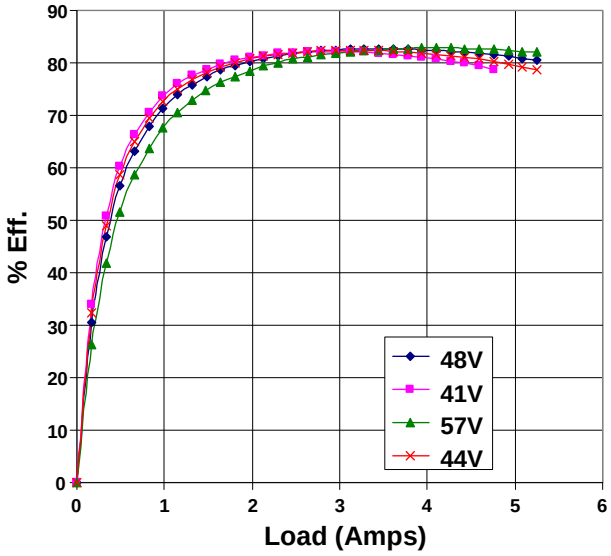


**Figure 21 - 5V 30W Load Regulation**

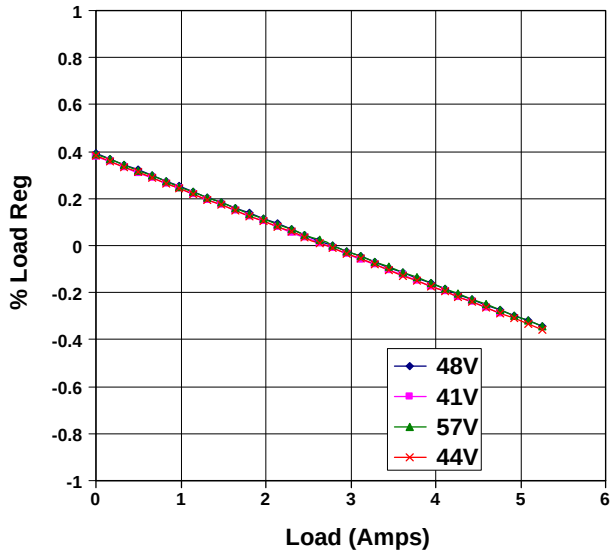



**Figure 22 - 5V 30W Line Regulation**

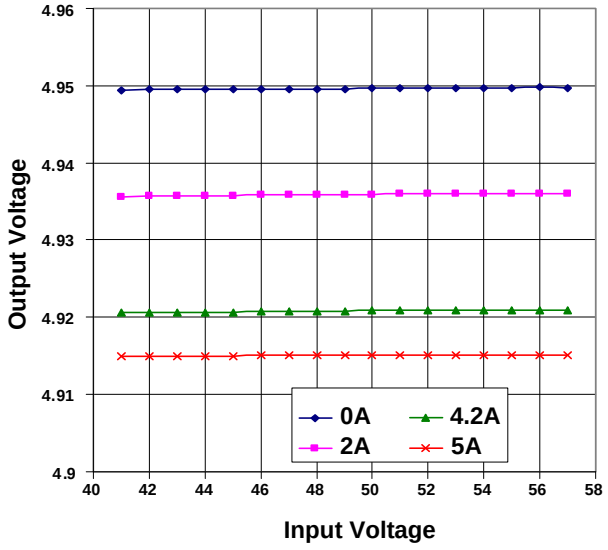



**Figure 23 - 12V 30W DC-DC Efficiency vs. Load**

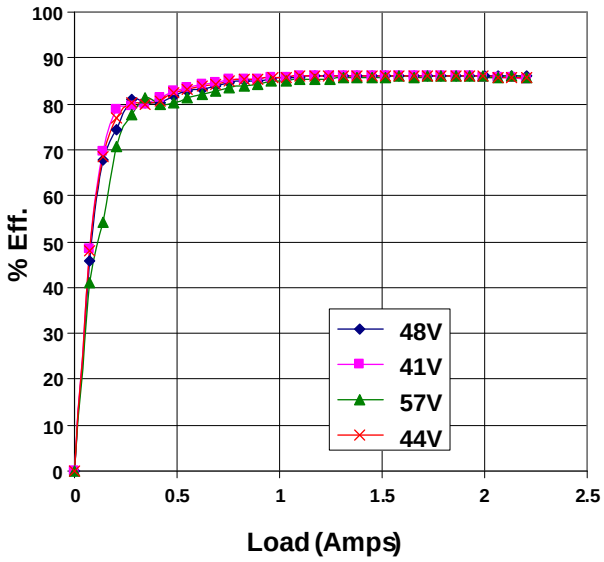



**Figure 24 - 12V 30W End-End Efficiency vs. Load**

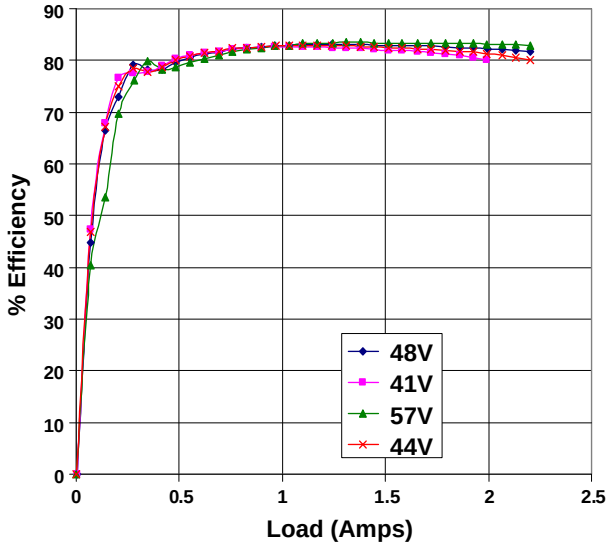


**Figure 25 - 12V 30W Load Regulation**

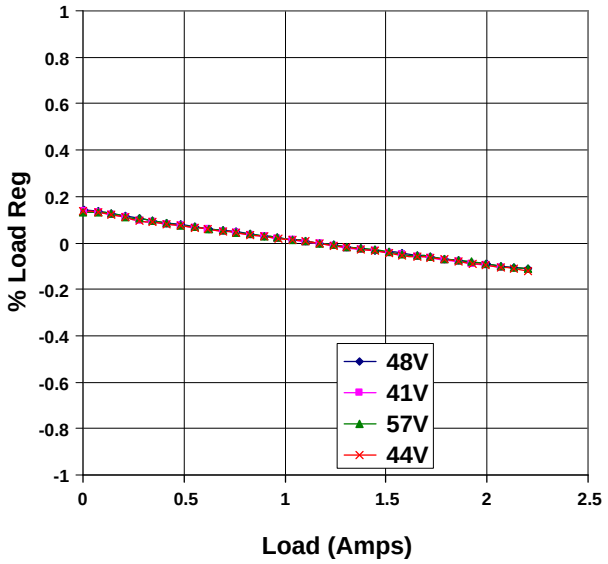
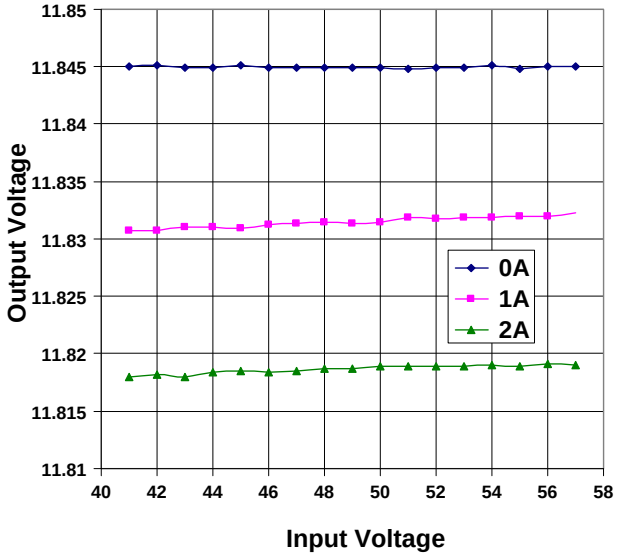



**Figure 26 - 12V 30W Line Regulation**



# FUNCTIONAL DESCRIPTION

## *Overview of PoE*

Power over Ethernet (PoE) offers an economical alternative for powering end network appliances, such as IP telephones, wireless access points, security and web cameras, and other powered devices (PDs). PoE standards IEEE® Std. 802.3af and 802.3at are intended to unify the delivery method of usable power over Ethernet cables to remotely powered client devices. These standards define a method for detecting and querying PDs and then supplying a range of current levels based on the power class the device belongs to. By employing this method, designers can create systems that predict and minimize power usage, allowing the maximum number of devices to be supported on a powered Ethernet network.

The power source that provides current through the Ethernet cables to remote devices is referred to as the Power Sourcing Equipment (PSE). The powered device (PD) on the other end of the Ethernet cable negotiates for and receives the agreed-upon power. IEEE® Std. 802.3af limits PSE power delivery to <13W at the PD input (Type 1 PD). IEEE® 802.3at allows for >13W power levels (Type 2 PD).

The PSE uses the following 802.3af sequence to detect a connected PD, determine how much power it requires and then initiate supply current to the device:

- **Reset** — Power is withdrawn from the PD if the applied voltage falls below a specified level.
- **Signature Detection** — The PSE detects and evaluates whether the PD is a valid PoE device.
- **Classification** — The PSE reads the power requirement of the PD. The Classification level identifies how much power the PD will require from the Ethernet line. This permits optimum use of the total power available from the PSE. Classification is considered optional by IEEE® standard 802.3af-2005 but IEEE® standard 802.3at-2009 requires Type 2 PSE to classify the PD for mutual identification.
- **On** — Operational state, during which the PSE provides the allocated power level to the PD.

This sequence occurs as a progressively rising voltage level from the PSE. It is designed to prevent high voltages from being present on an Ethernet line that does not have a valid PD attached (for user and non-PoE device safety).

To design PoE systems according to IEEE® standards, the following constraints apply:

**Table 6 - PoE Requirements**

| Requirement | Value |
|---|---|
| Maximum Type 1 PD input power | 12.95W |
| Maximum Type 2 PD input power | 25.5W |
| Output voltage from Type 1 PSE | 44-57V |
| Output voltage from Type 2 PSE | 50-57V |
| Minimum operating current limit, Type 1 @ PSE min output voltage | 350mA |
| Minimum operating current limit, Type 2 @ PSE min output voltage | 600mA |
| Line resistance, Type 2 operation | 12.5Ω |
| Input voltage at Type 1 PD interface | 37V-57V |
| Input voltage at Type 2 PD interface | 42.5V-57V |

## *AS1138 PoE Design*

To help designers meet these requirements, the AS1138 is a fully integrated PoE PD controller for Type1 and Type2 PD implementations. The AS1138 meets all system requirements for the IEEE® 802.3 standard for Ethernet and all power management requirements for IEEE® standard 802.3at-2009.

The AS1138 acts as an interface to the PSE, performing all detection, classification, and inrush current limiting control necessary for compliance with the PoE standards. An internal MOSFET and control circuit limits the inrush and steady-state current drawn from the Ethernet line. External diode bridges protect against polarity reversal, to provide alternative A and B detection.

The AS1138 also passes the 8kV Contact Discharge and 15kV Air Discharge requirements, tested per IEC 61000-4-2. EMI compliance of AS1138-based designs has been verified for CISP22 and FCC Class-B radiated and conducted emissions

## POWER FEED ALTERNATIVES FOR 10/100/1000 ETHERNET SYSTEMS

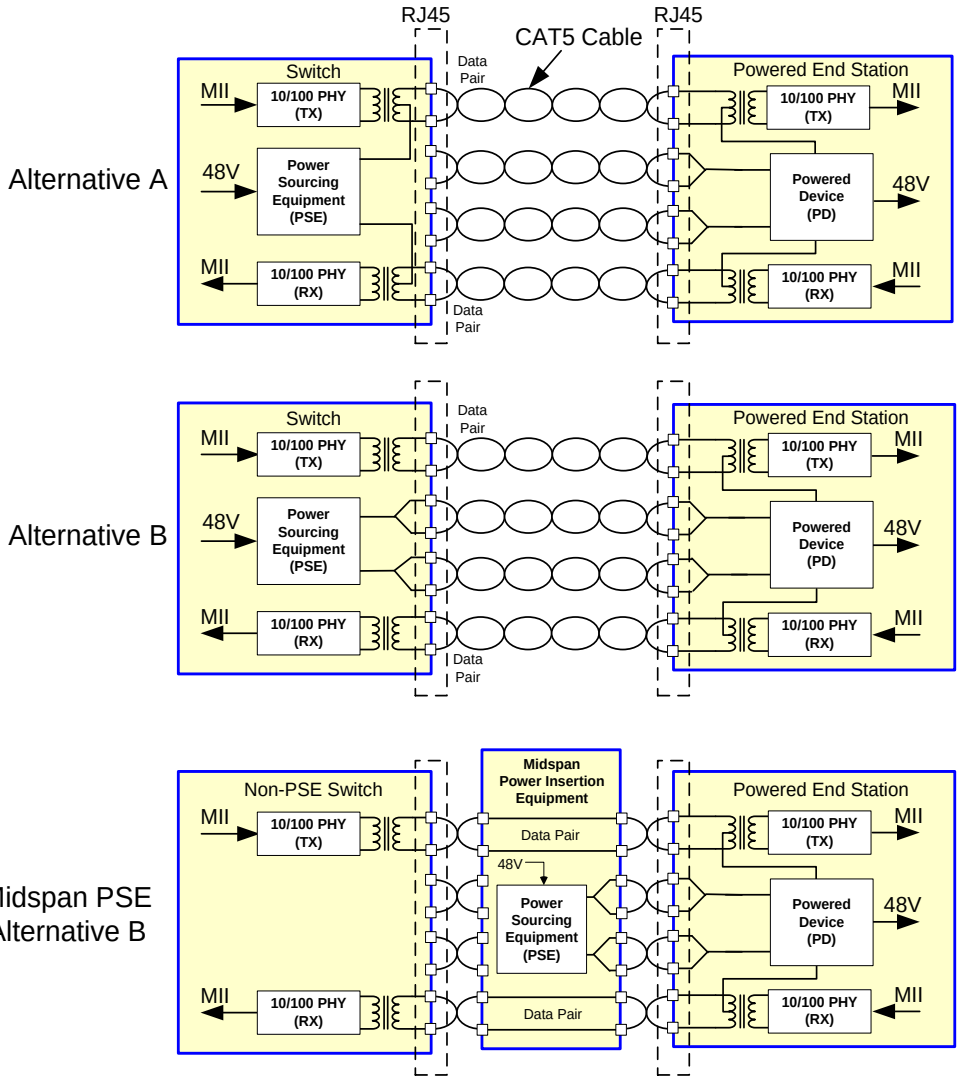
The Power Sourcing Equipment (PSE) supplies power to a single PD per node. A PSE located in the Data Terminal Equipment or Repeater is called an endpoint PSE, while a PSE located between MDIs is called a Mid-span PSE. Figure 27 illustrates the power feed options allowed in the 802.3at-2009 standard for 10/100/1000 Ethernet systems.

In Alternative A, a PSE powers the end station by feeding current along the twisted pair cable used for the 10/100/1000 Ethernet signal via center taps on the Ethernet transformers. On the line side of the transformers for the PD, power is delivered through pins 1 and 2 and returned through pins 3 and 6.

In Alternative B, a PSE powers the end station by feeding power through pins 4, 5, 7 and 8. In a 10/100/1000 system, this is done through the center taps of the Ethernet transformer. In a 10/100 system, power is applied directly to the spare cable pairs without using transformers.

The IEEE® Std. 802.3at-2009 standard is intended to be fully compliant with all existing non-powered Ethernet systems. As a result, the PSE is required to detect via a well-defined procedure whether or not the connected device is PD compliant and classify (optional in legacy 802.3af-2005 applications) the needed power prior to supplying it to the device. Maximum allowed voltage is 57V to stay within SELV (Safety Extra Low Voltage) limits.

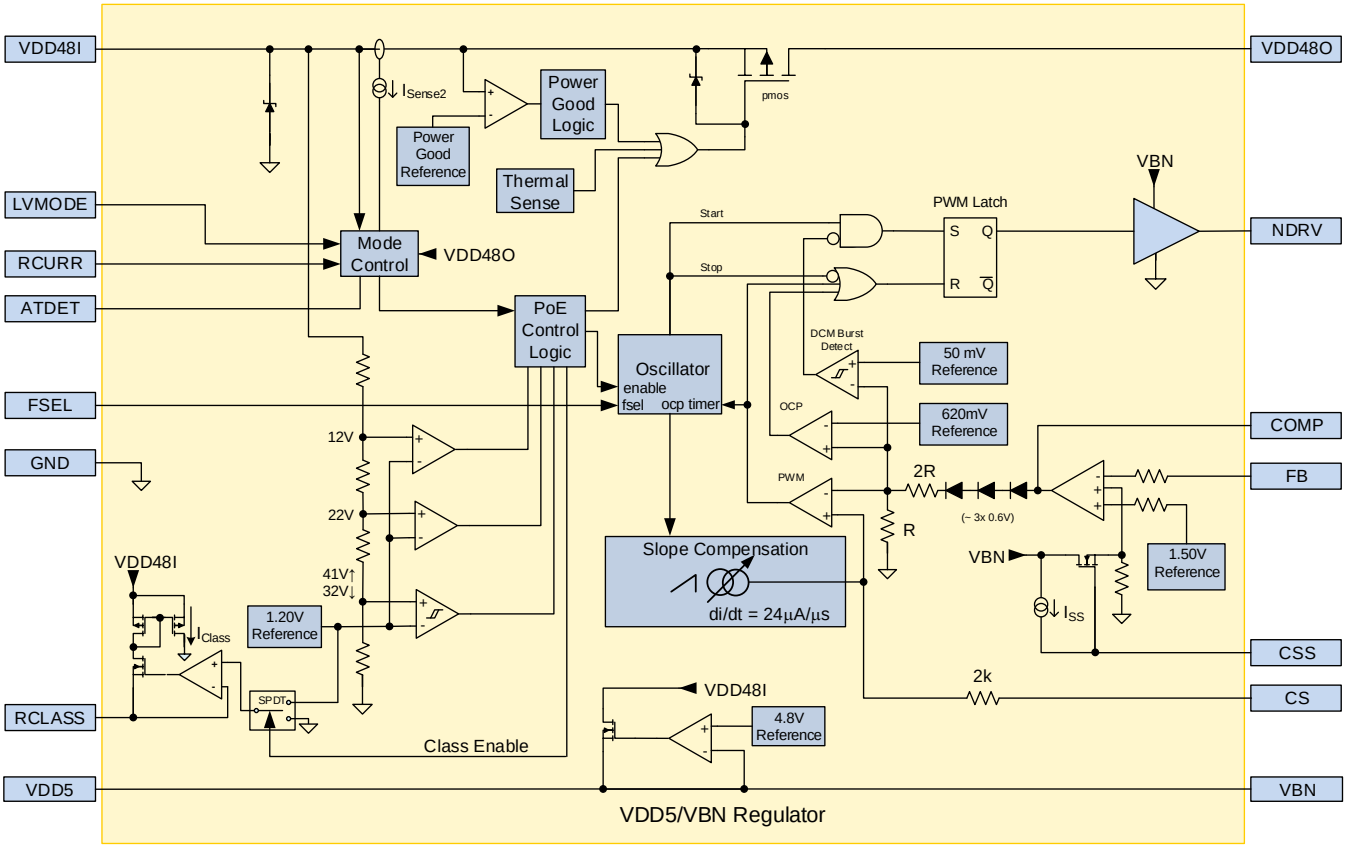
**Figure 27 - IEEE® Std. 802.3at-2009 Power Feeding Schemes for 10/100 Systems**



## AS1138 OVERVIEW

The AS1138 is a fully integrated PD that provides the functionality required for Power-over-Ethernet (PoE) applications. The optimized architecture reduces external component cost in a small footprint while delivering high performance.

**Figure 28 - AS1138 Top-Level Block Diagram**



## Rectification and Protection

To protect against polarity reversal, an external diode bridge is required. In conjunction with the external diode bridge, the AS1138 provides over-voltage and transient protection on the line side of the Hot-Swap FET.

The AS1138 is implemented in a robust 100V process technology. By integrating robust input protection circuitry, Kinetic has produced a solution that provides much faster response to surge events. The design also limits stray surge current from passing through sensitive circuits, such as the Ethernet PHY device and enables low-impedance safe discharge paths directly to earth ground. The protection circuit has been carefully designed to ensure that during these surge events, where currents can reach as high as 30A, voltages do not exceed critical breakdown and spark gap limits, protecting the PD from damage by the event. This enables system designers to achieve 15kV/8kV Air/Contact Discharge system ESD performance.

## PD Controller

The AS1138 PD Control Interface is designed to provide full PD functionality for IEEE® 802.3af and 802.3at compliant systems, with programmable support for standard PD control functions.

The PD Controller provides the following major functions:

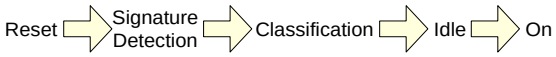
- A resistance/capacitance connection path for the detection signature.
- Classification current for power classification.
- Full 30Watt PD supply capability
- Power management and thermal protection override, including UVLO (Under Voltage Lock Out).
- ATDET signal output when connected to a Type 2 PSE that can deliver more than 13Watts.
- 2-Event Physical Layer classification.
- Maintain Power Signature feature.

## Modes of Operation

The AS1138 has five operating modes:

1. **Reset** — all blocks are disabled.
2. **Detection** — the external PD detection signature resistance / capacitance components are applied across the input.
3. **Classification** — PD indicates power requirements to the PSE via a Single-Event Classification for 802.3af or a 2-Event Physical Layer Classification for 802.3at.
4. **Idle** — this state is entered after Classification, and remains until full-power input voltage is applied.
5. **On** — The PD is enabled, and supplies power to the DC-DC controller and the local application circuitry.

As the supply voltage from the PSE increases from 0V, the AS1138 transitions through the modes of operation in this sequence:




If no PSE or local power supply is present, line voltage will be zero, which will hold the AS1138 in the Reset state. The AS1138 does not affect the Ethernet link function.

### Reset

When the voltage supplied to the AS1138 drops below the minimum valid detection voltage (i.e. <2.7V), the chip will enter the Reset state. While in Reset, the power supply to the PD is disconnected, the AS1138 consumes very little power and the device reverts to the pre-detection status.

### Detection Mode

During the detection sequence, the PSE applies a voltage to the PD to read its detection signature. The reading of the signature determines if a PD is present.

During detection, the PSE applies two sequential voltages, 1V or more apart, within the detection voltage range of 2.7V to 10.1V. It extracts a detection signature resistance value from the incremental I-V slope. Valid I-V slope resistance values are between 23.75kΩ and 26.25kΩ.

With the AS1138, detection signature resistance is generated by an external resistor connected between VDD48I and GND. Typically this is a 26.7kΩ, 1% resistor. With this value of $R_{SIGNATURE}$, the PSE normally detects a total effective signature resistance of approximately 25kΩ, which is centered within the 802.3af/at specification range of 23.75kΩ to 26.25kΩ.

Valid PD detection also requires a valid detection signature capacitance of 0.05 to 0.12uF at 2.7 to 10.1V, and 1.9V maximum offset voltage, per the IEEE® 802.3af/at standard, measured at the PD input connector. AS1138 detection signature capacitance is generated by an external 0.1uF capacitor connected between VDD48I and GND. The offset voltage is mainly provided by the external diode bridge voltage drop.

### Classification Mode

Each class represents a power allocation range for a PD to assist the PSE in managing power distribution. IEEE® Std. 802.3at defines classes of power levels for PDs, listed in Table 7. The AS1138 supports 2-Event Physical Layer classification, per IEEE® Std. 802.3at, as shown in Figure 14 and Figure 30.

The AS1138 identifies the PSE as either Type 1 or Type 2. If the 2-Event method is detected by the PD controller during the classification stage, it asserts the ATDET pin High, indicating connection to a Type 2 PSE. If the PD controller detects only single-event classification, it identifies the PSE to be Type 1 and the ATDET pin is asserted low.

In real applications, noise or transient ringing on the line during classification phase can lead to false 2-event classification or Type 2 PSE detection. To prevent such false positives, the AS1138 integrates a proprietary digital

filter to filter out noise events as long as 100uS during the classification phase, ensuring a very reliable AT Detection.

If a PSE is Type 1, to classify the AS1138, the Type 1 PSE presents a voltage between 14.5V and 20.5V to the PD and determines its class by measuring the resulting PD load current.

If a PSE is Type 2, in order to classify the AS1138 as the Type 2 PD, AS1138 has to be set as Class 4 (classification setting shown in Table 7), so that AS1138 returns a Class 4 signature.

The AS1138 allows the user to program the classification current via an external resistor connected to the RCLASS pin. Current, power levels and programming resistor values for each class are shown in Table 7. Note that for Class 0, RCLASS pin needs to be Pulled Up to VDD5 pin. This can be a direct short to VDD5 or using a resistor up to 100kΩ.

Use the following equation to determine the typical classification current:

$$I_{Class}[mA] = 2.0 + \frac{2360}{R_{Class}[k\Omega]} \quad (1)$$

Tolerance = Maximum of ±1.8mA or ±9%

$R_{CLASS}$ > 63.4kΩ

Once the classification process is done, the PD removes the classification current to conserve power.

Note: During the classification of a Type 2 PD, the PSE outputs a sequence of voltage signals (Class 1, Mark 1, Class 2, Mark 2, and Class 3) within the specific timing requirement. The PD has to respond within the limit range of voltage/current/impedance for each event according to section 33.3.5 PD Classifications of 802.3at standard.

**Table 7 - Classification Settings**

| Class | Power (W) | $I_{CLASS}$ (mA) | $R_{CLASS}$ (kΩ) |
|---|---|---|---|
| 0 | 0.44-12.95 | 0-4 mA | Pull-up (0-100kΩ) to VDD5 pin |
| 1 | 0.44-3.84 | 9-12 mA | 280kΩ, 1% |
| 2 | 3.84-6.49 | 17-20 mA | 143kΩ, 1% |
| 3 | 6.49-12.95 | 26-30 mA | 90.9kΩ, 1% |
| 4 | 12.96-25.5 | 36-44 mA | 63.4kΩ, 1% |

### Idle Mode

After the classification process, the PD enters Idle mode while it waits for On-state power delivery from the PSE. PD Current usage is limited to monitoring circuitry to detect the On-state voltage threshold.

### On State

In the On state, the AS1138 is supplying power across the Ethernet line(s) to the PD. At a voltage at or below 42V, the PD turns on and full power is available via the AS1138 DC-DC Controller

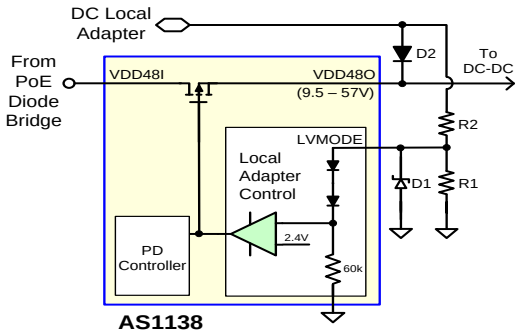
## *Local Power Mode (LVMODE)*

The LVMODE pin can be used in applications where the PD appliance is designed to draw power from either the Ethernet cable or an external DC local power adapter. The LVMODE pin is a current-mode input pin, with low and high thresholds as defined in the parametric tables (Table 4). The LVMODE is asserted when the input current exceeds the IIH threshold, and is de-asserted when the input current is below the IIL threshold. If LVMODE operation is not desired, the LVMODE pin should be connected to GND.

Figure 29 below shows a simplified internal implementation and external application circuit required to use the LVMODE feature. When power is applied at the local adapter input, the AS1138 enters Local Voltage Mode. This opens the internal Hot-Swap FET switch while the DC-DC converter is in operation.

In this configuration, local power always takes priority, even in presence of PoE power, irrespective of their relative voltages. If local power is removed, the device will exit Local Voltage Mode operation and PoE power will be used, if available.

**Figure 29 - LVMODE Implementation**




Local power is inserted at the VDD48O node through an external diode (D2). Use of a low reverse-leakage diode is recommended (<350uA, at worst case temperature). This ensures that when there is no local power, PoE voltage at the VDD48O node will not falsely pull up the LVMODE pin due to high reverse leakage through the diode. Please see Table 8 for part number information.

An appropriate ratio of R2 and R1 resistors should be used to ensure proper operation across all supply voltages. Table 8 lists appropriate choices of R2 and R1 resistors to work with a variety of popular local adapter DC voltages. Though a common value of R2 and R1 can be used across the whole range of local supply voltages from 9.5V to 57V, using different value pairs, per Table 8, will minimize power consumption. The maximum input voltage at the LVMODE pin should not exceed 6V, so a Zener diode (D1) is recommended to limit transient voltage excursions at the pin.

Since the input current at the LVMODE pin defines its state, it is not recommended to drive other circuits or components directly from the LVMODE node (such as an LED) that might draw current. LEDs or current-absorbing components may be driven directly from the Local Supply pin.

The AS1138 internal DC-DC controller is designed to operate with input voltages of 9.5V-57V, to allow applications to take advantage of the LVMODE feature. Besides configuring the device for operation from a local power source, the external power transformer must also be designed to ensure proper operation across the complete input range.

**Table 8 - LVMODE Configuration**

| Local Voltage Range | Recommended Local Adapters | R2 | R1 |
|---|---|---|---|
| 9.5V-57V | 12V, 18V | 2.74kΩ | 4.02kΩ |
| 20V-57V | 24V, 30V | 11.3kΩ | 4.02kΩ |
| 32.4V-57V | 36V, 48V | 20kΩ | 4.02kΩ |

Diode D1: 5.6V Zener, BZT56V

Diode D2: S3B (100V/3A, worst-case reverse leakage <250µA), use of a low reverse-leakage diode with worst-case reverse leakage under high temperature <350µA is recommended.

## PD CONTROLLER POWER AND THERMAL PROTECTION

The AS1138 provides the following PD controller power and thermal protection:

- Under Voltage Lock Out (UVLO)
- Inrush Current Limit with integrated current sense
- Thermal Limit / Protection

### *Under Voltage Lock Out (UVLO)*

The AS1138 contains line Under-Voltage Lock Out (UVLO) circuitry to determine when to power on the PD. If the PSE supply voltage at PD PI is equal or greater than UVLO $V_{IN\_RISING}$, the AS1138 PD will power on and run; if the PSE supply voltage at PD PI drops below UVLO $V_{IN\_FALLING}$, the AS1138 PD will power off. The PD circuit controls power flow to the DC-DC controller, to protect the PD from erratic operation or damage.

### *Inrush Current Limit / Current Sense*

Inrush limiting maintains the cable voltage above the turn-off threshold as the input capacitor charges. This also prevents the PSE from going into current limit mode. The Current Limit/Current Sense circuitry also minimizes the PD on-chip temperature peaks by limiting both inrush and operating current.

Current is monitored with an integrated sense circuit that regulates the gate voltage on an integrated low-leakage power MOSFET. The power MOSFET can also be shut off completely by either the PD Controller, the Thermal Limit Protection circuitry or the insertion of a local power adapter that causes the LVMODE pin to be pulled high (via a resistor divider).

During the PD startup sequence, VDS across the Hot-Swap FET is momentarily high as the VDD48O output capacitance is charged up, as illustrated in Figure 14. During this state, the Hot-Swap FET experiences a high instantaneous power drop and heating. Therefore, it is recommended that during this startup sequence, the incoming current should only be utilized for the charging of the VDD48O node, to minimize the startup time and associated power drop across the FET. The primary PWM controller is designed to accommodate for VDD48O startup before drawing power from the line. However, if the application requires direct use of the VDD48O node for other functions, the startup of those circuits should be delayed until the VDD48O node has reached its full voltage level.

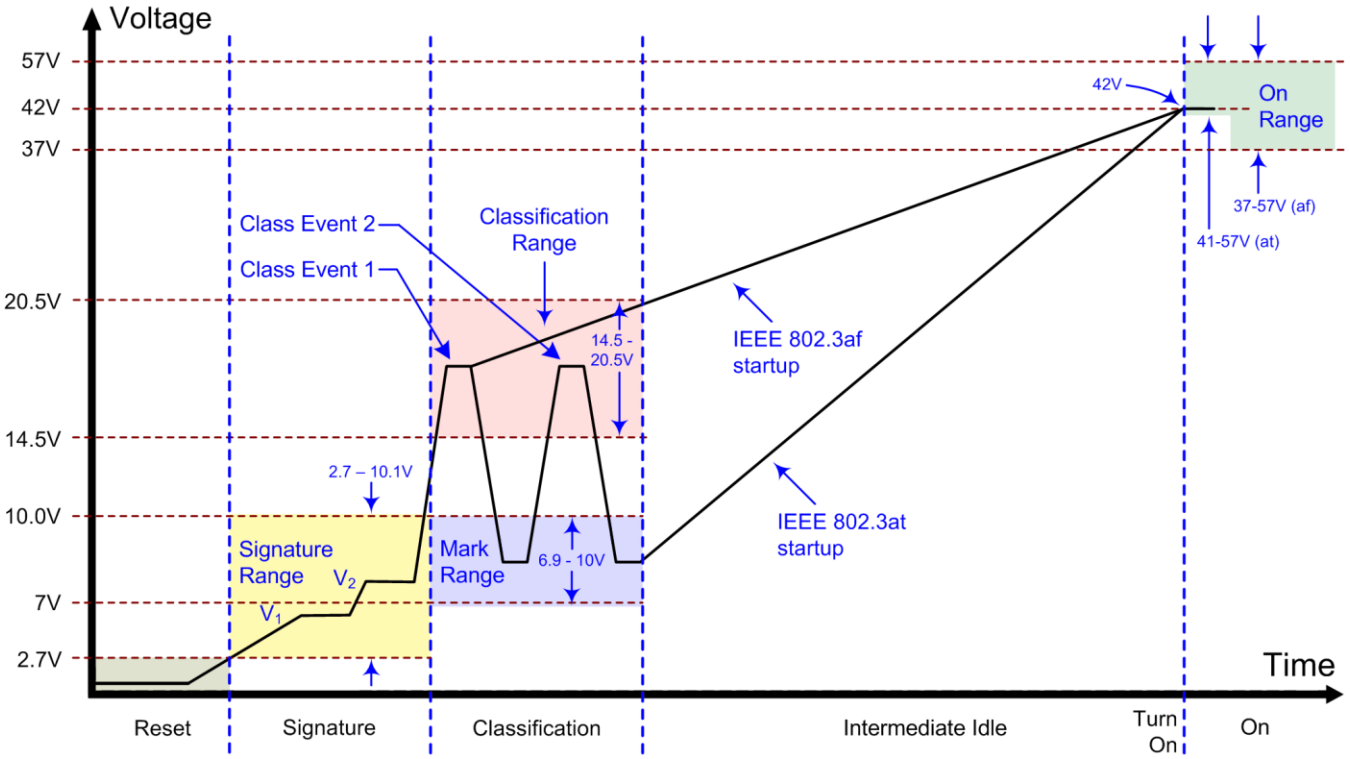
### *Thermal Limit / Protection*

The AS1138 provides thermal protection for itself by monitoring die temperature and reducing maximum current or disconnecting power as needed to prevent its pre-set thermal limits from being exceeded. Two-stage thermal current limiting is implemented, which reduces the operating current limit by 50% when the die temperature reaches 145˚C, and disables the power MOSFET switch above 165˚C. Normal current limits in both cases are re-applied when the die temperature returns below 125˚C.

## PoE POWER-ON STARTUP WAVEFORM

Figure 30 represents the power-on sequence for PoE operation. The waveform reflects typical voltages present at the PD during signature, classification and power-on.

**Figure 30 - 802.3at Typical Power-On Waveform**




1. Voltages $V_1$ and $V_2$ are applied by the PSE to extract a signature value.

2. The PSE takes current/impedance readings during Class/Mark Events to determine the class of the PD. At this time, the PD presents a load current determined by the resistance connected to the $R_{CLASS}$ pin.

3. After the PSE measures the PD load current, if it is a high-power PSE, it presents a mark voltage (6.9-10V), followed by a second classification voltage. The PD responds by presenting a load current as determined by the resistor on the $R_{CLASS}$ pin. After the PSE measures the PD load current the second time and determines that is can deliver the requested power, it moves into the On state by raising the voltage to approximately 42V.

## ATDET PIN

The ATDET output pin provides an indicator when 2-event classification is detected by being linked to a Type 2 PSE, or through the use of a local power supply that uses the LVMODE feature. This indicates system has more than 13W of available power. This pin can be used by the PD system controller to self-configure the application device based on available power.

If there is no local power present, ATDET will stay low during PD Reset, Detection and Classification phases. The ATDET pin will be set high once the PD recognizes the completion of the 2-Event Physical Layer Classification, as initiated by a Type 2 PSE. The pin will remain high and will only be reset low by the occurrence of a Reset or a power-down event. ATDET pin remains low if it identifies the PSE partner to be Type 1 during the Classification phase.

If LVMODE is asserted when supplying local power, the ATDET pin is forced high, irrespective of the PD mode. Please see Table 9 below for ATDET output definitions under various powering modes.

**Table 9 - ATDET Truth Table**

| ATDET Signal Status | PSE | |
|---|---|---|
| | Type 1 | Type 2 |
| LVMODE = Low | Low | High |
| LVMODE = High | High | High |

## DC-DC CONTROLLER

### Overview

The DC-DC architecture is a current-mode controller configurable with external components to fly-back, forward or buck topologies. Both non-isolated and isolated topologies are supported.

As part of a full system-level solution to control EMI, Kinetic has focused significant attention on reducing switching noise in the integrated power converters through unique methods of shaping FET driver waveforms. Ground bounce is also reduced by minimizing dV/dt switching noise.

The integrated DC-DC controller operates from a switched input voltage (VDD48O) and includes a programmable soft start and current limiting. Once input power is applied and enable signals are asserted, the DC-DC controller starts up. The controller provides a gate control signal, NDRV, to the external switching MOSFET and uses an external resistor to sense primary current in the transformer. It also provides for an 80% maximum duty cycle, programmable PWM switching frequency and a true voltage-output error amplifier.

### Programmable PWM Frequency

The FSEL pin allows the DC-DC converter switching frequency to be set externally. Placing a resistor between FSEL and GND sets the internal oscillator's frequency Table 10 identifies the resistor values for some commonly-used switching frequencies.

**Table 10 - PWM Switching Frequency Selection**

| Switching Frequency (kHz) | FSEL Resistor (kΩ, 1%) |
|---|---|
| 100 (kHz) | 178kΩ |
| 225 (kHz) | 100kΩ |
| 350 (kHz) | 53.6kΩ |
| 500 (kHz) | 36.8kΩ |

### Current-Limit/Current Sense

The DC/DC controller provides cycle-by-cycle current limit monitoring, via the CS input, to ensure that transformer current limits are not exceeded.

A short-circuit event is declared if the CS sensed current limit is triggered on 32 consecutive PWM clock cycles. Once a short-circuit event has been declared, the PWM will shut off for 256 cycles before a restart is attempted. This process will repeat indefinitely until the output short is removed.

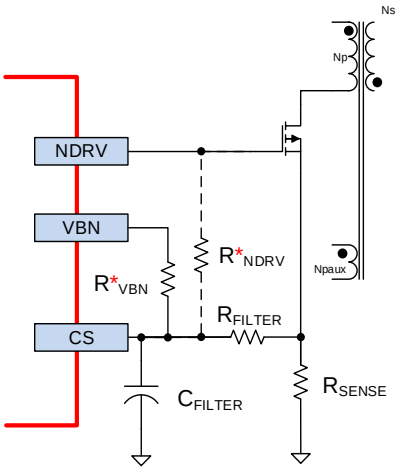
### Low Load Current Operation

The internal circuitry detects a low output power condition and puts the DC-DC Controller into a discontinuous operation mode (DCM burst). Burst mode operation occurs when the COMP pin voltage drops below ~ 2.00V.

In many applications it may be desirable to disable burst mode operation or reduce the load at which burst mode operation occurs. This can be accomplished by adding a DC offset to the current sense signal at the CS pin. Adding a pull-up resistor from either VBN or NDRV to CS provides the necessary offset voltage. Adding a minimum of 100mV of DC offset to CS will disable burst mode operation.

$$V_{CS(DC\,offset)} \approx VBN \cdot \frac{R_{FILTER}}{R_{VBN} + R_{FILTER}} \qquad (2)$$

**Figure 31 - Location of $R_{NDRV}$ or $R_{VBN}$ to Disable Burst Mode Operation**




* $R_{VBN}$ and $R_{NDRV}$ are alternate methods to add DC offset. Select one.

Burst mode should be disabled for synchronous rectified outputs. For diode rectified outputs, the load at which burst mode occurs may be reduced, but it is neither possible nor desirable to disable burst mode operation at very light or no load conditions.

### Compensation and Feedback

For isolated applications, loop compensation and output voltage feedback is generally provided by an opto-isolator circuit, and the Feedback pin (FB) is tied to ground. In these applications, the COMP pin is pulled up to approximately 4.8V by an internal current source. This pull-up can be the termination for an opto-isolator, or, an additional resistor can be used in parallel.

For non-isolated applications, a resistive divider network, connected directly to the FB pin, senses the output voltage. The internal error amplifier is connected to a 1.5V reference voltage and the control loop will servo the FB pin to this voltage. A capacitive/resistive network connected to the COMP pin provides loop compensation.

### Soft-Start

A capacitor is required on the CSS pin, and is used to provide a controlled application power supply startup.

Upon device power on, the capacitor on the CSS pin is slowly charged by the AS1138. In isolated designs this charging soft start voltage level limits the maximum voltage "seen" on the CS pin to:

$$V_{CS\_MAX} \approx V_{CSS} - 1$$

And since peak current detection is:

$$I_{PK} = V_{CS}/R_{CS}$$

the maximum Flyback output current ramps with $V_{CS}$, providing a soft start. For example, a 12V output flyback design with a max duty cycle of 45% and a CSS cap of 330nF will have a soft start of ~8ms.

For non-isolated designs, the soft start time ($T_{SS}$) in seconds for a given capacitor ($C_{CSS}$) is defined by the formula:

$$Tss = \frac{1.5 C_{CSS}}{10\mu A} \quad (3)$$

For example, in a non-isolated design, a 100nF capacitor creates a soft start time of ~15ms.

## DC-DC CONVERTER TOPOLOGIES

### Isolated Topologies

The DC-DC controller can be configured in several different isolated topologies. The Flyback mode is chosen when a minimum number of external components is desired, or there is a large step-down and the output voltage is < 7V.

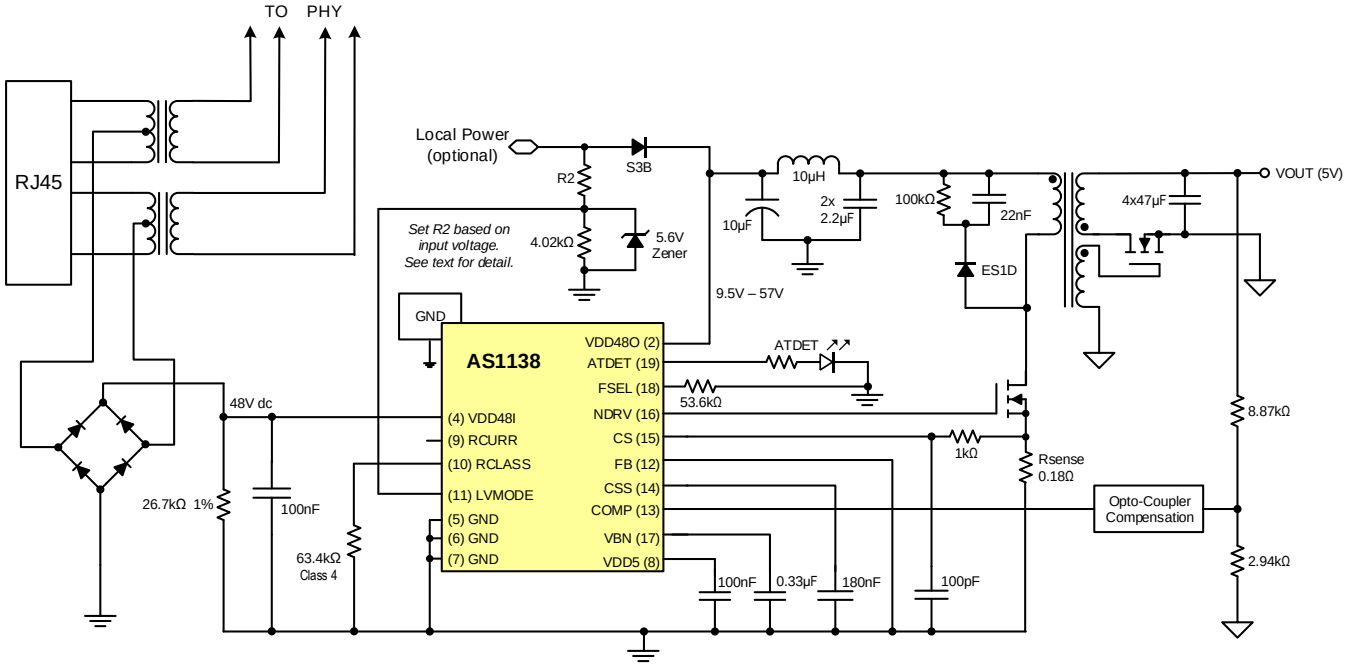
The Forward mode is chosen when lower switching noise is desired. Either of these isolated topologies can be designed for synchronous or non-synchronous operation, based on system requirements. A typical Isolated Synchronous Flyback design is shown in Figure 32.

### Non-Isolated Topologies

The Buck mode is used in non-isolated applications. This application uses inductor for energy storage, instead of a transformer. See Figure 33.

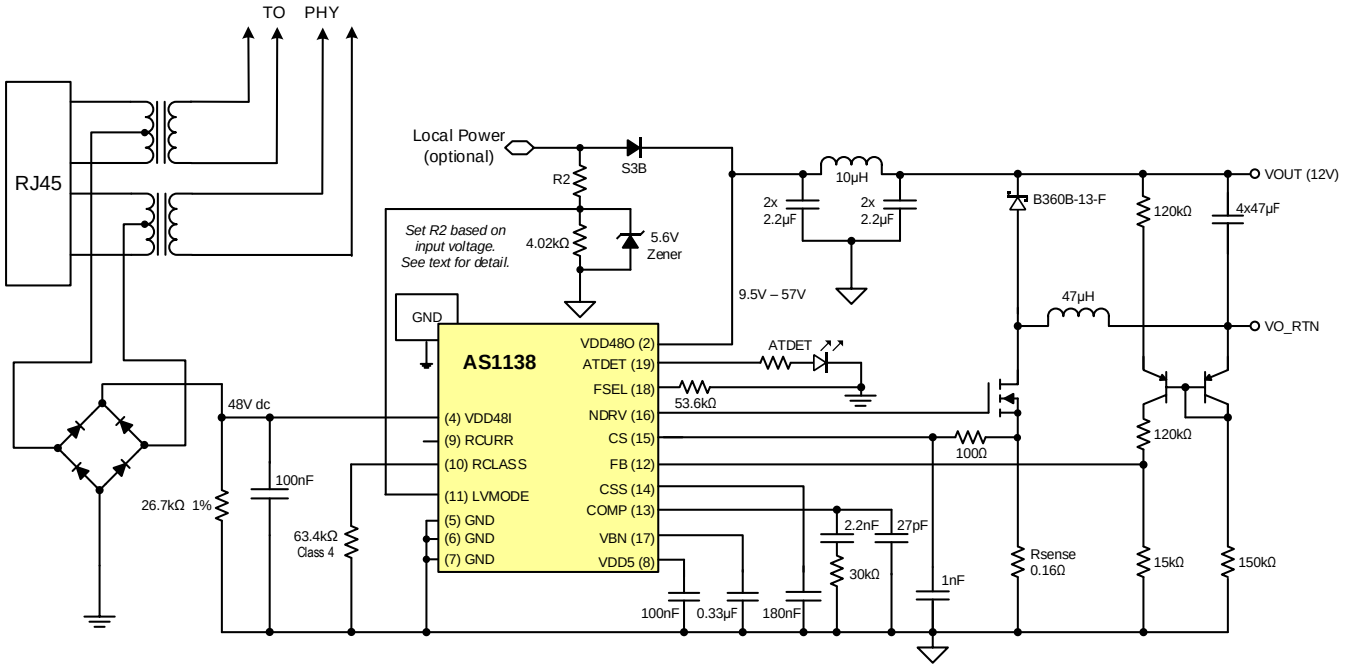
## APPLICATION CIRCUITS

**Figure 32 - PoE PD Controller with a High-Efficiency Isolated Synchronous Flyback DC-DC Converter**




Note: This is a simplified conceptual schematic. Please refer to the reference design documentation for detailed design and component information. Full PoE implementation will require two input diode bridges. For simplicity, only one is shown here.

**Figure 33 - PoE PD Controller with a Non-Isolated BUCK DC-DC converter**




Note: This is a simplified conceptual schematic. Please refer to the reference design documentation for detailed design and component information. Full PoE implementation will require two input diode bridges. For simplicity, only one is shown here.

## THERMAL DE-RATING AND BOARD LAYOUT CONSIDERATIONS

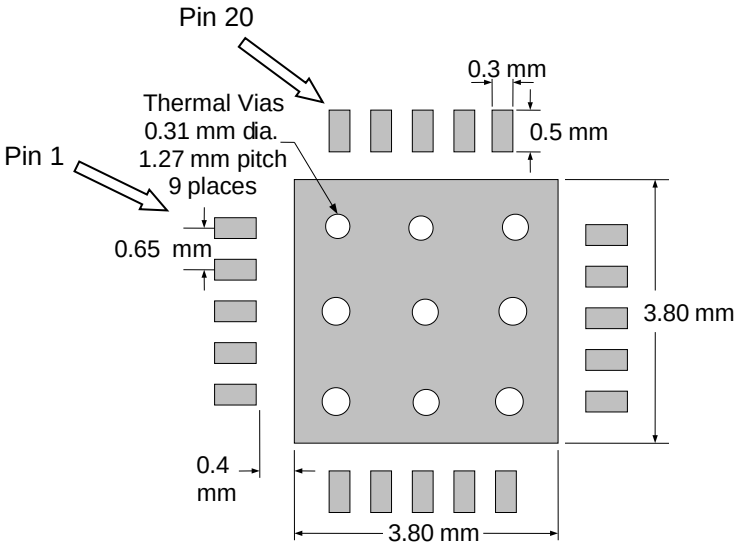
The AS1138 is capable of operating to an industrial temperature range of 85ºC in ambient air, without forced cooling. A thermal pad on the underside of the package dissipates the heat generated by the PD die.

In 30W applications, designers must consider thermal dissipation as an integral part of their system architecture and plan to remove heat via this pad.

If the PCB landing pattern is properly designed, the QFN package should exhibit a thermal resistance of $\Theta_{JA}$ = 31°C/W. For adequate heat dissipation, the board layout must include a ground pad which provides both the ground connection and dissipates the heat energy produced in the chip. Thermal vias are used to draw heat away from the PD package and to transfer it to the backside of the system PCB.

The recommended PCB layout for the AS1138 is shown in Figure 34 below:

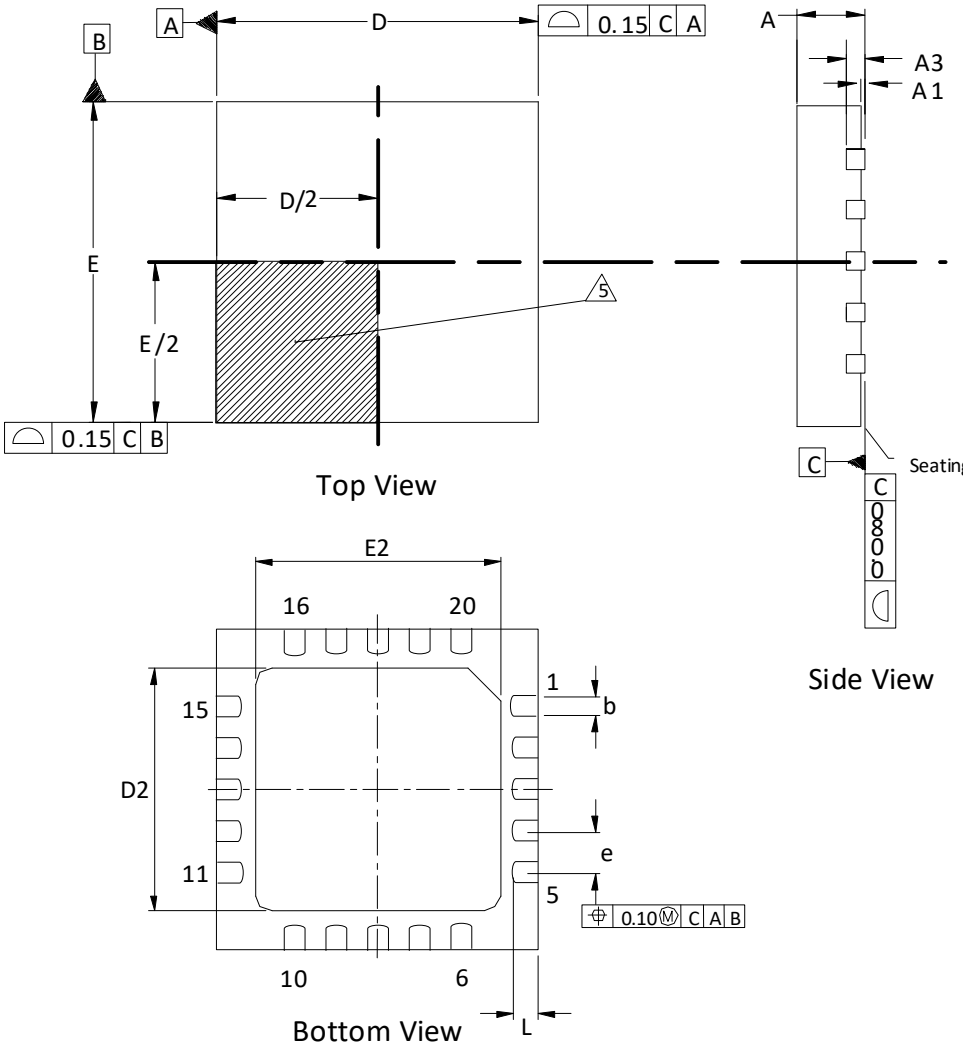
**Figure 34 - AS1138 PCB Footprint (Top View)**



## PHYSICAL DIMENSIONS

20 Pin QFN Package, 5mm X 5mm

**Figure 35 - Physical Dimensions**




| Common Dimensions | | | |
|---|---|---|---|
| | MIN. | NOM. | MAX |
| A | 0.80 | 0.85 | 0.95 |
| A1 | 0.00 | 0.02 | 0.04 |
| A3 | | 0.20 REF. | |
| D | 4.85 | 5.00 | 5.15 |
| D2 | 3.70 | 3.80 | 3.90 |
| E | 4.85 | 5.00 | 5.15 |
| E2 | 3.70 | 3.80 | 3.90 |
| L | 0.35 | 0.40 | 0.45 |
| N | | 20L | |
| b | 0.25 | 0.30 | 0.35 |
| e | | 0.650 BSC | |
| JEDEC | | MO-220-VHHC-2 | |

NOTES

1. Controlling dimensions in mm.
2. Dimension tolerances are ± 0.1 (angular tolerance ± 3°) unless otherwise specified.
3. All dimensions and tolerances conform to ANSI 14.5M-1994.
4. Co-planarity applies to exposed pad as well as the terminals.
5. Pin 1 location may be identified by either a mold or marked feature.
6. JEDEC reference MO-220.

# Important Notices

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