IEEE 802.3at PoE PD with Integrated DC-DC Controller

Features

- Fully supports both IEEE® Std. 802.3af-2005 and IEEE® Std. 802.3at-2009
- "2-Event" classification for 802.3at higher power PDs
- Robust Type 2 PSE detector with proprietary digital filtering line noise eliminating false positives
- IEC 61000-4-2/3/4/5/6 requirements for EMC Compliance
- Integrated Surge Protection for 15kV/8kV System level ESD Compliance
- Exceptional EMI performance
- Programmable DC current limit up to 730mA for 30W applications
- Seamless support for local power, down to 9.5V
- Low Rds-on Hot-Swap FET (typical 0.6Ω)
- Integrated Short-Circuit Protection
- Over temperature protection
- 5x5 mm, 20 lead QFN Package
- Industrial temperature range (-40°C to +85°C)

Applications

- Pan, tilt and zoom (PTZ), security and web cameras
- Voice over IP (VoIP) phones
- Wireless LAN access points, WiMAX terminals
- Point-of-sale (PoS) terminals, RFID terminals
- Thin clients and notebook computers
- Fiber-to-the-home (FTTH) terminals

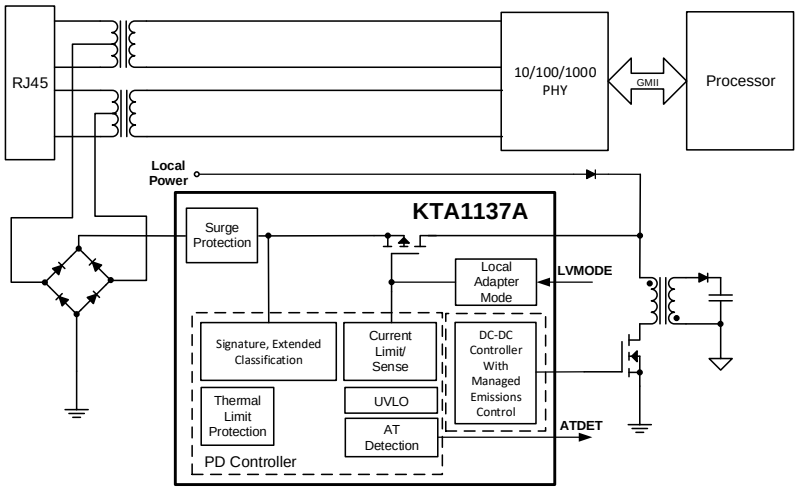
Brief Description

The KTA1137A is a single-chip, highly integrated CMOS solution for Power over Ethernet (PoE) Powered Devices requiring input power of up to 30Watts. Applications include Voice over IP (VoIP) Phones, Wireless LAN Access Point, Security Cameras, WiMAX Terminals, Point-of-Sales Terminals, RFID Readers, Thin Clients and Notebook computers.

The KTA1137A integrates input surge protection, a PD controller and a low-emission DC-DC controller. The KTA1137A implements all of the physical layer Powered Device (PD) functionality, as required by IEEE® 802.3af-2005 and IEEE® 802.3at-2009 standards. This includes 2-event classification, Type 2 PSE detection indicator (ATDET), PD detection, under-voltage lockout (UVLO), and Hot-Swap FET integration.

The KTA1137A has been architected to address both EM emission concerns and surge/over-voltage protection in PoE applications. The chip implements many design features that minimize transmission of system common-mode noise onto the Unshielded Twisted Pair (UTP). On-chip integration of surge protection provides faster response to surge events and limits stray surge current from passing through sensitive circuits, such as the Ethernet PHY. The device is designed to provide safe, low-impedance discharge paths directly to the earth ground, resulting in superior reliability and circuit protection.

Typical Applications



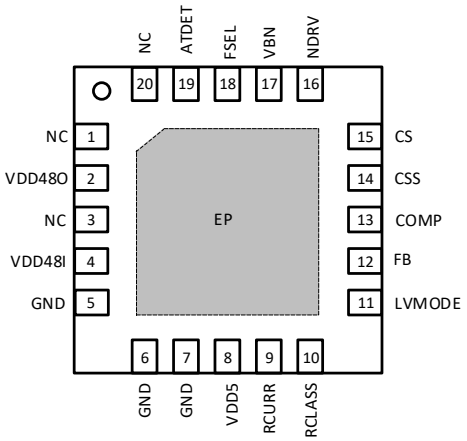
Pin Description

Pin #	I/O	Name	Function
1	-	NC	No Connect
2	P	VDD48O	Switched 48V supply output
3	-	NC	No Connect
4	P	VDD48I	48V positive bus pin, fed by the output of the external diode bridge. This bus requires the connection of a detection signature capacitor and resistor. Refer to Detection Mode section.
5	A	GND	Must be connected to paddle ground (GND)
6	A	GND	Must be connected to paddle ground (GND)
7	A	GND	Must be connected to paddle ground (GND)
8	O	VDD5	Internal 5 volts bus decoupling point
9	A	RCURR	Current limit pin. Connection to paddle ground sets the current limit to ILIM-AF (for 13W applications). Open circuit sets the current limit to ILIM-AT (for 30W applications).
10	A	RCLASS	Classification resistor connection
11	A	LVMODE	Local Voltage Mode. When pulled high, LVMODE opens the internal FET switch and keeps the DC-DC controller active. This is a current-mode input pin. It should be pulled to GND when not in use.
12	A	FB	DC-DC Controller feedback point
13	A	COMP	DC-DC Controller error amplifier compensation network connection
14	A	CSS	DC-DC Controller soft-start capacitor connection point (required).
15	A	CS	DC-DC Controller peak-current sense input (low side)
16	O	NDRV	DC-DC Controller N-MOSFET gate drive
17	O	VBN	DC-DC Controller low-side supply decoupling
18	I	FSEL	Frequency Select. This pin sets the switching frequency of the DC-DC converter.
19	O	ATDET	IEEE® 802.3at-2009 PSE detects. High level output indicates availability of higher system power, either via connection to a Type 2 PSE, or via a local power supply.
20	-	NC	No Connect
EP	Exposed Pad	GND	Local analog ground. This is the negative output from the external diode bridge and is not isolated from the line input.

Key: I = Input, O = Output, A = Analog Signal, P = Power

20-Pin QFN

Top View



Top Mark

XX = Device Code

YWZ = Date Code and Assembly Code

Absolute Maximum Ratings[1]

(T_A = 25°C unless otherwise noted)

Symbol	Description	Value	Units
VDD48I, VDD48O	High Voltage Pins[2]	100	V
VDD5, RCURR, RCLASS, LVMODE, FB, COMP, CSS, CS, NDRV, VBN, FSEL, ATDET	Low Voltage Pins	6	V
T_S	Storage Temperature	165	°C
T_J	Junction Operating Temperature	-40 to 150	°C

ESD Ratings

Symbol	Description	Value	Units
V_{ESD_HBM}	JEDEC-JS-001 Human Body Model (HBM)[3]	2	kV
V_{ESD_CD}	IEC 61000-4-2 Contact Discharge[4]	8	kV
V_{ESD_AGD}	IEC 61000-4-2 Air-Gap Discharge[4]	15	kV

Thermal Capabilities[5]

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance – Junction to Ambient	28	°C/W
P_D	Maximum Power Dissipation	4.4	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-35.7	mW/°C

Ordering Information

Part Number	Marking[6]	Operating Temperature	Package
KTA1137AEUAB-TR	OGYWZ	-40°C to +85°C	QFN55-20

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.[7]	Max.	Unit
$V_{IN\text{-}AF\ (Type\ 1\ PD)}$	Input Power Supply	37	48	57	V
$V_{IN\text{-}AT\ (Type\ 2\ PD)}$		42.5	48	57	V
$V_{IN\text{-}LP}$	Local Power Mode (VDD48O and GND)[8]	9.5		57	V
T_A	Ambient Operating Temperature Range	-40	-	+85	°C
T_{J_MAX}	Recommended Maximum Junction Operating Temperature			140	°C

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. Steady state or transient conditions like system start-up and other noise conditions. Device must not be exposed to sustained over-voltage condition at this level. See section on Rectification and Protection for further details on Integrated Surge Protection.
3. Human Body Model and Charged Device Model ESD limits are specified at the chip level.
4. Air Discharge, and Contact Discharge are specified at the system level.
5. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
6. “OG” is the device code, “YWZ” is the date code and assembly code.
7. Typical specification, not 100% tested. Performance guaranteed by design and/or other correlation methods.
8. Power transformer must be capable of handling the full voltage range.

Electrical Characteristics[9]

Unless otherwise noted, specifications are for T_A = -40°C to +85°C. Typical specifications are for T_A = +25°C and V_{IN} = 48V (at RJ45 Input). Typical specifications not 100% tested.

Symbol	Description	Conditions	Min	Typ	Max	Units
PD (all PD voltage limits specified at the RJ45 Interface)						
I_{INRUSH_AF}	Inrush Current Limit (AF) – Type 1 PD	For VDD48O ≤ 16V during startup, C_{IN} = 10µF	50	160	240	mA
I_{INRUSH_AT}	Inrush Current Limit (AT) – Type 2 PD		210	320	400	mA
I_{IN_AF}	Operating Current – Type 1	RCURR = GND; device configured for 13W operation			350	mA
I_{IN_AT}	Operating Current – Type 2	RCURR = left open; device configured for 30W operation			730	mA
I_{LIM-AF}	PoE Current Limit – Type 1	RCURR = GND; device configured for 13W operation	350	500	700	mA
I_{LIM-AT}	PoE Current Limit – Type 2	RCURR = left open; device configured for 30W operation	730	1100	1380	mA
R_{DS-ON}	Hot-Swap FET On Resistance	I_{IN} = 350mA		0.6	0.95	Ω
V_{DET_MIN}	Min Detection Signature voltage				2.7	V
V_{DET_MAX}	Max Detection Signature voltage		10.1	12.5	14.5	V
V_{CL_LOW}	Classification Lower Threshold	During Classification, the KTA1137A sinks current as defined in Table 2.	11.0	12.5	14.5	V
V_{CL_HIGH}	Classification Upper Threshold		20.5	22.0	25	V
V_{MARK_MIN}	Min Mark Event Voltage				6.9	V
V_{MARK_MAX}	Max Mark Event Voltage		10.0	12.5	13.0	V
I_{MARK}	Mark Event Current	When the input voltage is less than the minimum voltage mark threshold (V_{MARK_TH}) (IEEE® 802.3at-2009 defined) during the Classification signature, a Type 2 PD must draw Mark Event current.	0.25		4.00	mA
V_{CLMK_HYS}	Classification-Mark Hysteresis			1.5		V
V_{CL_RST}	Classification Reset Voltage		2.81		6.90	V
V_{ATDET_OH}	ATDET Output High	I_{ATDET} < 2mA output	4.5	4.7	5	V
V_{ATDET_OL}	ATDET Output Low	I_{ATDET} = 2mA		20	100	mV
$V_{IN\_UVLO\_R}$	Input UVLO Threshold	V_{IN} Rising	37	38	42	V
$V_{IN\_UVLO\_F}$		V_{IN} Falling	30	32	34	V
VDD5/VBN Internal Regulator						
$V_{VDD5/BN}$	Output Voltage	$C_{VDD5/VBN}$ = 0.5µF		4.7		V

9. KTA1137A is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

Electrical Characteristics[9]

Unless otherwise noted, specifications are for T_A = -40°C to +85°C. Typical specifications are for T_A = +25°C and V_{IN} = 48V (at RJ45 Input). Typical specifications not 100% tested.

Symbol	Description	Conditions		Min	Typ	Max	Units
DC-DC Controller							
F_{OSC}	Switching Frequency	R_{FSEL} = 178kΩ	All resistors ±1% Tolerance		105		kHz
		R_{FSEL} = 100kΩ			185		
		R_{FSEL} = 53.6kΩ			345		
		R_{FSEL} = 36.8kΩ			445		
$F_{OSC\_\Delta T}$	Oscillator Temperature Coefficient	R_{FSEL} = 100 kΩ			0.12		%/°C
R_{NDRV}	NDRV Drive Resistance				1.2		Ω
V_{NDRV_OH}	NDRV Voltage Output High				4.7		V
D_{NDRV_MAX}	Maximum Duty Cycle	R_{FSEL} = 53.6kΩ ±1% (350kHz)			85		%
D_{NDRV_MIN}	Minimum Duty Cycle				6	10	%
V_{EA_REF}	Error Amplifier Reference Voltage	Compared to input of the FB pin		1.41	1.51	1.61	V
V_{CST}	Peak Current Sense Threshold Voltage at CS	$I_{PEAK} = V_{PK}/R_{SENSE}$		500	600	700	mV
t_{SS}	Soft Start Ramp Time	Conditions: CSS = 100nF			15		ms
I_{C_SOURCE}	Comparator Source Current	FB = 0V, COMP = 0V			60		µA
I_{C_SINK}	Comparator Sink Current	FB = 5V, COMP = 5V			40		µA
G_{ea}	Error Amplifier Transconductance				120		µS
R_{ea}	Error Amplifier Output Resistance				20		MΩ
F_{ea}	Error Amplifier Crossover Frequency				16		MHz
I_{FB_LEAK}	FB Leakage (source or sink)				1		µA
Local Power Mode							
I_{IL}	LVMODE Threshold LOW					15	µA
I_{IH}	LVMODE Threshold HIGH			60			µA
Thermal Protection							
T_{J_TS}	Thermal Shutdown Temperature				160		°C
T_{J_HYS}	Thermal Shutdown Hysteresis				30		°C

Typical Characteristics

V_{IN} = 48V, T_A = 25°C unless otherwise specified.

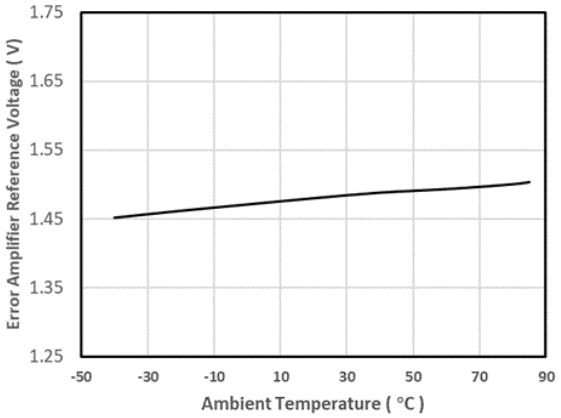


Figure 1. Reference Voltage vs. Temperature

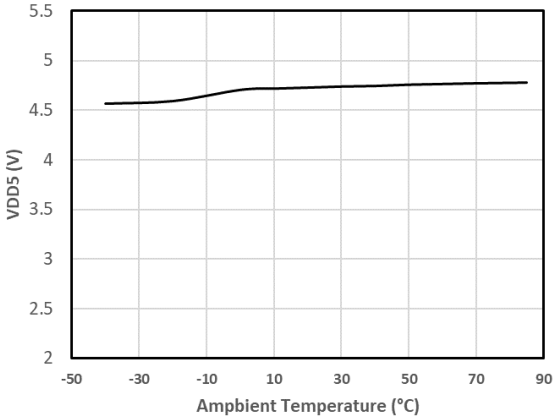


Figure 2. VDD5 vs. Temperature

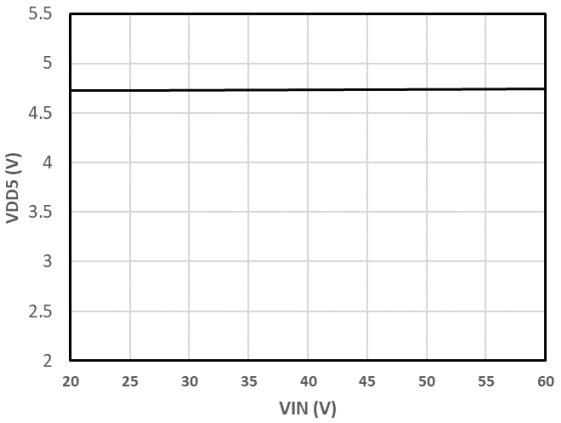


Figure 3. VDD5 vs. VIN

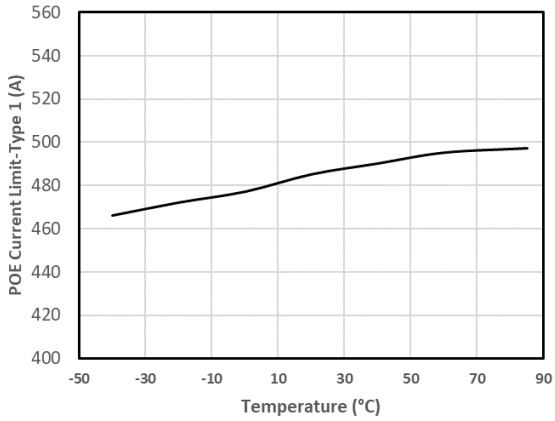


Figure 4. POE Current Limit - Type 1 vs. Temperature

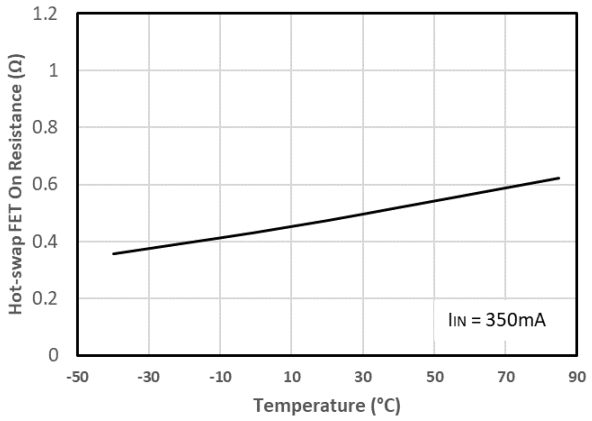


Figure 5. Hot-swap FET On Resistance vs. Temperature

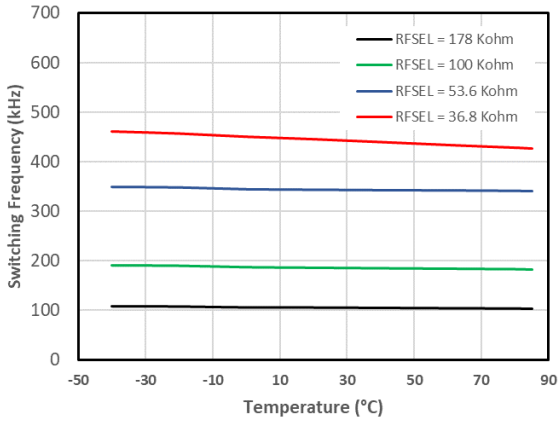


Figure 6. Switching Frequency vs. Temperature

Typical Characteristics (continued)

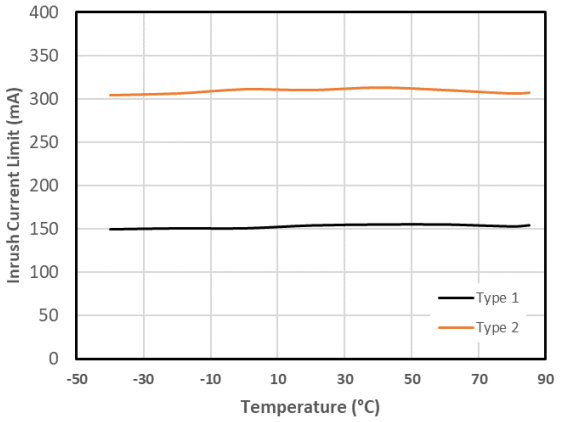


Figure 7. Inrush Current Limit vs. Temperature

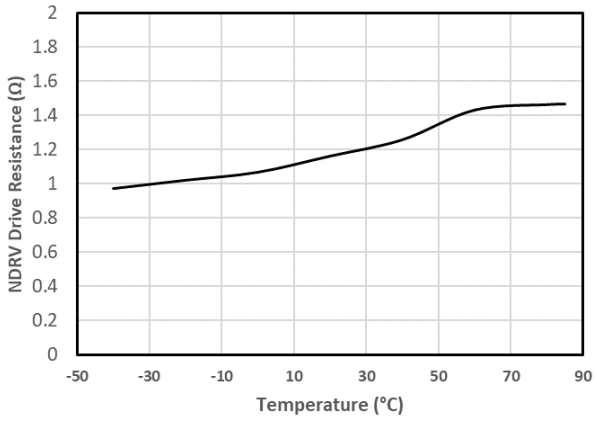


Figure 8. NDRV Drive Resistance vs. Temperature

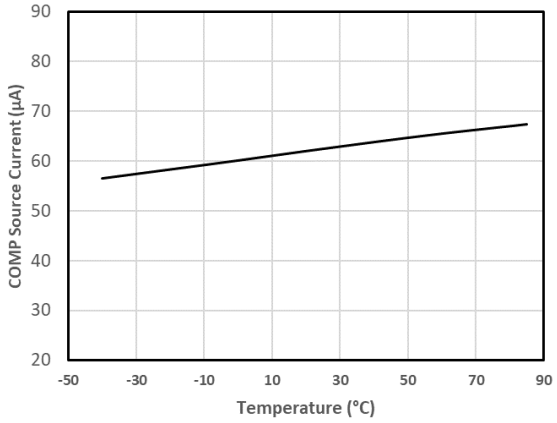


Figure 9. COMP Source Current vs. Temperature

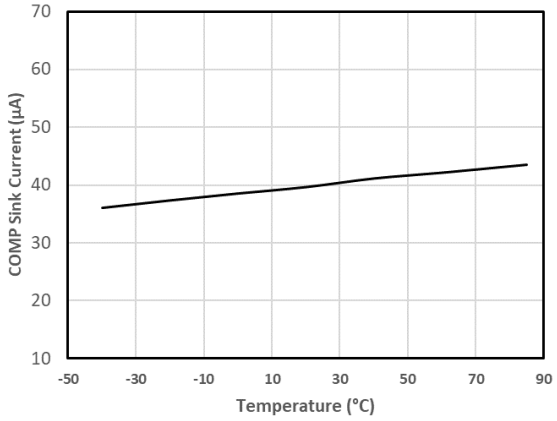


Figure 10. COMP Sink Current vs. Temperature

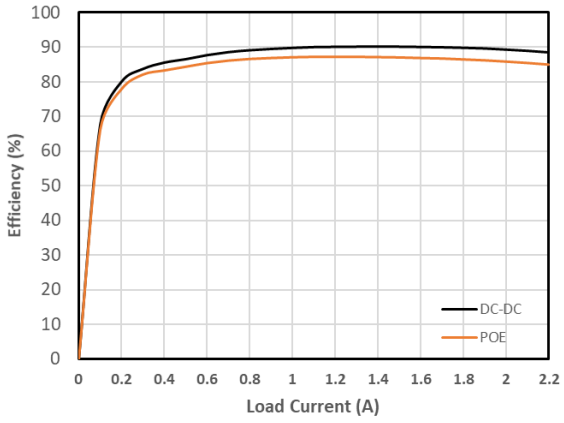


Figure 11. Efficiency vs. Load Current (VOUT = 12 V)

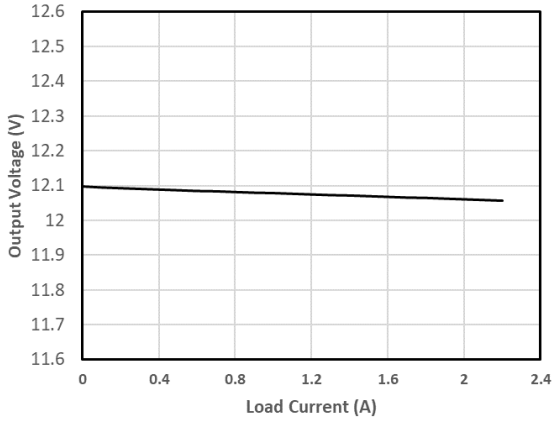


Figure 12. Output Voltage Load Regulation

Typical Characteristics (continued)

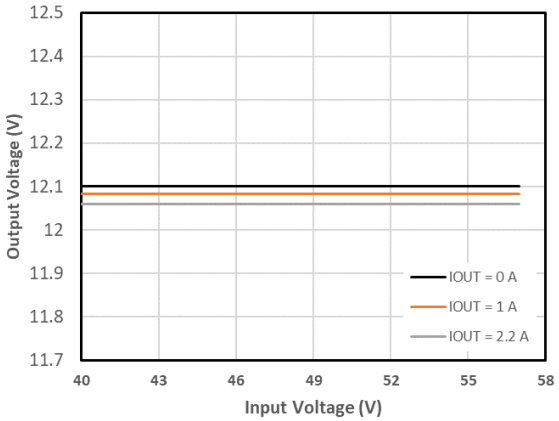


Figure 13. Output Voltage Line Regulation

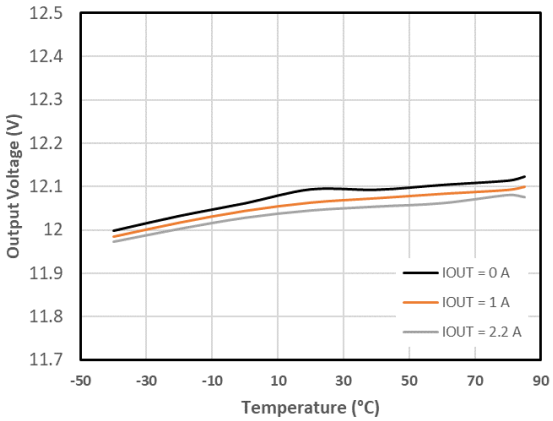


Figure 14. Output Voltage vs. Temperature

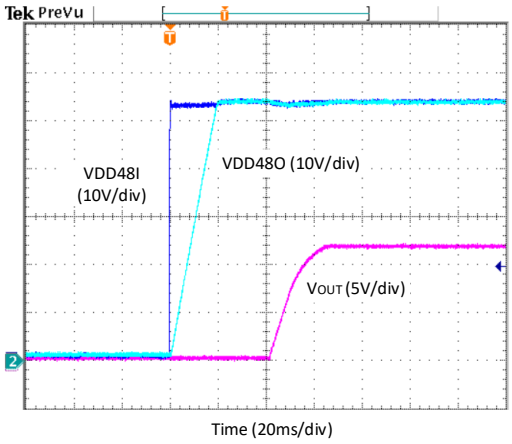


Figure 15. Example Waveforms of VDD48I / VDD48O / VOUT

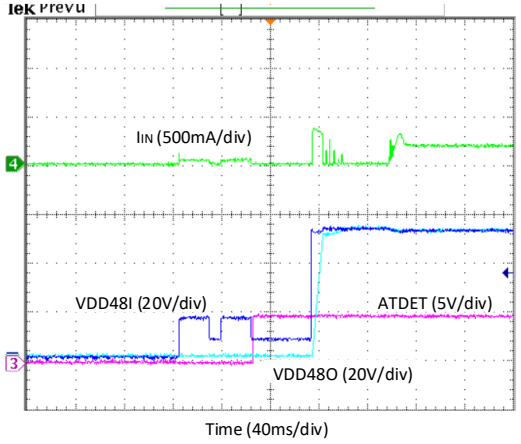


Figure 16. PI Input Voltage / Input Current and ATDET

Functional Block Diagram

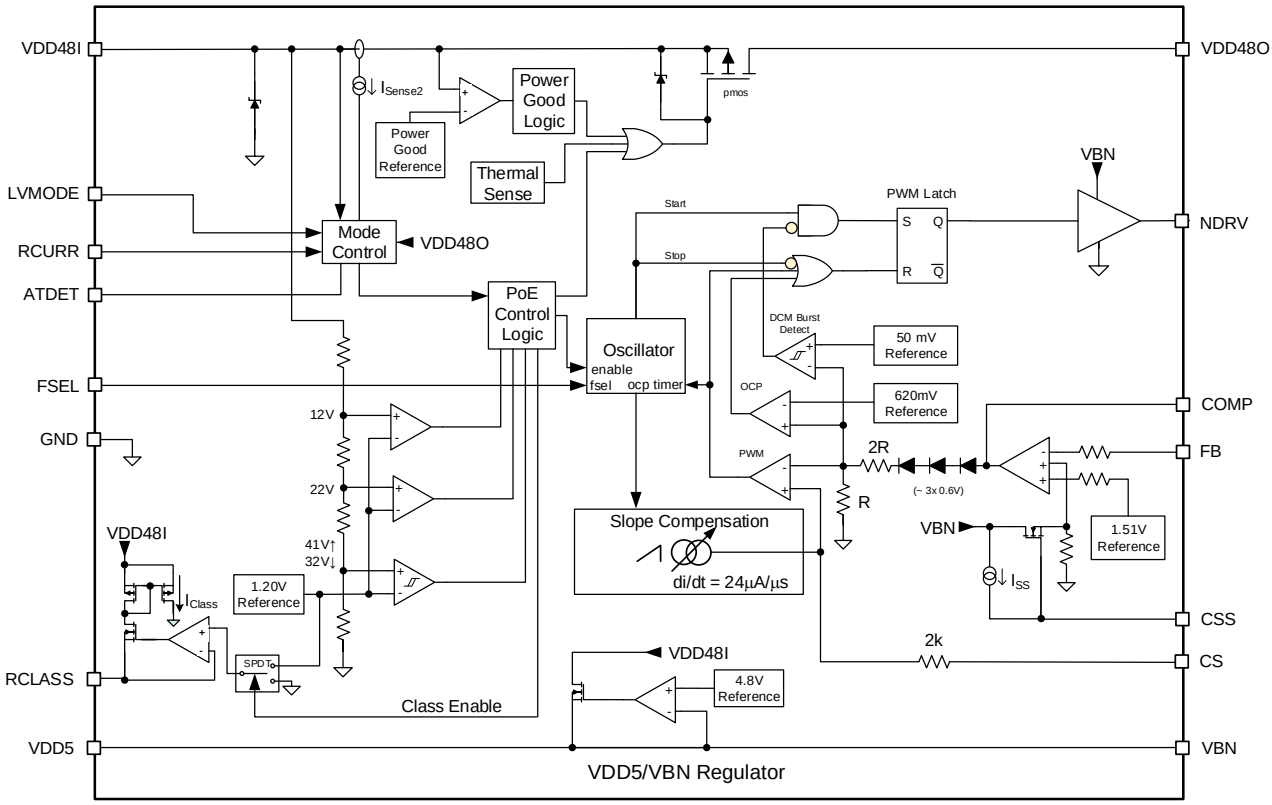


Figure 17. Block Diagram

Functional Description

Overview of PoE

Power over Ethernet (PoE) offers an economical alternative for powering end network appliances, such as IP telephones, wireless access points, security and web cameras, and other powered devices (PDs). PoE standards IEEE® Std. 802.3af and 802.3at are intended to unify the delivery method of usable power over Ethernet cables to remotely powered client devices. These standards define a method for detecting and querying PDs and then supplying a range of current levels based on the power class the device belongs to. By employing this method, designers can create systems that predict and minimize power usage, allowing the maximum number of devices to be supported on a powered Ethernet network.

The power source that provides current through the Ethernet cables to remote devices is referred to as the Power Sourcing Equipment (PSE). The powered device (PD) on the other end of the Ethernet cable negotiates for and receives the agreed-upon power. IEEE® Std. 802.3af limits PSE power delivery to <13W at the PD input (Type 1 PD). IEEE® 802.3at allows for >13W power levels (Type 2 PD).

The PSE uses the following 802.3af sequence to detect a connected PD, determine how much power it requires and then initiate supply current to the device:

- **Reset** — Power is withdrawn from the PD if the applied voltage falls below a specified level.
- **Signature Detection** — The PSE detects and evaluates whether the PD is a valid PoE device.
- **Classification** — The PSE reads the power requirement of the PD. The Classification level identifies how much power the PD will require from the Ethernet line. This permits optimum use of the total power available

from the PSE. Classification is considered optional by IEEE® standard 802.3af-2005 but IEEE® standard 802.3at-2009 requires Type 2 PSE to classify the PD for mutual identification.

- **On** — Operational state, during which the PSE provides the allocated power level to the PD.

This sequence occurs as a progressively rising voltage level from the PSE. It is designed to prevent high voltages from being present on an Ethernet line that does not have a valid PD attached (for user and non-PoE device safety).

To design PoE systems according to IEEE® standards, the following constraints apply:

Table 1. PoE Requirements

Requirement	Value
Maximum Type 1 PD input power	12.95W
Maximum Type 2 PD input power	25.5W
Output voltage from Type 1 PSE	44-57V
Output voltage from Type 2 PSE	50-57V
Minimum operating current limit, Type 1 @ PSE min output voltage	350mA
Minimum operating current limit, Type 2 @ PSE min output voltage	600mA
Line resistance, Type 2 operation	12.5Ω
Input voltage at Type 1 PD interface	37V-57V
Input voltage at Type 2 PD interface	42.5V-57V

KTA1137A Design

To help designers meet these requirements, the KTA1137A is a fully integrated PoE PD controller for Type1 and Type2 PD implementations. The KTA1137A meets all system requirements for the IEEE® 802.3 standard for Ethernet and all power management requirements for IEEE® standard 802.3at-2009.

The KTA1137A acts as an interface to the PSE, performing all detection, classification, and inrush current limiting control necessary for compliance with the PoE standards. An internal MOSFET and control circuit limits the inrush and steady-state current drawn from the Ethernet line. External diode bridges protect against polarity reversal, to provide alternative A and B detection.

The KTA1137A also passes the 8kV Contact Discharge and 15kV Air Discharge requirements, tested per IEC 61000-4-2. EMI compliance of KTA1137A-based designs has been verified for CISP22 and FCC Class-B radiated and conducted emissions.

Power Feed Alternatives for 10/100/1000 Ethernet Systems

The Power Sourcing Equipment (PSE) supplies power to a single PD per node. A PSE located in the Data Terminal Equipment or Repeater is called an endpoint PSE, while a PSE located between MDIs is called a Mid-span PSE. Figure 18 illustrates the power feed options allowed in the 802.3at-2009 standard for 10/100/1000 Ethernet systems.

In Alternative A, a PSE powers the end station by feeding current along the twisted pair cable used for the 10/100/1000 Ethernet signal via center taps on the Ethernet transformers. On the line side of the transformers for the PD, power is delivered through pins 1 and 2 and returned through pins 3 and 6.

In Alternative B, a PSE powers the end station by feeding power through pins 4, 5, 7 and 8. In a 10/100/1000 system, this is done through the center taps of the Ethernet transformer. In a 10/100 system, power is applied directly to the spare cable pairs without using transformers.

The IEEE® Std. 802.3at-2009 standard is intended to be fully compliant with all existing non-powered Ethernet systems. As a result, the PSE is required to detect via a well-defined procedure whether or not the connected device is PD compliant and classify (optional in legacy 802.3af-2005 applications) the needed power prior to supplying it to the device. Maximum allowed voltage is 57V to stay within SELV (Safety Extra Low Voltage) limits.

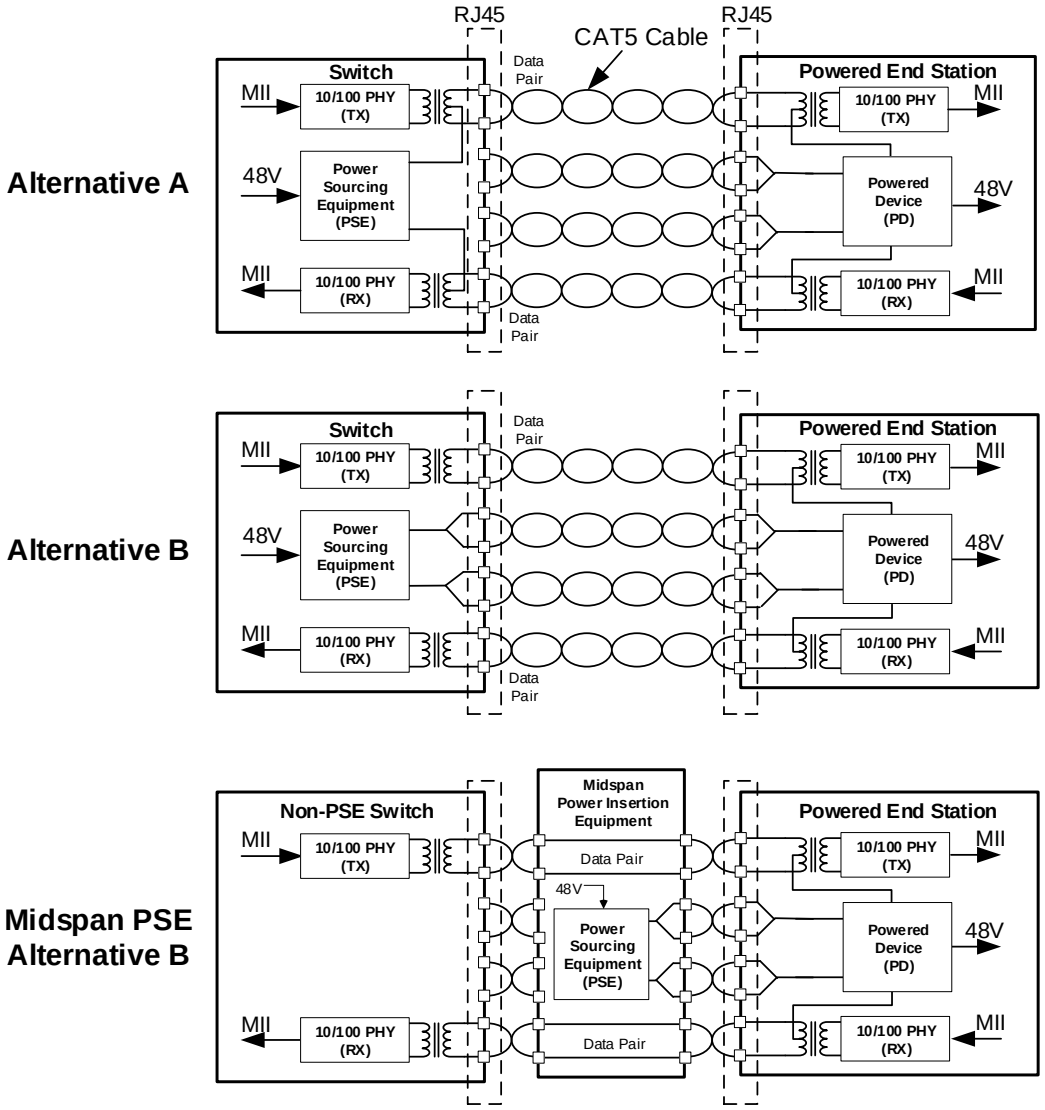


Figure 18. IEEE® Std. 802.3at-2009 Power Feeding Schemes for 10/100 Systems

KTA1137A Overview

The KTA1137A is a fully integrated PD that provides the functionality required for Power-over-Ethernet (PoE) applications. The optimized architecture reduces external component cost in a small footprint while delivering high performance.

Rectification and Protection

To protect against polarity reversal, an external diode bridge is required. In conjunction with the external diode bridge, the KTA1137A provides over-voltage and transient protection on the line side of the Hot-Swap FET.

The KTA1137A is implemented in a robust 100V process technology. By integrating robust input protection circuitry, Kinetic has produced a solution that provides much faster response to surge events. The design also limits stray surge current from passing through sensitive circuits, such as the Ethernet PHY device and enables low-impedance safe discharge paths directly to earth ground. The protection circuit has been carefully designed to ensure that during these surge events, where currents can reach as high as 30A, voltages do not exceed critical breakdown and spark gap limits, protecting the PD from damage by the event. This enables system designers to achieve 15kV/8kV Air/Contact Discharge system ESD performance.

PD Controller

The KTA1137A PD Control Interface is designed to provide full PD functionality for IEEE® 802.3af and 802.3at compliant systems, with programmable support for standard PD control functions.

The PD Controller provides the following major functions:

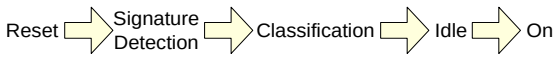
- A resistance/capacitance connection path for the detection signature.
- Classification current for power classification.
- Full 30Watt PD supply capability
- Power management and thermal protection override, including UVLO (Under Voltage Lock Out).
- ATDET signal output when connected to a Type 2 PSE that can deliver more than 13Watts.
- 2-Event Physical Layer classification.

Modes of Operation

The KTA1137A has five operating modes:

1. **Reset** — all blocks are disabled.
2. **Detection** — the external PD detection signature resistance / capacitance components are applied across the input.
3. **Classification** — PD indicates power requirements to the PSE via a Single-Event Classification for 802.3af or a 2-Event Physical Layer Classification for 802.3at.
4. **Idle** — this state is entered after Classification and remains until full-power input voltage is applied.
5. **On** — The PD is enabled and supplies power to the DC-DC controller and the local application circuitry.

As the supply voltage from the PSE increases from 0V, the KTA1137A transitions through the modes of operation in this sequence:



If no PSE or local power supply is present, line voltage will be zero, which will hold the KTA1137A in the Reset state. The KTA1137A does not affect the Ethernet link function.

Reset

When the voltage supplied to the KTA1137A drops below the minimum valid detection voltage (i.e. <2.7V), the chip will enter the Reset state. While in Reset, the power supply to the PD is disconnected, the KTA1137A consumes very little power and the device reverts to the pre-detection status.

Detection Mode

During the detection sequence, the PSE applies a voltage to the PD to read its detection signature. The reading of the signature determines if a PD is present.

During detection, the PSE applies two sequential voltages, 1V or more apart, within the detection voltage range of 2.7V to 10.1V. It extracts a detection signature resistance value from the incremental I-V slope. Valid I-V slope resistance values are between 23.75kΩ and 26.25kΩ.

With the KTA1137A, detection signature resistance is generated by an external resistor connected between VDD48I and GND. Typically this is a 25.5kΩ, 1% resistor. With this value of RSIGNATURE, the PSE normally detects a total effective signature resistance of approximately 25kΩ, which is centered within the 802.3af/at specification range of 23.75kΩ to 26.25kΩ.

Valid PD detection also requires a valid detection signature capacitance of 0.05µ to 0.12µF at 2.7 to 10.1V, and 1.9V maximum offset voltage, per the IEEE® 802.3af/at standard, measured at the PD input connector. KTA1137A detection signature capacitance is generated by an external 68nF capacitor connected between VDD48I and GND. The offset voltage is mainly provided by the external diode bridge voltage drop.

Classification Mode

Each class represents a power allocation range for a PD to assist the PSE in managing power distribution. IEEE® Std. 802.3at defines classes of power levels for PDs, listed in Table 2. The KTA1137A supports 2-Event Physical Layer classification, per IEEE® Std. 802.3at, as shown in Figure 16 and Figure 20.

The KTA1137A identifies the PSE as either Type 1 or Type 2. If the 2-Event method is detected by the PD controller during the classification stage, it asserts the ATDET pin High, indicating connection to a Type 2 PSE. If the PD controller detects only single-event classification, it identifies the PSE to be Type 1 and the ATDET pin is asserted low.

In real applications, noise or transient ringing on the line during classification phase can lead to false 2-event classification or Type 2 PSE detection. To prevent such false positives, the KTA1137A integrates a proprietary digital filter to filter out noise events as long as 100uS during the classification phase, ensuring a very reliable AT Detection.

If a PSE is Type 1, to classify the KTA1137A, the Type 1 PSE presents a voltage between 14.5V and 20.5V to the PD and determines its class by measuring the resulting PD load current.

If a PSE is Type 2, in order to classify the KTA1137A as the Type 2 PD, KTA1137A has to be set as Class 4 (classification setting shown in Table 2), so that KTA1137A returns a Class 4 signature.

The KTA1137A allows the user to program the classification current via an external resistor connected to the RCLASS pin. Current, power levels and programming resistor values for each class are shown in Table 2. Note that for Class 0, RCLASS pin needs to be Pulled Up to VDD5 pin. This can be a direct short to VDD5 or using a resistor up to 100kΩ.

Use the following equation to determine the typical classification current:

$$I_{Class}[mA] = 2.0 + \frac{2360}{R_{Class}[k\Omega]} \qquad (1)$$

Tolerance = Maximum of ±1.8mA or ±9%

R_{CLASS} > 63.4kΩ

Once the classification process is done, the PD removes the classification current to conserve power.

Note: During the classification of a Type 2 PD, the PSE outputs a sequence of voltage signals (Class 1, Mark 1, Class 2, Mark 2, and Class 3) within the specific timing requirement. The PD has to respond within the limit range of voltage/current/impedance for each event according to section 33.3.5 PD Classifications of 802.3at standard.

Table 2. Classification Settings

Class	Power (W)	I_{CLASS} (mA)	R_{CLASS} (kΩ)
0	0.44-12.95	0-4 mA	Pull-up (0-100kΩ) to VDD5 pin
1	0.44-3.84	9-12 mA	280kΩ, 1%
2	3.84-6.49	17-20 mA	143kΩ, 1%
3	6.49-12.95	26-30 mA	90.9kΩ, 1%
4	12.96-25.5	36-44 mA	63.4kΩ, 1%

Idle Mode

After the classification process, the PD enters Idle mode while it waits for On-state power delivery from the PSE. PD Current usage is limited to monitoring circuitry to detect the On-state voltage threshold.

On State

In the On state, the KTA1137A is supplying power across the Ethernet line(s) to the PD. At a voltage at or below 42V, the PD turns on and full power is available via the KTA1137A DC-DC Controller.

Local Power Mode (LVMODE)

The LVMODE pin can be used in applications where the PD appliance is designed to draw power from either the Ethernet cable or an external DC local power adapter. The LVMODE pin is a current-mode input pin, with low and high thresholds as defined in the electrical characteristics for the PD. The LVMODE is asserted when the input current exceeds the IIH threshold, and is de-asserted when the input current is below the IIL threshold. If LVMODE operation is not desired, the LVMODE pin should be connected to GND.

Figure 19 below shows a simplified internal implementation and external application circuit required to use the LVMODE feature. When power is applied at the local adapter input, the KTA1137A enters Local Voltage Mode. This opens the internal Hot-Swap FET switch while the DC-DC converter is in operation.

In this configuration, local power always takes priority, even in presence of PoE power, irrespective of their relative voltages. If local power is removed, the device will exit Local Voltage Mode operation and PoE power will be used, if available.

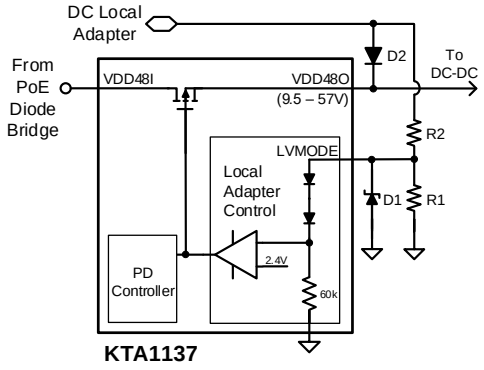


Figure 19. LVMODE Implementation

Local power is inserted at the VDD48O node through an external diode (D2). Use of a low reverse-leakage diode is recommended (<350µA, at worst case temperature). This ensures that when there is no local power, PoE voltage at the VDD48O node will not falsely pull up the LVMODE pin due to high reverse leakage through the diode. Please see Table 3 for part number information.

An appropriate ratio of R2 and R1 resistors should be used to ensure proper operation across all supply voltages. Table 3 lists appropriate choices of R2 and R1 resistors to work with a variety of popular local adapter DC voltages. Though a common value of R2 and R1 can be used across the whole range of local supply voltages from 9.5V to 57V, using different value pairs, per Table 3, will minimize power consumption. The maximum input voltage at the LVMODE pin should not exceed 6V, so a Zener diode (D1) is recommended to limit transient voltage excursions at the pin.

Since the input current at the LVMODE pin defines its state, it is not recommended to drive other circuits or components directly from the LVMODE node (such as an LED) that might draw current. LEDs or current-absorbing components may be driven directly from the Local Supply pin.

The KTA1137A internal DC-DC controller is designed to operate with input voltages of 9.5V-57V, to allow applications to take advantage of the LVMODE feature. Besides configuring the device for operation from a local power source, the external power transformer must also be designed to ensure proper operation across the complete input range.

Table 3. LVMODE Configuration

Local Voltage Range	Recommended Local Adapters	R2	R1
9.5V-57V	12V, 18V	2.74kΩ	4.02kΩ
20V-57V	24V, 30V	11.3kΩ	4.02kΩ
32.4V-57V	36V, 48V	20kΩ	4.02kΩ

Diode D1: 5.6V Zener, BZT56V

Diode D2: S3B (100V/3A, worst-case reverse leakage <250µA), use of a low reverse-leakage diode with worst-case reverse leakage under high temperature <350µA is recommended.

PD Controller Power and Thermal Protection

The KTA1137A provides the following PD controller power and thermal protection:

- Under Voltage Lock Out (UVLO)
- Inrush Current Limit with integrated current sense
- Thermal Limit / Protection

Under Voltage Lock Out (UVLO)

The KTA1137A contains line Under-Voltage Lock Out (UVLO) circuitry to determine when to power on the PD. If the PSE supply voltage at PD PI is equal or greater than UVLO VIN_RISING, the KTA1137A PD will power on and run; if the PSE supply voltage at PD PI drops below UVLO VIN_FALLING, the KTA1137A PD will power off. The PD circuit controls power flow to the DC-DC controller, to protect the PD from erratic operation or damage.

Inrush Current Limit / Current Sense

Inrush limiting maintains the cable voltage above the turn-off threshold as the input capacitor charges. This also prevents the PSE from going into current limit mode. The Current Limit/Current Sense circuitry also minimizes the PD on-chip temperature peaks by limiting both inrush and operating current.

Current is monitored with an integrated sense circuit that regulates the gate voltage on an integrated low-leakage power MOSFET. The power MOSFET can also be shut off completely by either the PD Controller, the Thermal Limit Protection circuitry or the insertion of a local power adapter that causes the LVMODE pin to be pulled high (via a resistor divider).

During the PD startup sequence, VDS across the Hot-Swap FET is momentarily high as the VDD48O output capacitance is charged up, as illustrated in Figure 20 below. During this state, the Hot-Swap FET experiences a high instantaneous power drop and heating. Therefore, it is recommended that during this startup sequence, the incoming current should only be utilized for the charging of the VDD48O node, to minimize the startup time and associated power drop across the FET. The primary PWM controller is designed to accommodate for VDD48O startup before drawing power from the line. However, if the application requires direct use of the VDD48O node for other functions, the startup of those circuits should be delayed until the VDD48O node has reached its full voltage level.

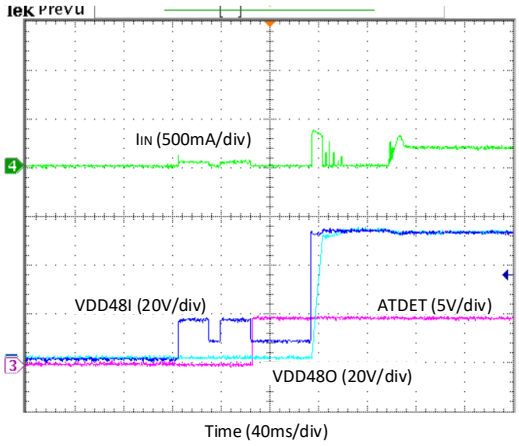


Figure 20. PI Input Voltage and Current / ATDET

Thermal Limit / Protection

The KTA1137A provides thermal protection for itself by monitoring die temperature and reducing maximum current or disconnecting power as needed to prevent its pre-set thermal limits from being exceeded. Two-stage thermal current limiting is implemented, which reduces the operating current limit by 50% when the die temperature reaches 145˚C, and disables the power MOSFET switch above 165˚C. Normal current limits in both cases are re-applied when the die temperature returns below 125˚C.

PoE Power-On Startup Waveform

Figure 21 represents the power-on sequence for PoE operation. The waveform reflects typical voltages present at the PD during signature, classification and power-on.

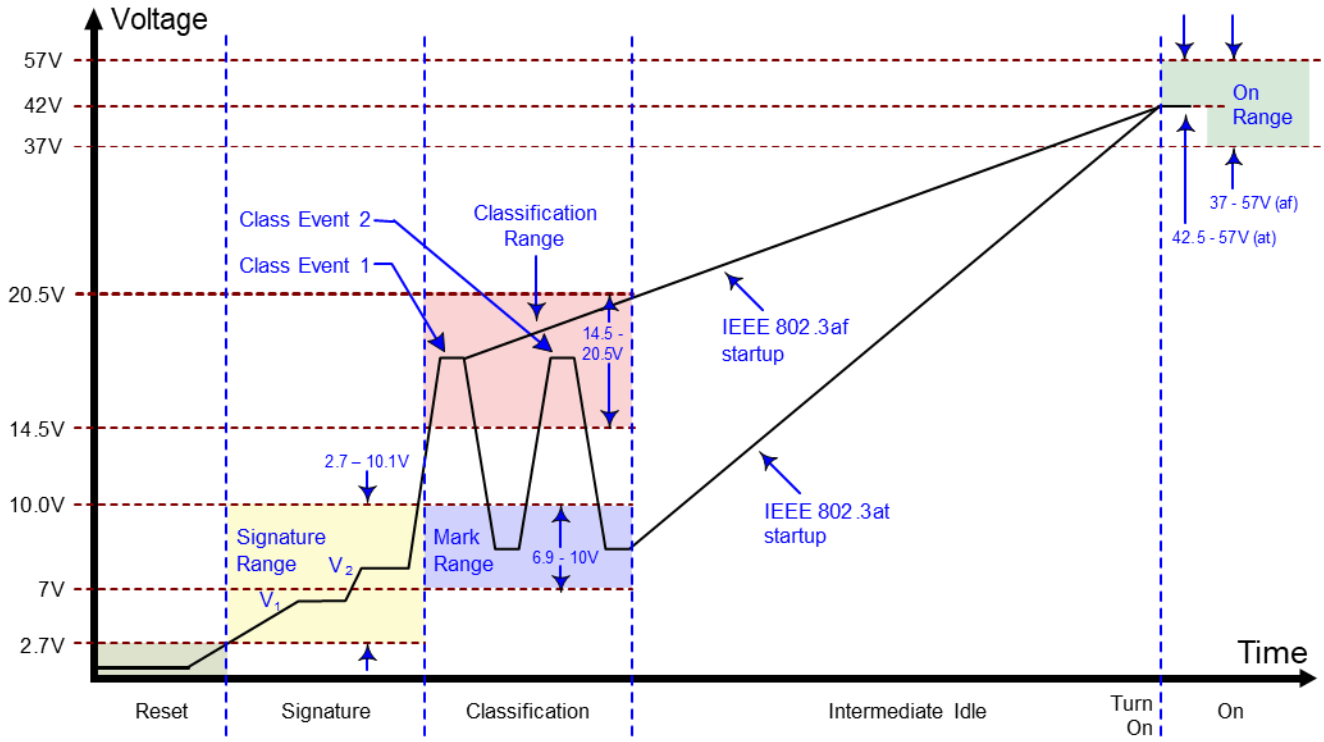


Figure 21. 802.3at Typical Power-On Waveform

1. Voltages V1 and V2 are applied by the PSE to extract a signature value.
2. The PSE takes current/impedance readings during Class/Mark Events to determine the class of the PD. At this time, the PD presents a load current determined by the resistance connected to the RCLASS pin.
3. After the PSE measures the PD load current, if it is a high-power PSE, it presents a mark voltage (6.9-10V), followed by a second classification voltage. The PD responds by presenting a load current as determined by the resistor on the RCLASS pin. After the PSE measures the PD load current the second time and determines that is can deliver the requested power, it moves into the On state by raising the voltage to approximately 42V.

ATDET Pin

The ATDET output pin provides an indicator when 2-event classification is detected by being linked to a Type 2 PSE, or through the use of a local power supply that uses the LVMODE feature. This indicates system has more than 13W of available power. This pin can be used by the PD system controller to self-configure the application device based on available power.

If there is no local power present, ATDET will stay low during PD Reset, Detection and Classification phases. The ATDET pin will be set high once the PD recognizes the completion of the 2-Event Physical Layer Classification, as initiated by a Type 2 PSE. The pin will remain high and will only be reset low by the occurrence of a Reset or a power-down event. ATDET pin remains low if it identifies the PSE partner to be Type 1 during the Classification phase.

If LVMODE is asserted when supplying local power, the ATDET pin is forced high, irrespective of the PD mode. Please see Table 4 below for ATDET output definitions under various powering modes.

Table 4. ATDET Truth Table

ATDET Signal Status	PSE	
	Type 1	Type 2
LVMODE = Low	Low	High
LVMODE = High	High	High

DC-DC Controller

Overview

The DC-DC architecture is a current-mode controller configurable with external components to fly-back, forward or buck topologies. Both non-isolated and isolated topologies are supported.

As part of a full system-level solution to control EMI, Kinetic has focused significant attention on reducing switching noise in the integrated power converters through unique methods of shaping FET driver waveforms. Ground bounce is also reduced by minimizing dV/dt switching noise.

The integrated DC-DC controller operates from a switched input voltage (VDD48O) and includes a programmable soft start and current limiting. Once input power is applied and enable signals are asserted, the DC-DC controller starts up. The controller provides a gate control signal, NDRV, to the external switching MOSFET and uses an external resistor to sense primary current in the transformer. It also provides for an 80% maximum duty cycle, programmable PWM switching frequency and a true voltage-output error amplifier.

Programmable PWM Frequency

The FSEL pin allows the DC-DC converter switching frequency to be set externally. Placing a resistor between FSEL and GND sets the internal oscillator's frequency Table 5 identifies the resistor values for some commonly-used switching frequencies.

Table 5. PWM Switching Frequency Selection

Switching Frequency (kHz)	FSEL Resistor (kΩ, ± 1%)
105	178
185	100
345	53.6
445	36.8

Current-Limit/Current Sense

The DC/DC controller provides cycle-by-cycle current limit monitoring, via the CS input, to ensure that transformer current limits are not exceeded.

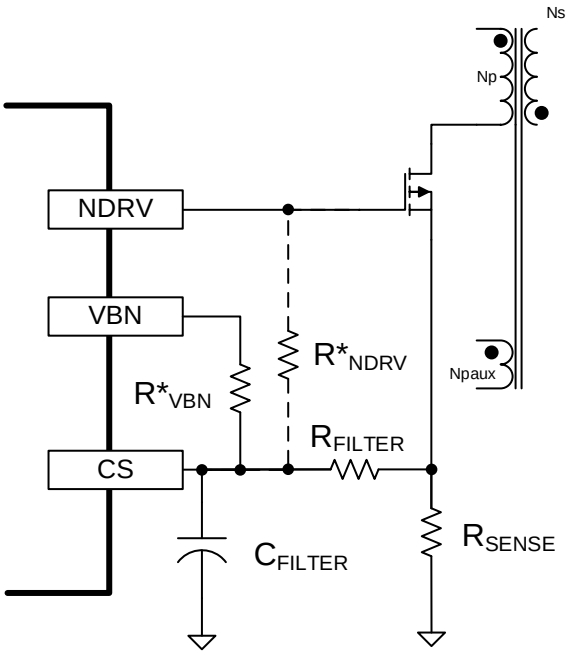
A short-circuit event is declared if the CS sensed current limit is triggered on 32 consecutive PWM clock cycles. Once a short-circuit event has been declared, the PWM will shut off for 512 cycles before a restart is attempted. This process will repeat indefinitely until the output short is removed.

Low Load Current Operation

The internal circuitry detects a low output power condition and puts the DC-DC Controller into a discontinuous operation mode (DCM burst). Burst mode operation occurs when the COMP pin voltage drops below ~ 1.00V.

In many applications it may be desirable to disable burst mode operation or reduce the load at which burst mode operation occurs. This can be accomplished by adding a DC offset to the current sense signal at the CS pin. Adding a pull-up resistor from either VBN or NDRV to CS provides the necessary offset voltage. Adding a minimum of 100mV of DC offset to CS will disable burst mode operation.

$$V_{CS(DC\ offset)} \approx VBN \cdot \frac{R_{FILTER}}{R_{VBN} + R_{FILTER}}$$



* R_{VBN} and R_{NDRV} are alternate methods to add DC offset. Select one.

Figure 22. Location of RNDRV or RVBN to Disable Burst Mode Operation

Burst mode should be disabled for synchronous rectified outputs. For diode rectified outputs, the load at which burst mode occurs may be reduced, but it is neither possible nor desirable to disable burst mode operation at very light or no-load conditions.

Compensation and Feedback

For isolated applications, loop compensation and output voltage feedback is generally provided by an opto-isolator circuit, and the Feedback pin (FB) is tied to ground. In these applications, the COMP pin is pulled up to approximately 4.8V by an internal current source. This pull-up can be the termination for an opto-isolator, or, an additional resistor can be used in parallel.

For non-isolated applications, a resistive divider network, connected directly to the FB pin, senses the output voltage. The internal error amplifier is connected to a 1.51V reference voltage and the control loop will servo the FB pin to this voltage. A capacitive/resistive network connected to the COMP pin provides loop compensation.

Soft-Start

A capacitor is required on the CSS pin and is used to provide a controlled application power supply startup.
Upon device power on, the capacitor on the CSS pin is slowly charged by the KTA1137A. In isolated designs this charging soft start voltage level limits the maximum voltage “seen” on the CS pin to:

$$V_{CS\_MAX} \approx V_{CSS} - 1$$

And since peak current detection is:

$$I_{PK} = V_{CS}/R_{CS}$$

the maximum Flyback output current ramps with VCS, providing a soft start. For example, a 12V output flyback design with a max duty cycle of 45% and a CSS cap of 330nF will have a soft start of ~8ms.

For non-isolated designs, the soft start time (TSS) in seconds for a given capacitor (CCSS) is defined by the formula:

$$Tss = \frac{1.5Css}{10\mu A}$$

For example, in a non-isolated design, a 100nF capacitor creates a soft start time of ~15ms.

DC-DC Converter Topologies

Isolated Topologies

The DC-DC controller can be configured in several different isolated topologies. The Flyback mode is chosen when a minimum number of external components is desired, or there is a large step-down and the output voltage is < 7V.

The Forward mode is chosen when lower switching noise is desired. Either of these isolated topologies can be designed for synchronous or non-synchronous operation, based on system requirements. A typical Isolated Synchronous Flyback design is shown in Figure 23.

Non-Isolated Topologies

The Buck mode is used in non-isolated applications. This application uses inductor for energy storage, instead of a transformer. See Figure 24.

Application Circuits

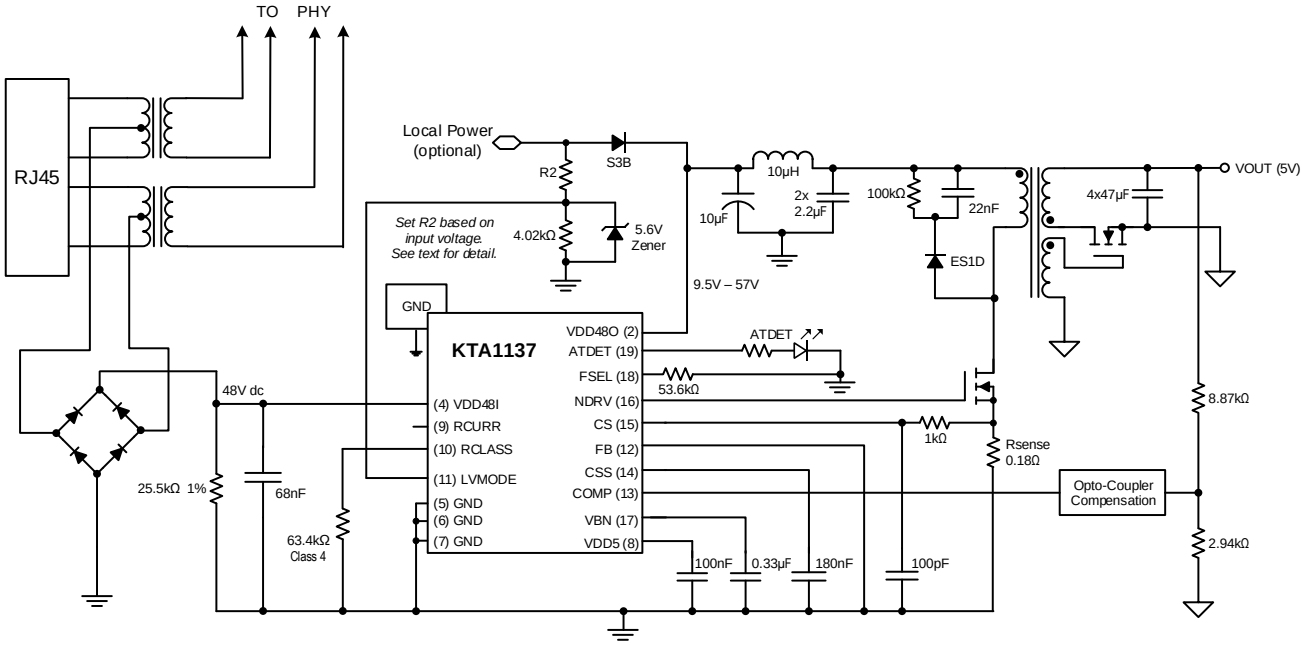


Figure 23. PoE PD Controller with a High-Efficiency Isolated Synchronous Flyback DC-DC Converter

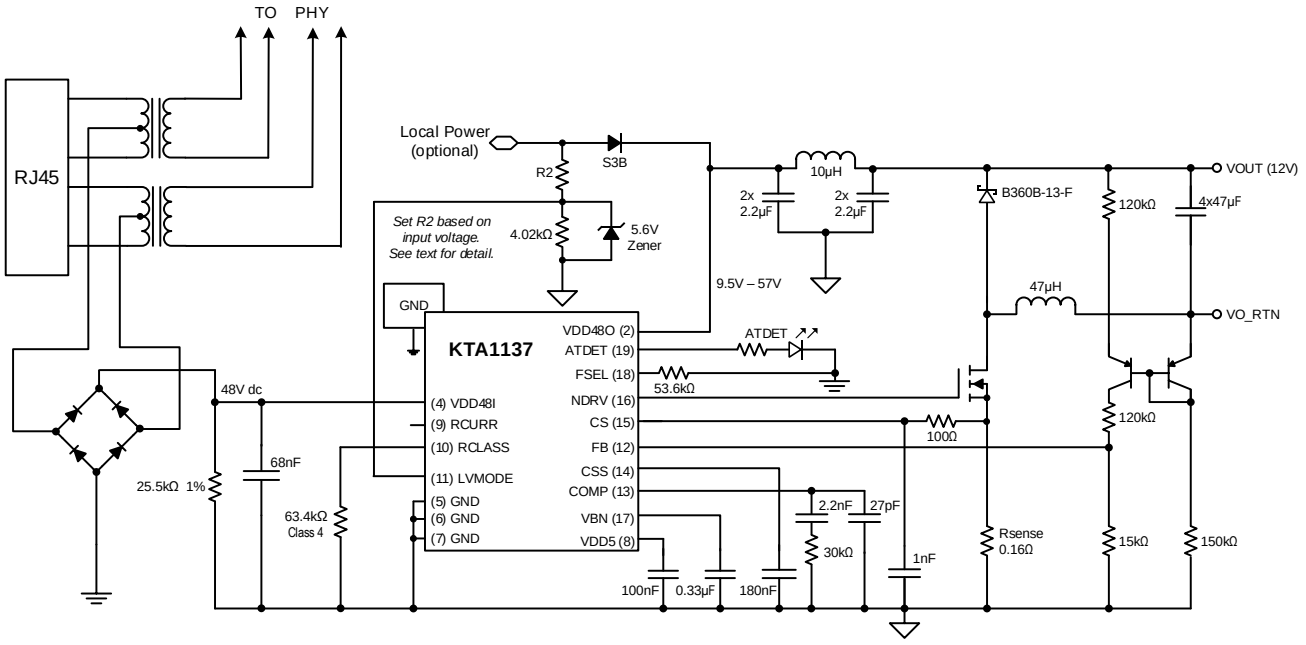


Figure 24. PoE PD Controller with a Non-Isolated BUCK DC-DC Converter

Note: This is a simplified conceptual schematic. Please refer to the reference design documentation for detailed design and component information. Full PoE implementation will require two input diode bridges. For simplicity, only one is shown here.

Thermal De-Rating and Board Layout Considerations

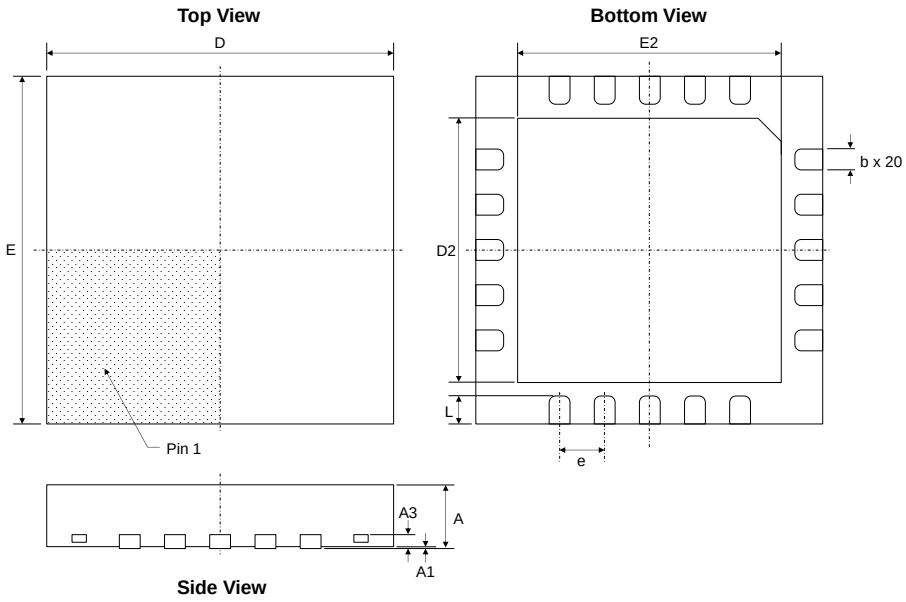
The KTA1137A is capable of operating to an industrial temperature range of 85°C in ambient air, without forced cooling. A thermal pad on the underside of the package dissipates the heat generated by the PD die.

In 30W applications, designers must consider thermal dissipation as an integral part of their system architecture and plan to remove heat via this pad.

If the PCB landing pattern is properly designed, the QFN package should exhibit a thermal resistance of ΘJA = 28°C/W. For adequate heat dissipation, the board layout must include a ground pad which provides both the ground connection and dissipates the heat energy produced in the chip. Thermal vias are used to draw heat away from the PD package and to transfer it to the backside of the system PCB.

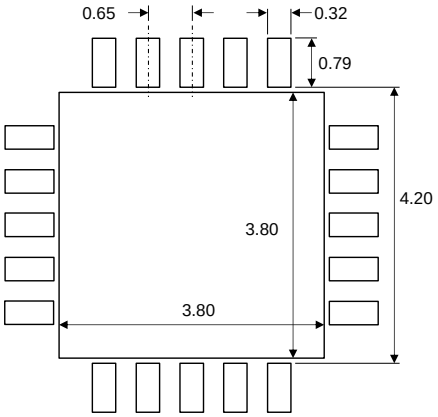
Packaging Information

TQFN55-20 (5.00mm x 5.00mm x 0.90mm)



Dimension	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.025	0.05
A3	0.203 REF		
b	0.25	0.30	0.35
D	4.85	5.00	5.15
D2	3.70	3.80	3.90
E	4.85	5.00	5.15
E2	3.70	3.80	3.90
L	0.35	0.40	0.45
e	0.650 BSC		

Recommended Footprint



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