Low Inductance Capacitors, KGL Series

Introduction

The signal integrity characteristics of a Power Delivery Network (PDN) are becoming critical aspects of board level and semiconductor package designs due to higher operating frequencies, larger power demands, and the ever shrinking lower and upper voltage limits around low operating voltages. These power system challenges are coming from mainstream designs with operating frequencies of 300MHz or greater, modest ICs with power demand of 15 watts or more, and operating voltages below 3 volts.

The classic PDN topology is comprised of a series of capacitor stages. Figure 1 is an example of this architecture with multiple capacitor stages.

An ideal capacitor can transfer all its stored energy to a load instantly. A real capacitor has parasitics that prevent instantaneous transfer of a capacitor's stored energy. The true nature of a capacitor can be modeled as an RLC equivalent circuit. For most simulation purposes, it is possible to model the characteristics of a real capacitor with one capacitor, one resistor, and one inductor. The RLC values in this model are commonly referred to as equivalent series capacitance (ESC), equivalent series resistance (ESR), and equivalent series inductance (ESL).

The ESL of a capacitor determines the speed of energy transfer to a load. The lower the ESL of a capacitor, the faster that energy can be transferred to a load. Historically, there has been a tradeoff between energy storage (capacitance) and inductance (speed of energy delivery). Low ESL devices typically have low capacitance. Likewise, higher capacitance devices typically have higher ESLs. This tradeoff between ESL (speed of energy delivery) and capacitance (energy storage) drives the PDN design topology that places the fastest low ESL capacitors as close to the load as possible. Low Inductance MLCCs are found on semiconductor packages and on boards as close as possible to the load.

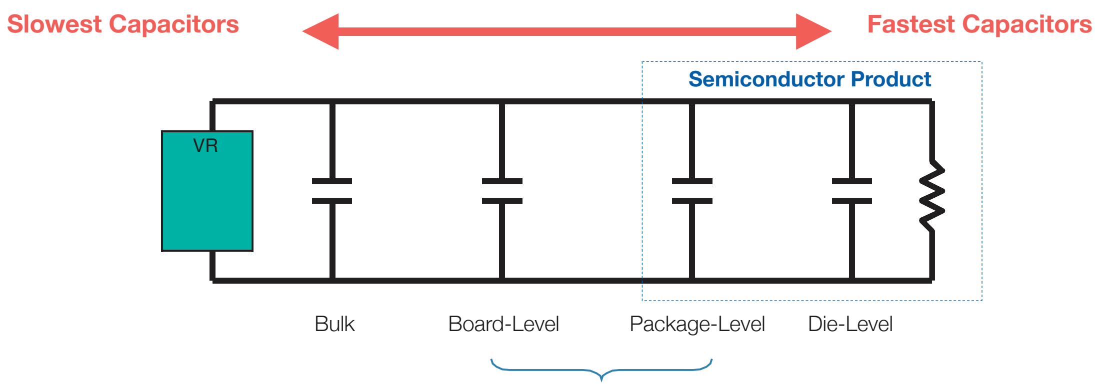

Figure 1 Classic Power Delivery Network (PDN) Architecture

LOW INDUCTANCE CHIP CAPACITORS

The key physical characteristic determining equivalent series inductance (ESL) of a capacitor is the size of the current loop it creates. The smaller the current loop, the lower the ESL. A standard surface mount MLCC is rectangular in shape with electrical terminations on its shorter sides. A Low Inductance Chip Capacitor (LICC®) sometimes referred to as Reverse Geometry Capacitor (RGC) has its terminations on the longer side of its rectangular shape.

When the distance between terminations is reduced, the size of the current loop is reduced. Since the size of the current loop is the primary driver of inductance, an 0306 with a smaller current loop has significantly lower ESL then an 0603. The reduction in ESL varies by EIA size, however, ESL is typically reduced 60% or more with an LICC® versus a standard MLCC.

INTERDIGITATED CAPACITORS

The size of a current loop has the greatest impact on the ESL characteristics of a surface mount capacitor. There is a secondary method for decreasing the ESL of a capacitor. This secondary method uses adjacent opposing current loops to reduce ESL. The InterDigitated Capacitor (IDC) utilizes both primary and secondary methods of reducing inductance. The IDC architecture shrinks the distance between terminations to minimize the current loop size, then further reduces inductance by creating adjacent opposing current loops.

An IDC is one single capacitor with an internal structure that has been optimized for low ESL. Similar to standard MLCC versus LICC®s, the reduction in ESL varies by EIA case size. Typically, for the same EIA size, an IDC delivers an ESL that is at least 80% lower than an MLCC.

Introduction

LAND GRID ARRAY (LGA) CAPACITORS

Land Grid Array (LGA) capacitors are based on the first Low ESL MLCC technology created to specifically address the design needs of current day Power Delivery Networks (PDNs). This is the 3rd low inductance capacitor technology developed by KYOCERA AVX. LGA technology provides engineers with new options. The LGA internal structure and manufacturing technology eliminates the historic need for a device to be physically small to create small current loops to minimize inductance.

The first family of LGA products are 2 terminal devices. A 2 terminal 0306 LGA delivers ESL performance that is equal to or better than an 0306 8 terminal IDC. The 2 terminal 0805 LGA delivers ESL performance that approaches the 0508 8 terminal IDC. New designs that would have used 8 terminal IDCs are moving to 2 terminal LGAs because the layout is easier for a 2 terminal device and manufacturing yield is better for a 2 terminal LGA versus an 8 terminal IDC.

LGA technology is also used in a 4 terminal family of products that KYOCERA AVX is sampling and will formerly introduce in 2008. Beyond 2008, there are new multi-terminal LGA product families that will provide even more attractive options for PDN designers.

LOW INDUCTANCE CHIP ARRAYS (LICA®)

The LICA® product family is the result of a joint development effort between KYOCERA AVX and IBM to develop a high performance MLCC family of decoupling capacitors. LICA was introduced in the 1980s and remains the leading choice of designers in high performance semiconductor packages and high reliability board level decoupling applications.

LICA® products are used in 99.999% uptime semiconductor package applications on both ceramic and organic substrates. The C4 solder ball termination option is the perfect compliment to flip-chip packaging technology. Mainframe class CPUs, ultimate performance multi-chip modules, and communications systems that must have the reliability of 5 9's use LICA®.

LICA® products with either Sn/Pb or Pb-free solder balls are used for decoupling in high reliability military and aerospace applications. These LICA® devices are used for decoupling of large pin count FPGAs, ASICs, CPUs, and other high power ICs with low operating voltages.

When high reliability decoupling applications require the very lowest ESL capacitors, LICA® products are the best option.

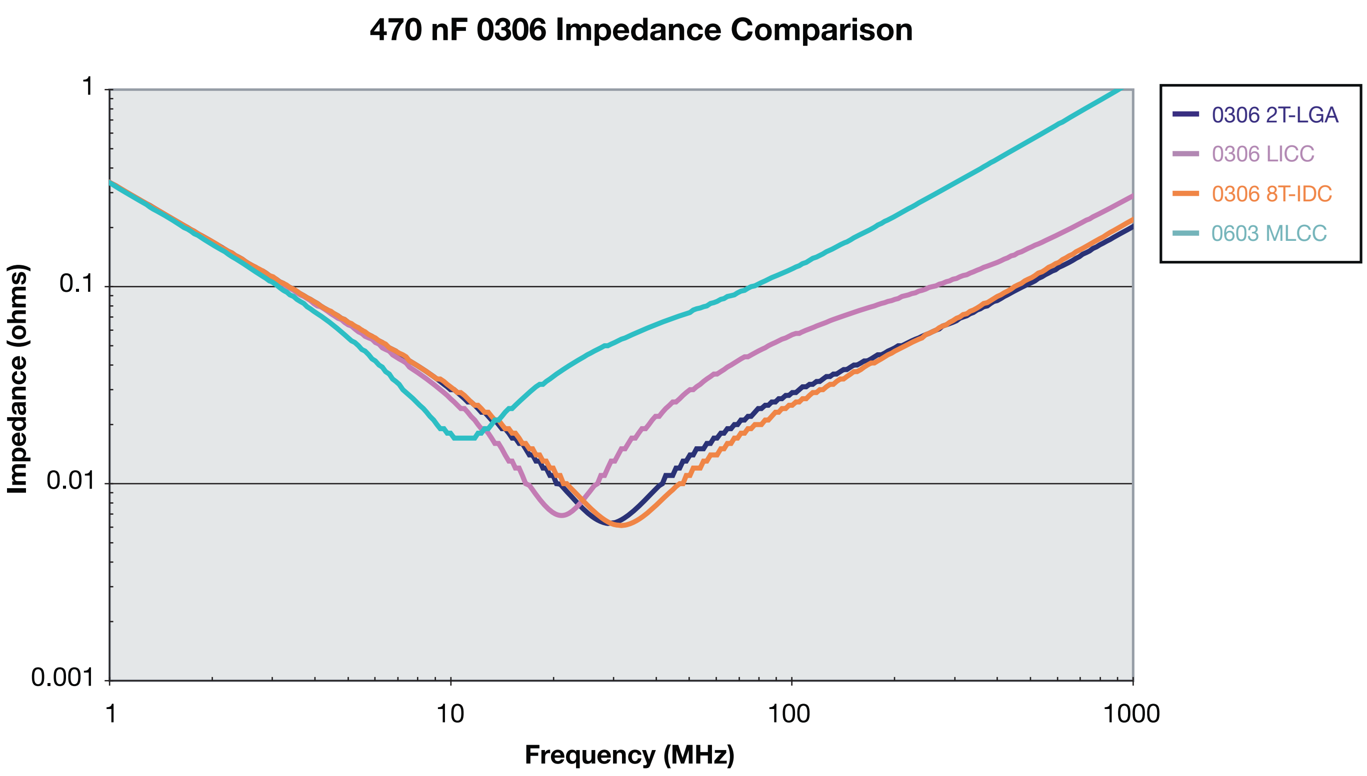

Figure 2 MLCC, LICC®, IDC, and LGA technologies deliver different levels of equivalent series inductance (ESL).

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Low Inductance Capacitors, KGL Series

LICC® (Low Inductance Chip Capacitors) 0204/0306/0508/0612 RoHS Compliant

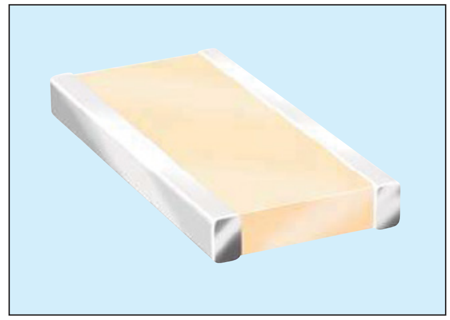
GENERAL DESCRIPTION

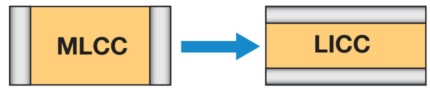
The key physical characteristic determining equivalent series inductance (ESL) of a capacitor is the size of the current loop it creates. The smaller the current loop, the lower the ESL.

A standard surface mount MLCC is rectangular in shape with electrical terminations on its shorter sides. A Low Inductance Chip Capacitor (LICC®) sometimes referred to as Reverse Geometry Capacitor (RGC) has its terminations on the longer sides of its rectangular shape. The image on the right shows the termination differences between an MLCC and an LICC®.

When the distance between terminations is reduced, the size of the current loop is reduced. Since the size of the current loop is the primary driver of inductance, an 0306 with a smaller current loop has significantly lower ESL then an 0603. The reduction in ESL varies by EIA size, however, ESL is typically reduced 60% or more with an LICC® versus a standard MLCC.

KYOCERA AVX LICC® products are available with a lead-free finish of plated Nickel/Tin.





PERFORMANCE CHARACTERISTICS

Capacitance Tolerances	K = ±10%; M = ±20%
Operation Temperature Range	X7R = -55°C to +125°C X5R = -55°C to +85°C X7S = -55°C to +125°C
Temperature Coefficient	X7R, X5R = ±15%; X7S = ±22%
Voltage Ratings	4, 6.3, 10, 16, 25 VDC
Dissipation Factor	4V, 6.3V = 6.5% max; 10V = 5.0% max; 16V = 3.5% max; 25V = 3.0% max
Insulation Resistance (@+25°C, RVDC)	100,000MΩ min, or 1,000MΩ per μF min.,whichever is less

HOW TO ORDER

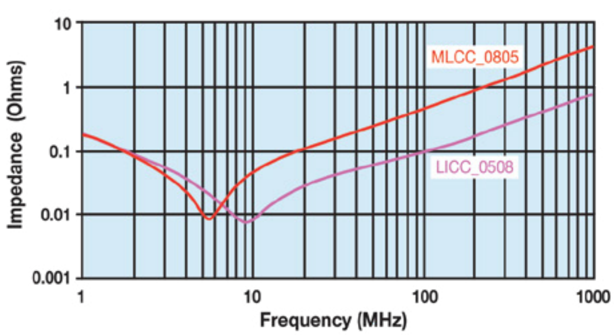
KGL	05	L	S7	0G	104	M	N
Series General Purpose Tin/ Nickel Finish	**Size** 05 = 0204 15 = 0306 21 = 0508 31 = 0612	**Thickness** See Cap Chart	**Dielectric** X7S = S7 X7R = R7 X5R = R5	**Voltage** 0G = 4.0V 0J = 6.3V 1A = 10V 1C = 16V 1E = 25V 1H = 50V	**Capacitance Code Code (in pF)** 2 Significant Digits +Number of zeros eg. 10μF = 106 10nF = 103 47pF = 470	**Capacitance Tolerance** K = ±10% M = ±20%	**Packaging** See Table Below

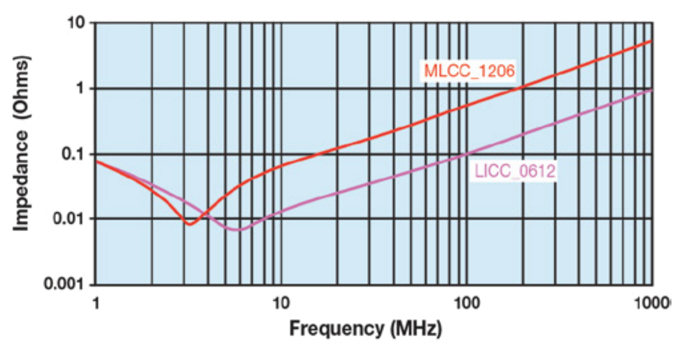
RoHS COMPLIANT

PACKAGING CODES

Code	EIA (inch)	IEC(mm)	7" Paper	7" Embossed	13" Paper	13"Embossed
05	0204	1005	H		N	
15	0306	1608	T		M	
21	0508	2012	T	U	M	L
31	0612	3216	T	U	M	L

TYPICAL IMPEDANCE CHARACTERISTICS





Low Inductance Capacitors, KGL Series

LICC® (Low Inductance Chip Capacitors) 0204/0306/0508/0612 RoHS Compliant

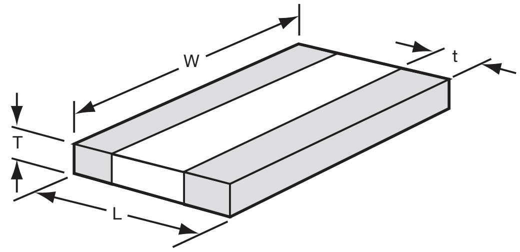
SIZE		0204				0306					0508					0612				
Packaging		Paper				Paper					Paper/Embossed					Paper/Embossed				
Length	mm (in.)	0.50 ± 0.05 (0.020 ± 0.002)				0.81 + 0.15 (0.032 ± 0.006)					1.27 + 0.25 (0.050 ± 0.010)					1.60 + 0.25 (0.063 ± 0.010)				
Width	mm (in.)	1.00 ± 0.05 (0.040 ± 0.002)				1.60 + 0.15 (0.063 ± 0.006)					2.00 + 0.25 (0.080 ± 0.010)					3.20 + 0.25 (0.126 ± 0.010)				
Cap Code	WVDC	4	6.3	10	16	4	6.3	10	16	25	6.3	10	16	25	50	6.3	10	16	25	50
102	Cap 0.001						Z	Z	Z	Z	Y	Y	Y	Y	Y	U	U	U	U	Z
222	(μF) .0022						Z	Z	Z	Z	P	P	P	P	Y	U	U	U	U	Z
332	0.0033						Z	Z	Z	Z	P	P	P	P	Y	U	U	U	U	Z
472	0.0047						Z	Z	Z	Z	P	P	P	P	Y	U	U	U	U	Z
682	0.0068						Z	Z	Z	Z	P	P	P	P	Y	U	U	U	U	Z
103	0.01						Z	Z	Z	Z	P	P	P	P	Y	U	U	U	U	Z
153	0.015						Z	Z	Z	Z	P	P	P	P	Y	U	U	U	U	C
223	0.022						Z	Z	Z	Z	P	P	P	P	Y	U	U	U	U	C
333	0.033						Z	Z	Z		P	P	P	Y	Y	U	U	U	U	C
473	0.047						Z	Z	Z		P	P	P	Y	D	U	U	U	U	C
683	0.068						Z	Z	Z		P	P	P	D	D	U	U	U	Z	C
104	0.1	L					Z	Z	Z		P	P	Y	D	D	U	U	U	Z	C
154	0.15						Z	Z			P	P	Y			U	U	U	C	C
224	0.22						Z	Z			P	P	D			U	U	Z	C	
334	0.33										Y	Y	D			U	U	Z		
474	0.47										Y	Y	D			U	U	Z		
684	0.68										D	D				Z	Z	C		
105	1					Z					D	D				Z	Z	N		
155	1.5										D					C	C			
225	2.2															N	N			
335	3.3															N				
475	4.7																			
685	6.8																			
106	10																			

X7S | X7R | X5R

Case Size	0204 (KGL 05)	0306 (KGL 15)	0508 (KGL 21)			0612 (KGL 31)			
Thickness Letter	L	Z	D	Y	P	C	N	U	Z
Max Thickness(mm)	0.35	0.55	1.02	0.76	0.55	1.02	1.27	0.55	0.76
Carrier Tape	PAPER	PAPER	EMB	PAPER		EMB	EMB	PAPER	PAPER
Packaging Code 7"reel	H	T	U	T	T	U	U	T	T
Packaging Code 13"reel	N	M	L	M	M	L	L	M	M

PAPER | Embossed(EMB)

PHYSICAL DIMENSIONS AND PAD LAYOUT



PHYSICAL DIMENSIONS

MM (IN.)

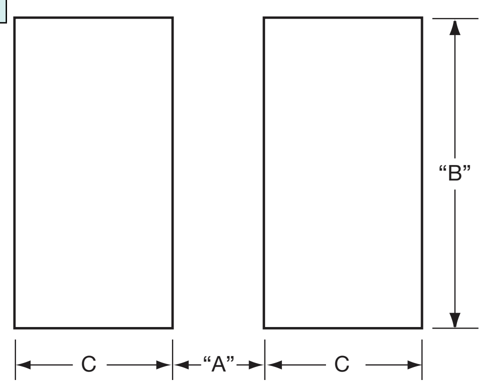
Size	L	W	t
0204	0.50 ± 0.05 (0.020 ± 0.002)	1.00 ± 0.05 (0.040 ± 0.002)	0.18 ± 0.08 (0.007 ± 0.003)
0306	0.81 ± 0.15 (0.032 ± 0.006)	1.60 ± 0.15 (0.063 ± 0.006)	0.13 min. (0.005 min.)
0508	1.27 ± 0.25 (0.050 ± 0.010)	2.00 ± 0.25 (0.080 ± 0.010)	0.13 min. (0.005 min.)
0612	1.60 ± 0.25 (0.063 ± 0.010)	3.20 ± 0.25 (0.126 ± 0.010)	0.13 min. (0.005 min.)

T - See Range Chart for Thickness and Codes

PAD LAYOUT DIMENSIONS

MM (IN.)

Size	A	B	C
0306	0.31 (0.012)	1.52 (0.060)	0.51 (0.020)
0508	0.51 (0.020)	2.03 (0.080)	0.76 (0.030)
0612	0.76 (0.030)	3.05 (0.120)	0.635 (0.025)
0204			



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