

IDC Low Inductance Capacitors (RoHS)

0306/0612/0508 IDC (InterDigitated Capacitors)

GENERAL DESCRIPTION

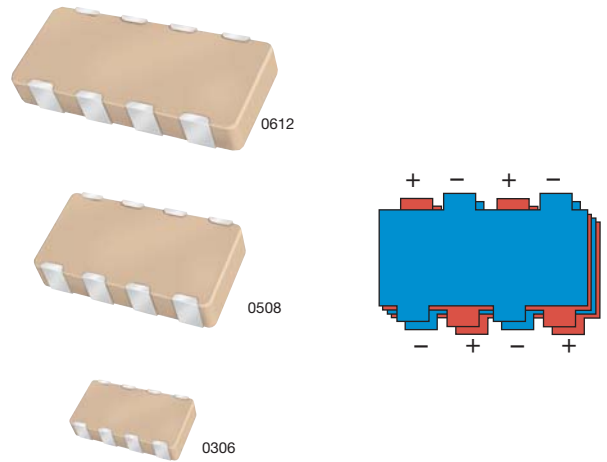
Inter-Digitated Capacitors (IDCs) are used for both semiconductor package and board level decoupling. The equivalent series inductance (ESL) of a single capacitor or an array of capacitors in parallel determines the response time of a Power Delivery Network (PDN). The lower the ESL of a PDN, the faster the response time. A designer can use many standard MLCCs in parallel to reduce ESL or a low ESL Inter-Digitated Capacitor (IDC) device. These IDC devices are available in versions with a maximum height of 0.95mm or 0.55mm.

IDCs are typically used on packages of semiconductor products with power levels of 15 watts or greater. Inter-Digitated Capacitors are used on CPU, GPU, ASIC, and ASSP devices produced on 0.13 μ m, 90nm, 65nm, and 45nm processes. IDC devices are used on both ceramic and organic package substrates. These low ESL surface mount capacitors can be placed on the bottom side or the top side of a package substrate. The low profile 0.55mm maximum height IDCs can easily be used on the bottom side of BGA packages or on the die side of packages under a heat spreader.

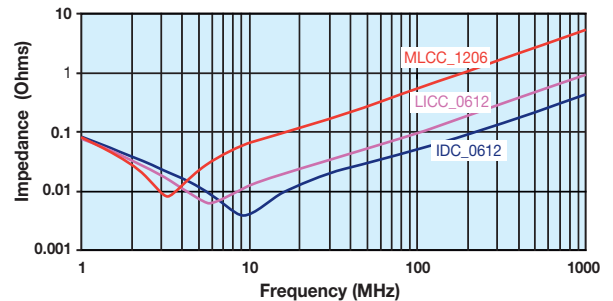
IDCs are used for board level decoupling of systems with speeds of 300MHz or greater. Low ESL IDCs free up valuable board space by reducing the number of capacitors required versus standard MLCCs. There are additional benefits to reducing the number of capacitors beyond saving board space including higher reliability from a reduction in the number of components and lower placement costs based on the need for fewer capacitors.

The Inter-Digitated Capacitor (IDC) technology was developed by AVX. This is the second family of Low Inductance MLCC products created by AVX. IDCs are a cost effective alternative to AVX's first generation low ESL family for high-reliability applications known as LICA (Low Inductance Chip Array).

AVX IDC products are available with a lead-free finish of plated Nickel/Tin.



TYPICAL IMPEDANCE



HOW TO ORDER

W	3	L	1	6	D	225	M	A	T	3	A
Style	IDC Case Size	Low Inductance	Number of Terminals	Voltage	Dielectric	Capacitance Code (In pF)	Capacitance Tolerance	Failure Rate	Termination	Packaging	Thickness
	2 = 0508 3 = 0612 4 = 0306		1 = 8 Terminals	4 = 4V 6 = 6.3V Z = 10V Y = 16V 3 = 25V	C = X7R D = X5R Z = X7S	2 Sig. Digits + Number of Zeros	M = $\pm 20\%$	A = N/A	T = Plated Ni and Sn	Available 1=7" Reel 3=13" Reel	Max. Thickness mm (in.) A=Standard S=0.55 (0.022)

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

PERFORMANCE CHARACTERISTICS

Capacitance Tolerance	$\pm 20\%$ Preferred
Operation Temperature Range	X7R = -55°C to +125°C X5R = -55°C to +85°C X7S = -55°C to +125°C
Temperature Coefficient	$\pm 15\%$ (OVDC), $\pm 22\%$ (X7S)
Voltage Ratings	4, 6.3, 10, 16, 25 VDC
Dissipation Factor	$\leq 6.3V = 6.5\%$ max; 10V = 5.0% max; $\geq 16V = 3.5\%$ max
Insulation Resistance (@+25°C, RVDC)	100,000M Ω min, or 1,000M Ω per μF min., whichever is less

Dielectric Strength	No problems observed after 2.5 x RVDC for 5 seconds at 50mA max current
CTE (ppm/C)	12.0
Thermal Conductivity	4-5W/M K
Terminations Available	Plated Nickel and Solder

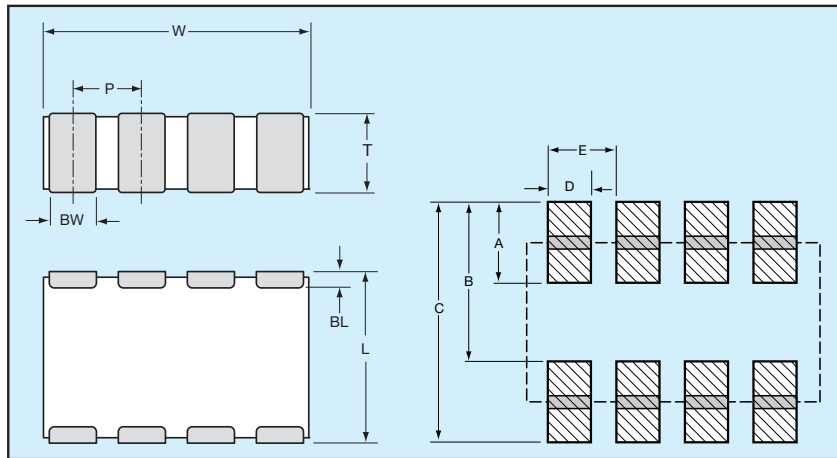
IDC Low Inductance Capacitors (RoHS)

0306/0612/0508 IDC (InterDigitated Capacitors)

SIZE	0306		Thin 0508			0508			Thin 0612				0612					THICK 0612							
Max. Thickness	0.55 (0.022)		0.55 (0.022)			0.95 (0.037)			0.55 (0.022)				0.95 (0.037)					1.22 (0.048)							
WVDC	4	6.3	4	6.3	10	16	25	4	6.3	10	16	25	4	6.3	10	16	4	6.3	10	16	25	4	6.3	10	16
Cap (μF)	This table contains a grid of colored cells representing availability. Blue cells (X7S) are in the first column for sizes 0306 and 0612. Tan cells (X7R) are in columns 3-12 for sizes 0306, 0508, and 0612. Red cells (X5R) are scattered in various columns for sizes 0508, 0612, and THICK 0612.																								

PHYSICAL DIMENSIONS AND PAD LAYOUT

Consult factory for additional requirements



- = X7R
- = X5R
- = X7S

PHYSICAL CHIP DIMENSIONS millimeters (inches)

SIZE	W	L	BW	BL	P
0306	1.60 ± 0.20 (0.063 ± 0.008)	0.82 ± 0.10 (0.032 ± 0.006)	0.25 ± 0.10 (0.010 ± 0.004)	0.20 ± 0.10 (0.008 ± 0.004)	0.40 ± 0.05 (0.015 ± 0.002)
0508	2.03 ± 0.20 (0.080 ± 0.008)	1.27 ± 0.20 (0.050 ± 0.008)	0.30 ± 0.10 (0.012 ± 0.004)	0.25 ± 0.15 (0.010 ± 0.006)	0.50 ± 0.05 (0.020 ± 0.002)
0612	3.20 ± 0.20 (0.126 ± 0.008)	1.60 ± 0.20 (0.063 ± 0.008)	0.50 ± 0.10 (0.020 ± 0.004)	0.25 ± 0.15 (0.010 ± 0.006)	0.80 ± 0.10 (0.031 ± 0.004)

PAD LAYOUT DIMENSIONS

SIZE	A	B	C	D	E
0306	0.38 (0.015)	0.89 (0.035)	1.27 (0.050)	0.20 (0.008)	0.40 (0.015)
0508	0.64 (0.025)	1.27 (0.050)	1.91 (0.075)	0.28 (0.011)	0.50 (0.020)
0612	0.89 (0.035)	1.65 (0.065)	2.54 (0.101)	0.45 (0.018)	0.80 (0.031)

IDC Low Inductance Capacitors (SnPb)

0306/0612/0508 IDC with Sn/Pb Termination

GENERAL DESCRIPTION

Inter-Digitated Capacitors (IDCs) are used for both semiconductor package and board level decoupling. The equivalent series inductance (ESL) of a single capacitor or an array of capacitors in parallel determines the response time of a Power Delivery Network (PDN). The lower the ESL of a PDN, the faster the response time. A designer can use many standard MLCCs in parallel to reduce ESL or a low ESL Inter-Digitated Capacitor (IDC) device. These IDC devices are available in versions with a maximum height of 0.95mm or 0.55mm.

IDCs are typically used on packages of semiconductor products with power levels of 15 watts or greater. Inter-Digitated Capacitors are used on CPU, GPU, ASIC, and ASSP devices produced on 0.13 μ m, 90nm, 65nm, and 45nm processes. IDC devices are used on both ceramic and organic package substrates. These low ESL surface mount capacitors can be placed on the bottom side or the top side of a package substrate. The low profile 0.55mm maximum height IDCs can easily be used on the bottom side of BGA packages or on the die side of packages under a heat spreader.

IDCs are used for board level decoupling of systems with speeds of 300MHz or greater. Low ESL IDCs free up valuable board space by reducing the number of capacitors required versus standard MLCCs. There are additional benefits to reducing the number of capacitors beyond saving board space including higher reliability from a reduction in the number of components and lower placement costs based on the need for fewer capacitors.

The Inter-Digitated Capacitor (IDC) technology was developed by AVX. This is the second family of Low Inductance MLCC products created by AVX. IDCs are a cost effective alternative to AVX's first generation low ESL family for high-reliability applications known as LICA (Low Inductance Chip Array).

AVX IDC products are available with a lead termination for high reliability military and aerospace applications that must avoid tin whisker reliability issues.



TYPICAL IMPEDANCE



Not RoHS Compliant

HOW TO ORDER

L	3	L	1	6	D	225	M	A	B	3	A
Style	IDC Case Size	Low Inductance	Number of Terminals	Voltage	Dielectric	Capacitance Code (In pF)	Capacitance Tolerance	Failure Rate	Termination	Packaging Available	Thickness
	2 = 0508 3 = 0612 4 = 0306		1 = 8 Terminals	4 = 4V 6 = 6.3V Z = 10V Y = 16V 3 = 25V	C = X7R D = X5R Z = X7S	2 Sig. Digits + Number of Zeros	M = $\pm 20\%$	A = N/A	B = 5% min. Lead	1=7" Reel 3=13" Reel	Max. Thickness mm (in.) A=Standard S=0.55 (0.022)

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

PERFORMANCE CHARACTERISTICS

Capacitance Tolerance	$\pm 20\%$ Preferred
Operation Temperature Range	X7R = -55°C to +125°C X5R = -55°C to +85°C X7S = -55°C to +125°C
Temperature Coefficient	$\pm 15\%$ (0VDC), $\pm 22\%$ (X7S)
Voltage Ratings	4, 6.3, 10, 16, 25 VDC
Dissipation Factor	$\leq 6.3V = 6.5\%$ max; 10V = 5.0% max; $\geq 16V = 3.5\%$ max
Insulation Resistance (@+25°C, RVDC)	100,000M Ω min, or 1,000M Ω per μ F min., whichever is less

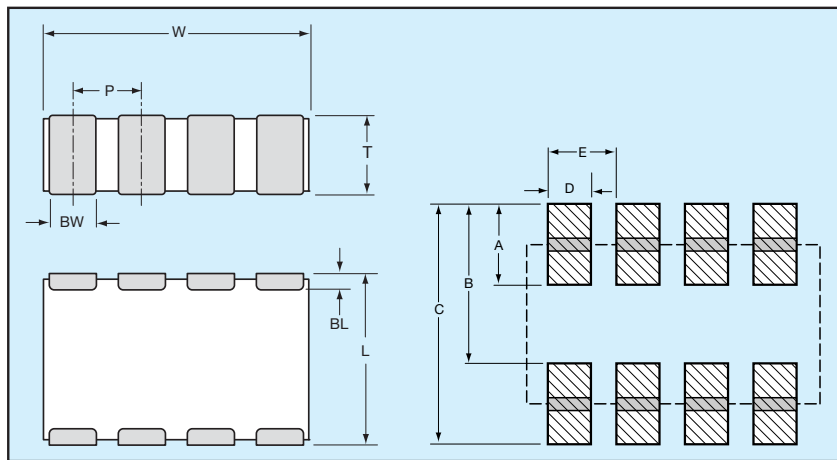
Dielectric Strength	No problems observed after 2.5 x RVDC for 5 seconds at 50mA max current
CTE (ppm/C)	12.0
Thermal Conductivity	4-5W/M K
Terminations Available	Plated Nickel and Solder

IDC Low Inductance Capacitors (SnPb)

0306/0612/0508 IDC with Sn/Pb Termination

SIZE	0306		Thin 0508			0508			Thin 0612				0612					THICK 0612							
Max. Thickness	0.55 (0.022)		0.55 (0.022)			0.95 (0.037)			0.55 (0.022)				0.95 (0.037)					1.22 (0.048)							
WVDC	4	6.3	4	6.3	10	16	25	4	6.3	10	16	25	4	6.3	10	16	4	6.3	10	16	25	4	6.3	10	16
Cap (μF)	This table contains a grid of colored cells representing availability. Row 0.010: 0306 (4, 6.3) are blue (X7S); others are brown (X7R). Row 0.022: 0306 (4, 6.3) are blue (X7S); others are brown (X7R). Row 0.033: 0306 (4, 6.3) are blue (X7S); others are brown (X7R). Row 0.047: 0306 (4, 6.3) are blue (X7S); others are brown (X7R). Row 0.068: 0306 (4, 6.3) are blue (X7S); others are brown (X7R). Row 0.10: 0306 (4, 6.3) are blue (X7S); 0508 (10, 16) are red (X5R); others are brown (X7R). Row 0.22: 0306 (4, 6.3) are blue (X7S); others are brown (X7R). Row 0.33: 0306 (4, 6.3) are blue (X7S); others are brown (X7R). Row 0.47: 0306 (4, 6.3) are blue (X7S); others are brown (X7R). Row 0.68: 0306 (4, 6.3) are blue (X7S); 0508 (4, 6.3) and 0612 (4, 6.3) are red (X5R); others are brown (X7R). Row 1.0: 0306 (4, 6.3) are blue (X7S); 0508 (4, 6.3) and 0612 (4, 6.3) are red (X5R); 0612 (10, 16) are brown (X7R); THICK 0612 (4, 6.3) are brown (X7R). Row 1.5: 0306 (4, 6.3) are blue (X7S); 0508 (4, 6.3) and 0612 (4, 6.3) are red (X5R); 0612 (10, 16) are brown (X7R); THICK 0612 (4, 6.3) are brown (X7R). Row 2.2: 0306 (4, 6.3) are blue (X7S); 0508 (4, 6.3) and 0612 (4, 6.3) are red (X5R); 0612 (10, 16) are brown (X7R); THICK 0612 (4, 6.3) are brown (X7R). Row 3.3: 0306 (4, 6.3) are blue (X7S); 0612 (4, 6.3) is red (X5R); others are brown (X7R).																								

PHYSICAL DIMENSIONS AND PAD LAYOUT



Consult factory for additional requirements

- = X7R
- = X5R
- = X7S

PHYSICAL CHIP DIMENSIONS millimeters (inches)

SIZE	W	L	BW	BL	P
0306	1.60 ± 0.20 (0.063 ± 0.008)	0.82 ± 0.10 (0.032 ± 0.006)	0.25 ± 0.10 (0.010 ± 0.004)	0.20 ± 0.10 (0.008 ± 0.004)	0.40 ± 0.05 (0.015 ± 0.002)
0508	2.03 ± 0.20 (0.080 ± 0.008)	1.27 ± 0.20 (0.050 ± 0.008)	0.30 ± 0.10 (0.012 ± 0.004)	0.25 ± 0.15 (0.010 ± 0.006)	0.50 ± 0.05 (0.020 ± 0.002)
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PAD LAYOUT DIMENSIONS

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