User Guide 60-SIPT Development Kit

21 November 2017

Version 1.2

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Europe: +44-1628-858-940
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Revision History

Version	Date	Notes	Approver
1.0	29 July 2017	Initial Release	Jay White
1.1	19 Nov 2017	Converted LaTeX	Steve Braneky
1.2	21 Nov 2017	Updated content	Steve Braneky

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1 Overview

The 60-SIPT development board is a universal development tool to highlight the capabilities of the 60-SIPT module. It offers a platform for rapid wireless connectivity prototyping, providing multiple options for the development of Wi-Fi and Bluetooth applications.

Laird provides two kinds of development kits, DVK-ST60-SIPT and DVK-SU60-SIPT, for the 60-series SIP module. DVK-ST60-SIPT is for the Sterling ST60 product family with a SIP form factor and DVK-SU60-SIPT is for the Summit SU60 product family. Unless otherwise noted all information in this document applies to both versions of the development kits.

This guide applies to Rev. 01 of the development PCB and relates to DVK-60-SIPT_1.0 on the PCB itself.

1.1 Introduction

The Laird 60-SIPT development kit is designed to support the development of applications and software for the 60-SIPT Dual-band 802.11ac Wave2 Wi-Fi + Bluetooth v4.2 module. It supports multiple host interfaces as well as host power requirements, while breakout headers and slide switches enable rapid selection and configuration. More information regarding this product series including additional documentation is available from the 60 Series product page of the Laird website.

1.2 Package Contents

All kits contain the following:

Development board	The development board has the required 60-SIPT module installed onto it and exposes all the various hardware interfaces available.
Power options	USB cable – Type A to micro B. This cable can also provide serial communications via the FTDI USB – RS232 converter chip on the development board. DC barrel plug with clips for connection to external power supply.
SDIO Extender	With pin header supplied to allow a simple connection to the SDIO socket at low speeds. Without pin header supplied for use at higher speeds.
Ribbon cable	Supplied to allow a simple connection to the SDIO socket. **Note: Laird strongly advises this cable be used for SDIO DS and HS speed modes only.**
Antennas	Two 2.4G/5GHz FlexPIFA antennas.
Web link card	Provides links to additional information including the 60-series user guide, schematics, quick start guides, and firmware release notes.

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2 60-SIPT Development Kit - Main Development Board

This section describes the 60-SIPT development board hardware. The 60-SIPT development board is delivered with the 60-SIPT module but no onboard firmware and applications. The complete functionality of the development kit hardware requires the use of Laird 60-SIPT firmware version 08.05.05.26 or greater which Laird makes available for download. The development kit is supplied in a default configuration which should be suitable for multiple experimentation options. It also offers multiple pin headers that help to create different configurations for the 60-SIPT module and allows for testing of different operating scenarios.

The development board allows the 60-SIPT module to physically connect to a SDIO host via the supplied SDIO extension card/cable, to a PCIe host via the PCIe golden finger, and to a USB host via a USB cable for development purposes. The development board also provides USB-to-Virtual COM port conversion through a FTDI chip – part number FT232R. Any Windows or Linux PC should auto-install the necessary drivers; if your PC cannot locate the drivers, you can download them from FTDI Chip.

2.1 Key Features

The 60-SIPT development board contains the following features:

- SU60-SIPT or ST60-SIPT module installed on-board.
- Power supply options for powering development board from:
  - USB
  - External DC supply
  - SDIO interface
  - PCIe interface
- Regulated 3.3 V for powering the 60-SIPT module.
- Optional regulated 1.8 V for powering the VCCIO for FTDI chip.
- USB to UART bridge (FTDI chip)
- USB interface for Wi-Fi or Bluetooth
- PCIe interface for Wi-Fi
- SDIO interface for Wi-Fi or Bluetooth
- UART interface for Bluetooth
- Module UART can be interfaced to:
  - USB (PC) using the USB-UART bridge
  - External UART source

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- Current measuring options:
  - Pin header (Ammeter)
- IO break-out (2.54 mm pitch headers) connectors interface for plugging-in external modules and accessing all interfaces of the 60-SIPT module.
  - UART
  - LTE coexistence
  - PCM
  - GPIO
  - JTAG
- Two buttons and LEDs for user interaction
- Seven slide switches for DC source, IO level, and host config
- External 32.768 kHz oscillator for the sleep clock

2.2 Understsanding the Development Board

Figure 1 below provides an overview of certain components and signals on the development board.

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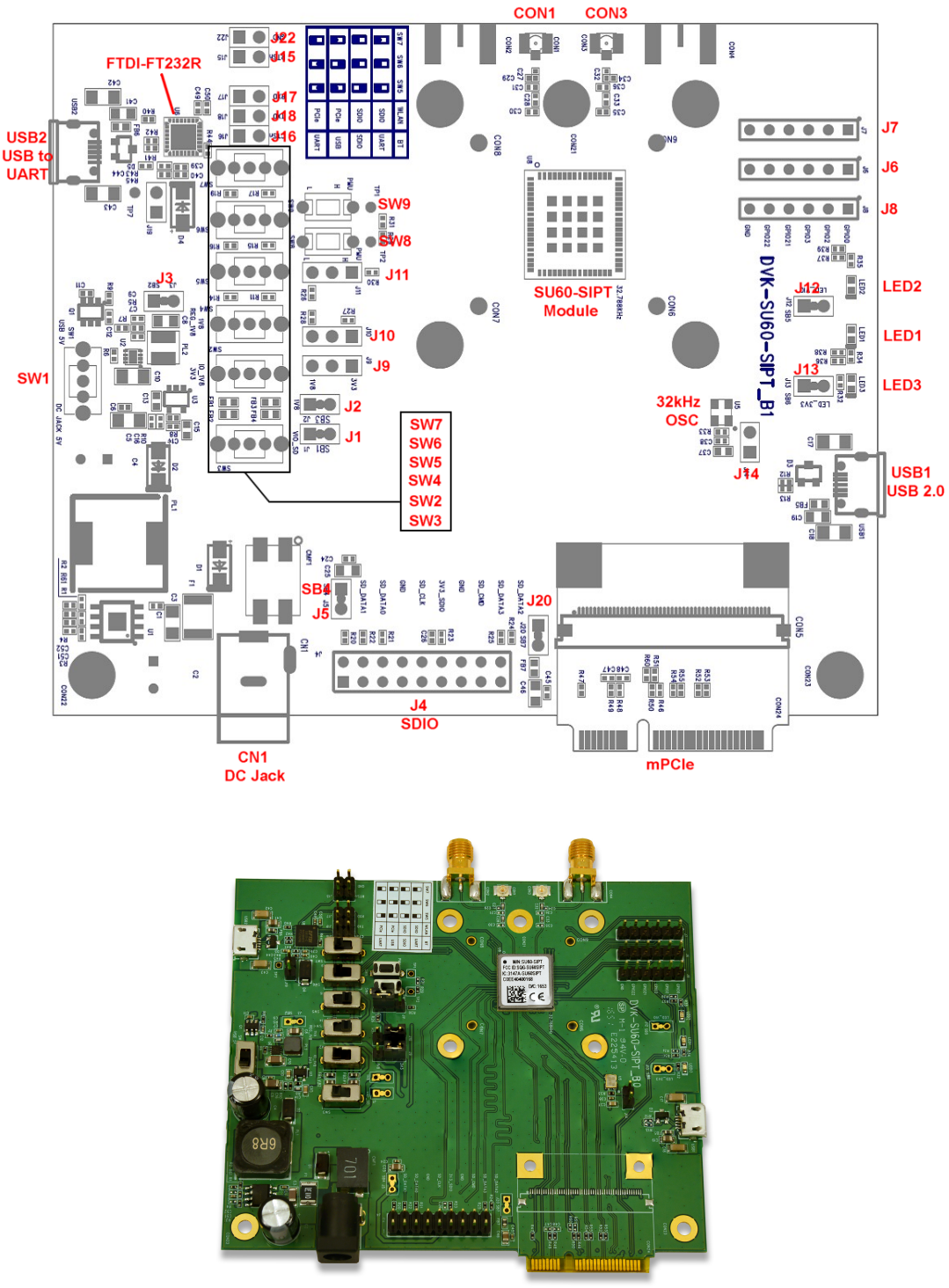

Figure 1: Development board

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3 Functional Blocks

The development board is formed from the following major functional blocks:

3.1 Pin Definitions

3.1.1 SDIO-Pin Header

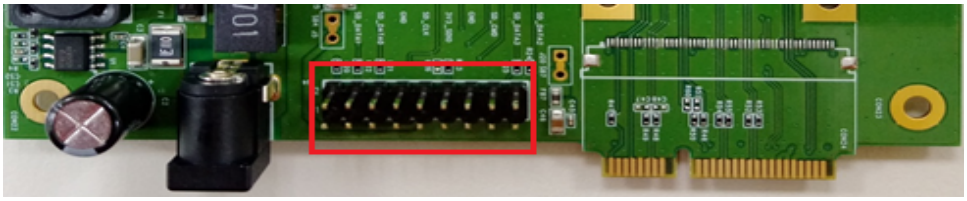

Figure 2: DVK-60-SIP SDIO pin header

Table 1: SDIO pin definitions

Pin #	Name	Type	Voltage Ref.	Description	If Not Used
1	GND	-	-	Ground	GND
2	SDIO DATA2	I/O,PU	1.8V	SDIO 4-bit Mode DATA line Bit[2]	N/C
3	GND	-	-	Ground	GND
4	SDIO DATA3	I/O,PU	1.8V	SDIO 4-bit Mode DATA line Bit[3]	N/C
5	GND	-	-	Ground	GND
6	SDIO CMD	I/O	1.8V	SDIO 4-bit Mode Command/Response	N/C
7	GND	-	-	Ground	GND
8	GND	-	-	Ground	GND
9	SDIO_3V3	Power	-	3.3V module power supply	-
10	SDIO_3V3	Power	-	3.3V module power supply	-
11	GND	-	-	Ground	GND
12	SDIO CLK	I,PU	1.8V	SDIO 4-bit Mode Clock Input	N/C
13	GND	-	-	Ground	GND
14	GND	-	-	Ground	GND
15	GND	-	-	Ground	GND
16	SDIO DATA0	I/O,PU	1.8V	SDIO 4-bit Mode DATA line Bit[0]	N/C
17	GND	-	-	Ground	GND
18	SDIO DATA1	I/O,PU	1.8V	SDOI 4-bit Mode DATA line Bit[1]	N/C

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3.1.2 PCIe Golden Finger

Table 2: PCIe pin definitions

Pin #	Name	Type	Voltage Ref.	Description	If Not Used
1	PEWAKE0#	I/O	3.3V	PCIe wake signal	N/C
2	PCIE_3V3	Power	-	3.3V module power supply	-
3	-	-	-	-	-
4	GND	-	-	Ground	GND
5	-	-	-	-	-
6	-	-	-	-	-
7	CLKREQ0#	I/O	3.3V	PCIe clock request	GND
8	-	-	-	-	-
9	GND	-	-	Ground	GND
10	-	-	-	-	-
11	REFCLKn0	I	1.8V	PCIe Differential Clock Input-Negative	N/C
12	-	-	-	-	-
13	REFCLKp0	I	1.8V	PCIe Differential Clock Input-Postiive	N/C
14	-	-	-	-	-
15	GND	-	-	Ground	GND
16	-	-	-	-	-
17	-	-	-	-	-
18	GND	-	-	Ground	GND
19	-	-	-	-	-
20	W_DISABLE1#	I,PU	3.3V	PCIe host indication to disable the WLAN function of the device	N/C
21	GND	-	-	Ground	GND
22	PERST0#	I,PD	3.3V	PCIe host indication to reset the device	N/C
23	PETn0	O	1.8V	PCIe Transmit Data-Negative	N/C
24	PCIE_3V3	Power	-	3.3V module power supply	-
25	PETp0	O	1.8V	PCIe Transmit Data-Positive	N/C
26	GND	-	-	Ground	GND
27	GND	-	-	Ground	GND
28	-	-	-	-	-
29	GND	-	-	Ground	GND
30	-	-	-	-	-
31	PERn0	I	1.8V	PCIe Receive Data-Negative	N/C
32	-	-	-	-	-
33	PERp0	I	1.8V	PCIe Receive Data-Positive	N/C
34	GND	-	-	Ground	GND
35	GND	-	-	Ground	GND
36	USB_D-	I/O	3.3V	USB Differential Data-Negative	N/C
37	GND	-	-	Ground	GND
38	USB_D+	I/O	3.3V	USB Differential Data-Positive	N/C
39	PCIE_3V3	Power	-	3.3V module power supply	-

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Table 3: PCIe pin definitions continued

Pin #	Name	Type	Voltage Ref.	Description	If Not Used
40	GND	-	-	Ground	GND
41	PCIE_3V3	Power	-	3.3V module power supply	-
42	-	-	-	-	-
43	GND	Power	-	Ground	GND
44	LED1#	O,PU	3.3V	LED indicator for WLAN with 10mA drive capability	N/C
45	-	-	-	-	-
46	LED2#	O,PU	3.3V	LED indicator for BT with 10mA drive capability	N/C
47	-	-	-	-	-
48	-	-	-	-	-
49	-	-	-	-	-
50	GND	-	-	Ground	GND
51	-	-	-	-	-
52	PCIE_3V3	Power	-	3.3V module power supply	-

3.2 Power Supply

3.2.1 3.3V source

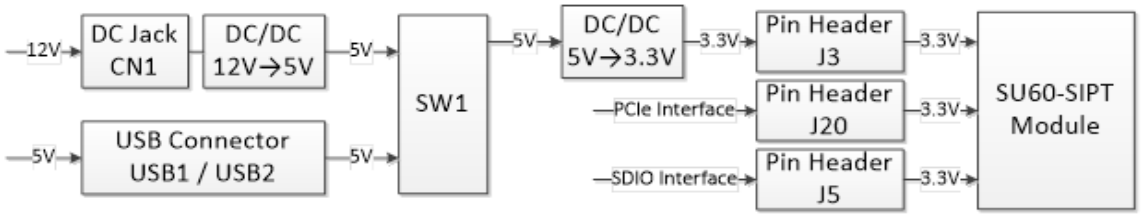

Figure 3: DVK-60-SIPT 3.3V power supply options

The DVK-60-SIPT development board requires a 3.3V power source which is used to supply 3.3V to the 60-SIPT module only.

The 3.3V rail can be obtained from a DC 12V supply (into DC jack connector CN1), USB type micro-B connector (USB1 and USB2), or directly from the host interface (PCIe or SDIO assuming SDIO VIO is using 3.3V).

A power source fed into the DC jack is regulated down to 5V with an on-board regulator and wired to SW1, as is the 5V from the USB. Switch SW1 selects between the regulated 5V and USB 5V. The SW1 5V output,from either the USB or the DC jack, is then regulated down to 3.3V with an on-board regulator on the development board.

The voltage from host interface (PCIe or SDIO interface) is not regulated but is fed directly to 60-SIPT module supply pin.

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Depending on the 3.3V supply used the header connector J3, J20, or J5 (see Figure 4) may be used to measure the current of the 3V3 power domain .

Note: For the initial out-of-the-box setup Laird recommends using the 12V DC supply when possible to eliminate issues such as failures to initialize the firmware do to too heavy of a load for the power source.

3.2.2 VIO/VIO_SD source

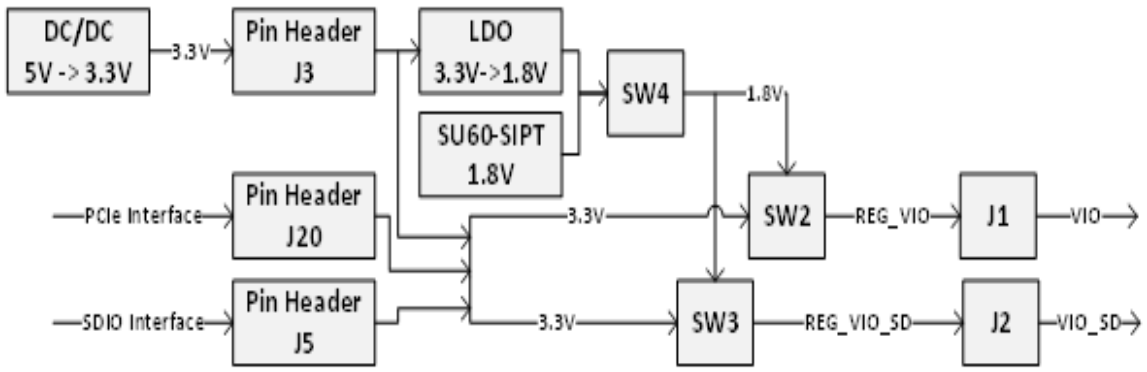

Figure 4: DVK-60-SIPT VIO & VIO_SD power supply

The DVK-60-SIPT development boards allow for the configuration of VIO and VIO_SD supplies to accomodate both 1.8V and 3.3V host platforms.

Switch SW2 is used to select between 3.3V and 1.8V for the VIO rail. While switch SW3 is used to select between 3.3V and 1.8V for the VIO_SD rail. The default positions for both SW2 and SW3 is to select the regulated 3.3V.

SW4 is used to select the regulated 1.8V from the LDO or the 1.8V from the 60-SIPT. The default for SW4 is to select the LDO 1.8V.

3.3 Host Interface Configuration

The development board has three slide switches (SW5, SW6, SW7) for bootstrapping of the host interfaces. To view their settings, refer to Table 4.

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Table 4: Bootstrap configuration

Strap Value SW7, SW6, SW5 CON[0], CON[1], CON[2]	WLAN	BT
000	SDIO	UART
001	SDIO	SDIO
010	PCIe	USB 2.0
011	PCIe	UART
101	USB 2.0	USB 2.0

A value of '0' can be selected by sliding the switch towards the USB2 connector while a value of '1' can be selected by sliding the switch towards the 60-SIPT Module (see Figure 1).

3.4 Tact Switches

The 60-SIPT development board has two tact switches (SW8, SW9). To view their locations, refer to Figure 1.

3.4.1 PDn (SW9)

The Full Power-Down signal (PDn) is an active low input used to reset the 60-SIPT Module. It can use either 1.8V or 3.3V as an input and may be driven by the host. Note that there is an internal pull-up resistor on this pin and PDn must be high for normal operation.

The Power-Down tact switch SW9 may be used to manually assert the PDn signal and reset the 60-SIPT module.

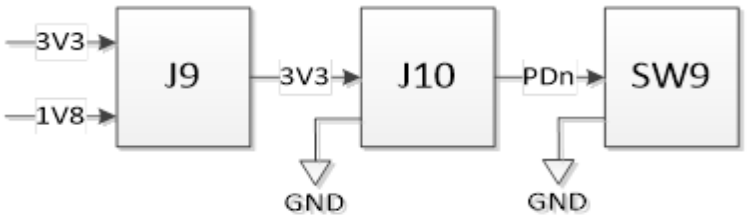

Figure 5: DVK-60-SIPT PDn power supply

Note: J9 can be used to select between the 3.3V and 1.8V rail while J10 pulls the PDn signal high (1.8V/3.3V) or low, 'permanently' disabling the 60-SIPT Module.

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3.4.2 PMU_EN (SW8)

The PMU Enable signal is an active high input used to activate the internal PMU on the 60-SIPT module. PMU_EN can accept 3.3V as an input and may be driven by the host using GPI021 or PCIE_PERST#. Note there is an internal pull-up resistor on this pin and PMU_EN must be high for normal operation.

The PMU Enable tact switch SW8 may be used to manually de-assert the PMU_EN signal and reset the 60-SIPT module's PMU.

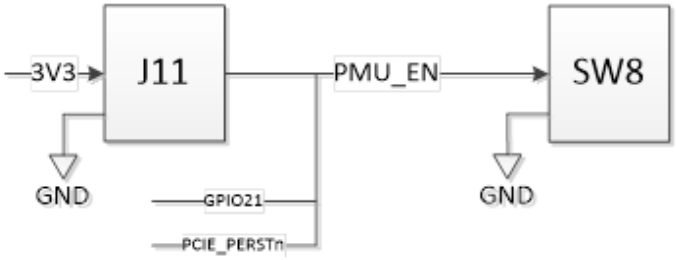

Figure 6: DVK-60-SIPT PMU_EN power supply

Note: J11 can be used to pull PMU_EN signal high (3.3V) or low, 'permanently' disabling the PMU module on the 60-SIPT Module.

Note: PDn and PMU_EN are also wired to TP1 and TP2. To view their location, refer to Figure 1.

3.5 4-wire UART Serial Interface

The 60-SIPT development board provides access to the 60-SIPT module's 4-wire UART interface (TX, RX, CTS, RTS) either through USB (via U6 FTDI USB-UART convertor chip) or through a breakout header connector.

Note: For 3.3V VIO, V_{IH} is from 2.31V to 3.7V; V_{IL} is from -0.4V to 0.99V.
For 1.8V VIO, V_{IH} is from 1.26V to 2.2V; V_{IL} is from -0.4V to 0.54V.

3.5.1 UART Mapping

UART connection on the 60-SIPT module, FTDI IC, and breakout connectors are shown in Table 5. Refer to Figure 1 to see where the 60-SIPT module UART breakout header connectors are located.

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Table 5: UART mapping

SU6-SIPT Default function	Breakout Pin	FTDI IC UART Pin
UART_RXD (O)	J17	TXD
UART_TXD (I)	J18	RXD
UART_CTSn (O)	J16	RTS#
UART_RTSn (I)	J15	CTS#

3.5.2 UART Interface Driven by USB

USB Connector - The development kit provides a USB Type micro-B connector (USB2) which allows connection to any USB host device. The connector optionally supplies power to the development kit and the USB signals are connected to a USB to serial convertor device (FT232R).

USB to UART - The development kit is fitted with a (U6) FTDI FT232R USB to UART converter which provides USB-to-Virtual COM port to facility easy connection of the 60-SIPT Bluetooth module when configured to use the UART port. Upon connection, a Window or Linux PC should auto-install the required drivers. For more details and driver downloads, visit FTDI Chip.

UART interface driven by USB FTDI chip- In normal operation, the 60-SIPT module UART interface is driven by the FTDI FT232R USB to UART converter.

3.5.3 UART Interface Driven by External Source

UART interface driven by external UART source – The 60-SIPT module UART interface (TX, RX, CTS, RTS) is presented at a 2.54 mm (0.1”) pitch headers (J15, J16, J17, and J18).

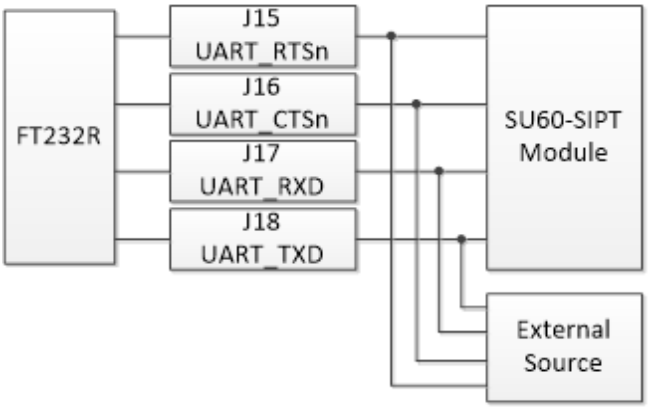

Figure 7: USB to UART Interface and Header to UART interface

Note: To allow the 60-SIPT UART interface to be driven from these breakout connectors, **the development board must be powered from the DC jack (CON5)** and switch SW1 must be in position DC JACK 5V.

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3.6 32.768kHz Oscillator

The development kit is fitted with a (U5) 32.768kHz oscillator which provides sleep clock to 60-SIPT module. Fit a jumper on J14 to disable the sleep clock, if necessary.

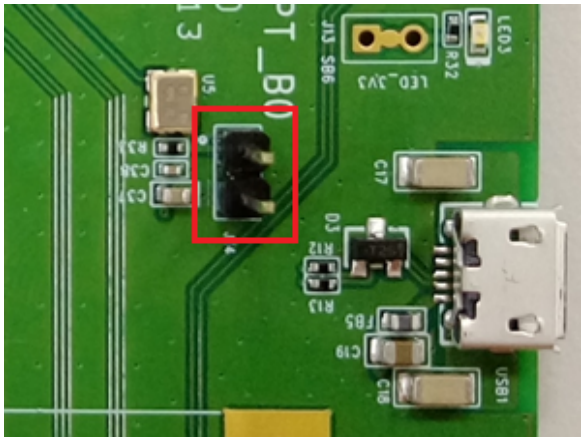

Figure 8: Pin Header J14

3.7 PCM

The development kit provides the Pulse Code Modulation interface signals on J7. The pin descriptions of J7 for PCM signal are shown in Table 6 below.

Table 6: PCM signal pins

J7	Description
Pin 1	GND
Pin 2	PCM_IN
Pin 3	PCM_OUT
Pin 4	PCM_BCLK
Pin 5	PCM_SYNC
Pin 6	GND

Pin 1 on J7 is located the furthest away from the 60-SIPT Module and closest to the development board's edge.

Note: For 3.3V VIO, V_{IH} is from 2.31V to 3.7V; V_{IL} is from -0.4V to 0.99V.
For 1.8V VIO, V_{IH} is from 1.26V to 2.2V; V_{IL} is from -0.4V to 0.54V.

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3.8 LTE Coexistence

The development kit provides the LTE coexistence and JTAG signals on J6. The pin descriptions of J6 are shown in Table 7 below.

Table 7: LTE coexistence pins

J6	Description
Pin 1	GND
Pin 2	LTE_SOUT
Pin 3	LTE_SIN
Pin 4	JTAG_TMS
Pin 5	JTAG_TCK
Pin 6	GND

Pin 1 on J6 is located the furthest away from the 60-SIPT Module and closest to the development board's edge.

Note: For 3.3V VIO, V_{IH} is from 2.31V to 3.7V; V_{IL} is from -0.4V to 0.99V.
For 1.8V VIO, V_{IH} is from 1.26V to 2.2V; V_{IL} is from -0.4V to 0.54V

3.9 GPIOs

The development kit provides GPIO signals on J8. The pin descriptions of J6 are shown in Table 8 below.

Table 8: GPIO pins

J8	Description
Pin 1	GPIO0 WoW for Wi-Fi
Pin 2	GPIO2 LED WLAN
Pin 3	GPIO3 LED BT WoW for Bluetooth
Pin 4	GPIO21
Pin 5	GPIO22
Pin 6	GND

Pin 1 on J8 is located the furthest away from the 60-SIPT Module and closest to the development board's edge.

Note: For 3.3V VIO, V_{IH} is from 2.31V to 3.7V; V_{IL} is from -0.4V to 0.99V.
For 1.8V VIO, V_{IH} is from 1.26V to 2.2V; V_{IL} is from -0.4V to 0.54V

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3.10 LED Indicator

The development kit provides three LED Indicators. These indicators provide visual feedback that things are powered correctly and working.

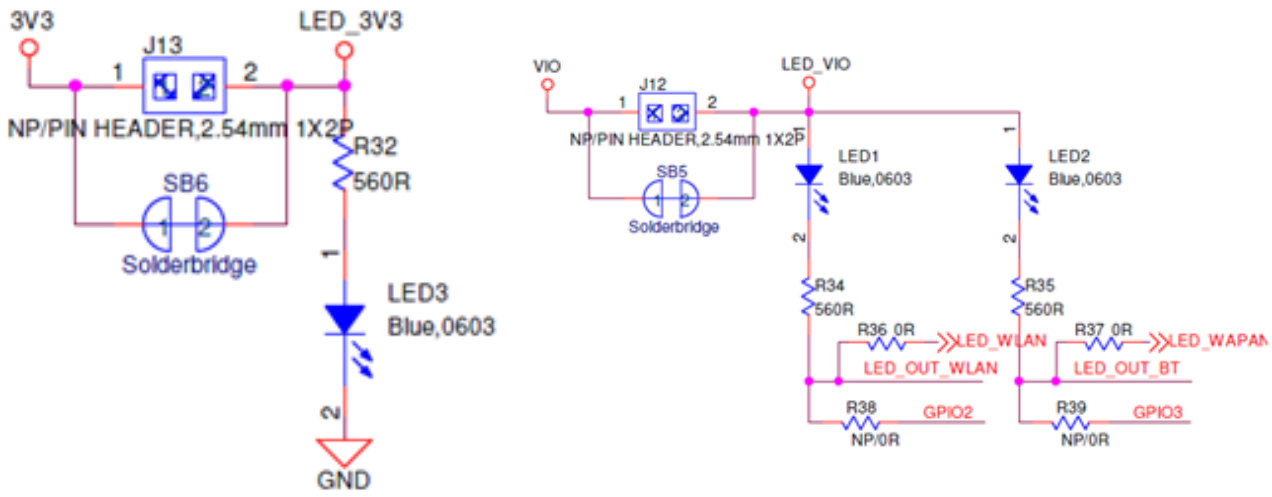

Figure 9: LED Indicators

Table 9: LED pins

LEDs	Description
LED1	WLAN status (Active Low)
LED2	BT status (Active Low)
LED3	3.3V Module Power

Note: J12 and J13 may be removed to disable the LEDs.

3.11 U.FL Connector

The development kit provides U.FL connectors for RF measurement.

Table 10: U.FL connectors

U.FL	Description
CON3	ANT0(Wi-Fi)
CON1	ANT1(Wi-Fi+BT)

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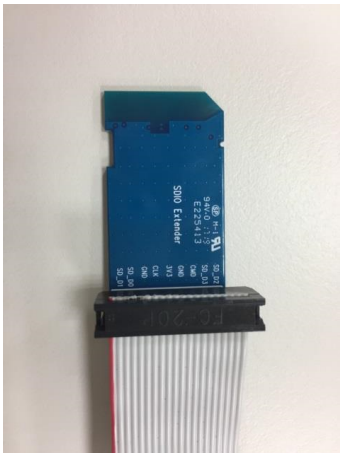
4 DVK Setup with SDIO 2.0 and SDIO 3.0 Host

With SDIO 2.0 and SDIO 3.0, the development kit setup is different not only in the DVK board switch settings, but also with the SDIO connector wiring. Which way to setup the DVK's SDIO environment will depend on the SDIO host controller.

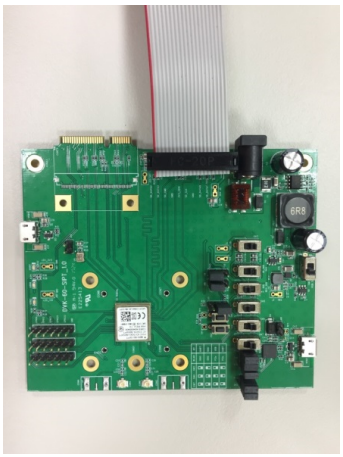
4.1 Environment setup with a SDIO 2.0 host

To wire the DVK-60-SIPT for a SDIO 2.0 host, follow these steps:

1. Wire one side of ribbon cable to the SDIO extender with pin header. The SD-D1 should align with the connector marked in red.



2. Wire the other side of ribbon cable with the connector on the DVK-60-SIPT board. The pin closest to the nearby PCIe bus should be aligned with the connector marked in red.



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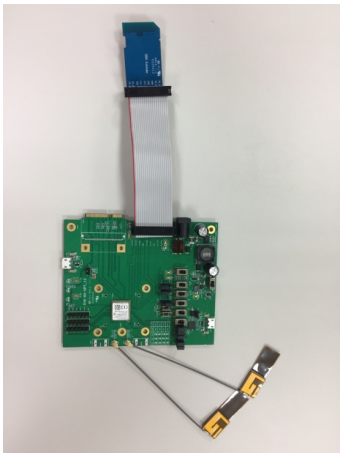
3. Connect the two antennas to the u.FL connectors on the DVK-60-SIPT board.

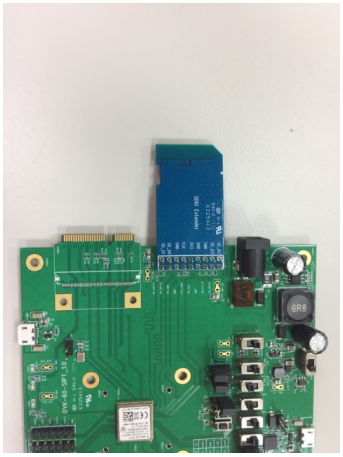


4.2 Environment setup with a SDIO 3.0 host

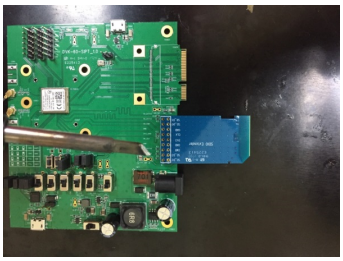
With an SDIO 3.0 host, the Laird module can run in SDR104 mode. Because the SDIO clock is much faster than SDIO 2.0 speeds it is also more sensitive and therefore requires cleaner bus signals.

To wire the DVK-60-SIPT for a SDIO 3.0 host, follow these steps to prevent driver loading failures or crashes due to poor SDIO signaling:

1. Mount the SDIO extender board without pin header on the DVK-60-SIPT SDIO connector. Align the pin closest to the PCIe bus with the SD_D1 pin of SDIO extender board.



2. Solder each pin of the SDIO extender board.



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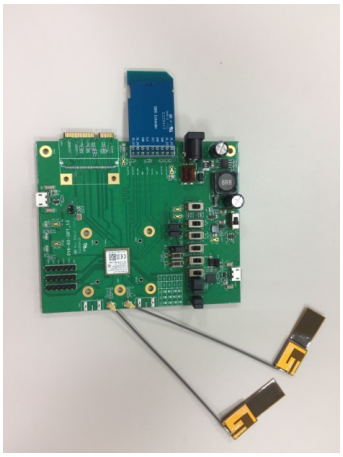
3. Connect the two antennas to the u.FL connectors on the DVK-60-SIPT board.



4.3 Board Switch and Jumper Setings

SDIO 2.0 supports both 1.8V and 3.3V VIO, while SDIO 3.0 only supports 1.8V. In order to properly interact with host SDIO controllers certain jumpers and switches must be set appropriatly.

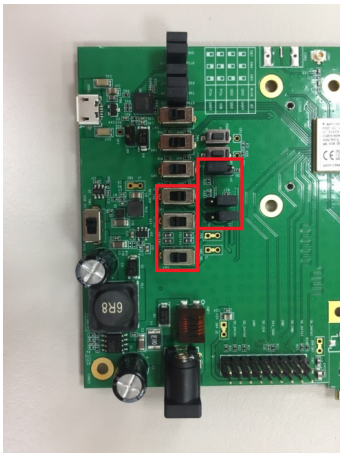
For an overview and block diagram of the DVK-60-SIPT power supply refer to Figure 3 and Figure 4.

And to view the location of the following components, refer to Figure 1.

4.3.1 VIO 3.3V host platform

A VIO 3.3V host platform requires the follwing switch and jumper settings:

- J11: Left (towards USB2)
- J10: Right (towards 60-SIPT Module)
- J9: Right (towards 60-SIPT Module)
- SW4: Right (towards 60-SIPT Module)
- SW2: Left (towards USB2)
- SW3: Left (towards USB2)



4.3.2 VIO 1.8V host platform

A VIO 1.8V host platform requires the following switch and jumper settings:

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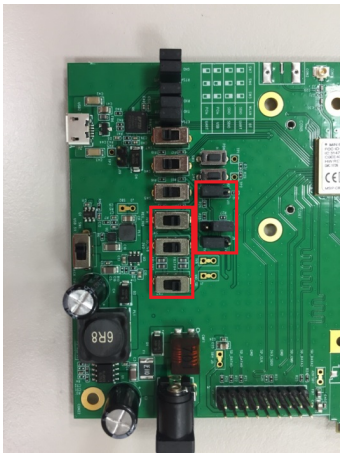
- J11: Left (towards USB2)
- J10: Right (towards 60-SIPT Module)
- J9: Left (towards USB2)
- SW4: Right (towards 60-SIPT Module)
- SW2: Right (towards 60-SIPT Module)
- SW3: Right (towards 60-SIPT Module)



Note: The first released revision of the DVK-60-SIPT developer kit (DVK-60-SIPT_1.0) contains a ***hardware incompatability*** which prevents a 1.8V host platform from properly transitioning to 1.8V. ***To rectify this issue cut solderbridge SB4 located next to J5.***

5 ADDITIONAL DOCUMENTATION

Laird offers a variety of documentation and ancillary information to support our customers through the initial evaluation process and ultimately into mass production. Additional documentation includes:

DVK-SU60-SIPT – User Manual
DVK-SU60-SIPT – Schematics
SU60-SIPT Module – User Manual
SU60-SIPT Module – Hardware Datasheet
SU60-SIPT Module – Integration Guide

For any additional questions or queries, or to receive local technical support for this Development Kit or 60 series modules, please contact wirelessinfo@lairdtech.com

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