LANTRONIX®

PremierWave® 2050
802.11ac Embedded Wi-Fi® IoT Gateway Integration Guide

Intellectual Property

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Disclaimer

This equipment has to be tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

1. Reorient or relocate the receiving antenna.

2. Increase the separation between the equipment and receiver.

3. Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

4. Consult the dealer or an experienced radio/TV technician for help.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This device is intended only for OEM Integrators. The OEM integrator should be aware of the following important considerations.

Labeling of the End Product

The label on the end product incorporating the PremierWave 2050 gateway must clearly state that it contains an FCC-approved RF gateway. Canada and Japan also require a similar statement.

For example, "This product contains RF transmitter ID # (put FCC, IC, CMIIT, and/or Japan gateway grant numbers here)."   The label must include the ID numbers for the regions where the end product is installed. The grant numbers are below.

♦ PremierWave 2050 FCC ID number: R68PW2050

♦ PremierWave 2050 IC ID number: 3867A-PW2050

♦ PremierWave 2050 Japan ID numbers: 201-152843

♦ PremierWave 2050 China SRRC CMIIT ID: 2015AJ6847 (M)

RSS-GEN Sections 7.1.4 and 7.1.5 Statement for Devices with Detachable Antennas

This device has been designed to operate with the antennas listed in the Certificate, and having a maximum gain of 5.5 dBi. Antennas not included in this list or having a gain greater than 5.5 dBi are strictly prohibited for use with this device, unless system level approval is gained. The required antenna impedance is 50 ohms.

To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (EIRP) is not more than that required for successful communication.

Integration Notes

This gateway is authorized under limited gateway approval specific to mobile host equipment. The antenna must be installed with a 20 cm space maintained between the antenna and users.

The transmitter gateway may not be co-located with any other transmitter or antenna.

As long as the two conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end product for any additional compliance requirements required with this gateway installed (for example, digital device emission, PC peripheral requirements, etc.)

In the event that these conditions cannot be met (for example certain laptop configurations, general purpose PCMCIA or similar cards, or co-location with another transmitter) and obtaining a separate FCC authorization will be required, then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product (including the transmitter).

Changes or modifications to this device not explicitly approved by Lantronix will void the user's authority to operate this device.

Note: With the purchase of any PremierWave 2050 family product, the OEM agrees to an OEM firmware license agreement that grants the OEM a non-exclusive, royalty-free firmware license to use and distribute the binary firmware image provided, only to the extent necessary to use the PremierWave 2050 hardware. For further details, please see the PremierWave 2050 OEM firmware license agreement.

Note: Please refer to the PremierWave 2050 802.11ac Embedded Wi-Fi IoT Gateway Datasheet, available at www.lantronix.com/support/documentation, for the full compliance specification and requirements.

Warranty

For details on the Lantronix warranty policy, please go to our Web site at www.lantronix.com/support/warranty.

Revision History

Date	Rev.	Comments
February 2016	A	Initial document.
May 2016	B	Added the "Sample Solder Process Using 5 Mil Stencil" section.
February 2017	C	Updated the DEFAULT#, WAKE and SHDN signal descriptions.
August 2017	D	Updated product label.
January 2019	E	Added the "Integrating Secure Element in Your Designs" section.

For the latest revision of this product document, please check our online documentation at www.lantronix.com/support/documentation.

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1: Introduction

About the Integration Guide

This user guide provides the information needed to integrate the Lantronix® PremierWave® 2050 family of products into customer-printed circuit boards. This manual is intended for engineers responsible for integrating the PremierWave 2050 802.11ac Embedded Wi-Fi® IoT Gateway into their product. This document provides instruction for connecting to the various gateway pin function groups as well as general gateway placement and mounting. For detailed technical and compliance specifications please refer to the *PremierWave 2050 802.11ac Embedded Wi-Fi IoT Gateway Datasheet* available at www.lantronix.com/support/documentation.

The table below describes the integration guide sections.

Table 1-1 PremierWave 2050 Integration Guide Sections

Section	Description
PremierWave 2050 Features	Provides an overview of the gateway functions and mechanical drawing
PremierWave 2050 Block Diagram	Shows the gateway functional blocks
Signal Descriptions	Provides signal descriptions and pinout information
Antenna Interface	Lists the antennas pre-certified for use with the gateway
Antenna Placement	Provides a general recommendation for antenna placement
Using the RF1 Signal Pin	This section is reserved for a future off gateway antenna connection option
Serial Interface	Provides an example on how to connect the unit to external RS232/485/422 networks
Ethernet Interface	Gives an example on how to connect the gateway Ethernet
USB Device Port	Provides an example on how to connect the unit up as a USB device port
USB Host Port	Provides an example on how to connect the gateway USB host ports
LEDs	Describes the gateway LED connections
General Purpose IO Pins	Describes the gateway GPIO connections
Reset Pins	Describes the gateway RESET, DEFAULT, and WAKE pins
Mounting Instructions and PCB Footprint	Provides the gateway PCB footprint and solder profile
Product Information Label	Provides an image and description of the unit label contents
Evaluation Board Schematic	Provides the PremierWave 2050 evaluation board schematic.

Additional Documentation

Visit the Lantronix web site at www.lantronix.com/support/documentation for the latest documentation and the following additional documentation.

Document	Description
PremierWave 2050 802.11ac Embedded Wi-Fi IoT Gateway Datasheet	Provides a unit description and all technical and compliance specifications for the gateway
PremierWave 2050 802.11ac Embedded Wi-Fi IoT Gateway User Guide	Provides information needed to configure, use, and update the PremierWave 2050 firmware.
PremierWave 2050 802.11ac Embedded Wi-Fi IoT Gateway Evaluation Kit Quick Start Guide	Provides the steps for getting the PremierWave 2050 and PremierWave 2050 evaluation kit up and running.
PremierWave 2050 802.11ac Embedded Wi-Fi IoT Gateway Evaluation Kit User Guide	Provides a detailed description of the PremierWave 2050 evaluation kit hardware
Notification Soldering Profile and Washing	Provides guidance in developing a manufacturing assembly process for various Lantronix embedded products.

2: Functional Description

Designed for quick integration with minimal engineering effort, the chip-sized PremierWave 2050 gateway provides simplicity and flexibility making it the easiest and fastest networking-enabling gateway on the market.

PremierWave 2050 gateways are extremely compact networking solutions that enable Ethernet or wireless connectivity on virtually any device with a serial interface. The included industry-proven Lantronix gateway application and full IP stack allow seamless remote access to device data simplifying design integration while providing robust connectivity.

The PremierWave 2050 gateway s can be utilized in designs typically intended for chip solutions. A key difference with the PremierWave 2050 gateway is that there is virtually no need to write a single line of code, translating to a much lower development cost and faster time-to-market.

Table 2-1 PremierWave 2050 Part Numbers

Part Number	Description
PW205010001B	PremierWave 2050, 802.11ac embedded Wi-Fi IoT gateway, dual U.FL, ind. temp, Bulk
PW205020001B	PremierWave 2050, 802.11ac embedded Wi-Fi IoT gateway, chip ant +U.FL, ind. temp, Bulk
PW205010001S	PremierWave 2050, 802.11ac embedded Wi-Fi IoT gateway, dual U.FL, ind. temp, Sample
PW205020001S	PremierWave 2050, 802.11ac embedded Wi-Fi IoT gateway, chip ant + U.FL, ind. temp, Sample
PWGG2051000K	PremierWave 2050 evaluation Kit, 802.11ac embedded Wi-Fi IoT gateway, dual U.FL
PWGG2052000K	PremierWave 2050 evaluation kit, 802.11ac embedded Wi-Fi IoT gateway, chip ant

PremierWave 2050 Features

The PremierWave 2050 gateway is built around a 400 Mhz ARM9 processor with 32 MB of DDR2 DRAM and 128 MB of embedded flash memory. Network connections are provided by a dual band 802.11 ac/b/g/n WLAN radio and 10/100Mbps Ethernet MAC and PHY.

The PremierWave 2050 gateway also supports the following:

♦ 400 Mhz ARM9 CPU

♦ 32 MB DDR2 DRAM

♦ 128 MB NAND Flash

♦ 802.11 ac/bgn wireless with option for on gateway antenna or on gateway U.FL

♦ On gateway 10/100 Mbps Ethernet MAC/PHY. External magnetic and RJ45 required.

- ♦ One USB 2.0 high speed host/device interface.

- ♦ One USB 2.0 high speed host only port

- ♦ One USB 2.0 full speed host only port

- ♦ Two 3.3V serial interface

- ♦ 13 configurable I/O pins

- ♦ Power supply filters

- ♦ Reset circuit

- ♦ Integrated wake up and shutdown for sleep and standby states

- ♦ Interface for connection to an external JTAG software debugger.

- ♦ Dedicated two wire serial port for debug

The PremierWave 2050 gateway requires +5V DC power and is designed to operate in an extended temperature range. (See the *PremierWave 2050 802.11ac Embedded Wi-Fi IoT Gateway Datasheet* available at www.lantronix.com/support/documentation for all technical specifications.)

Figure 2-1 PremierWave 2050 Dimensions and Views
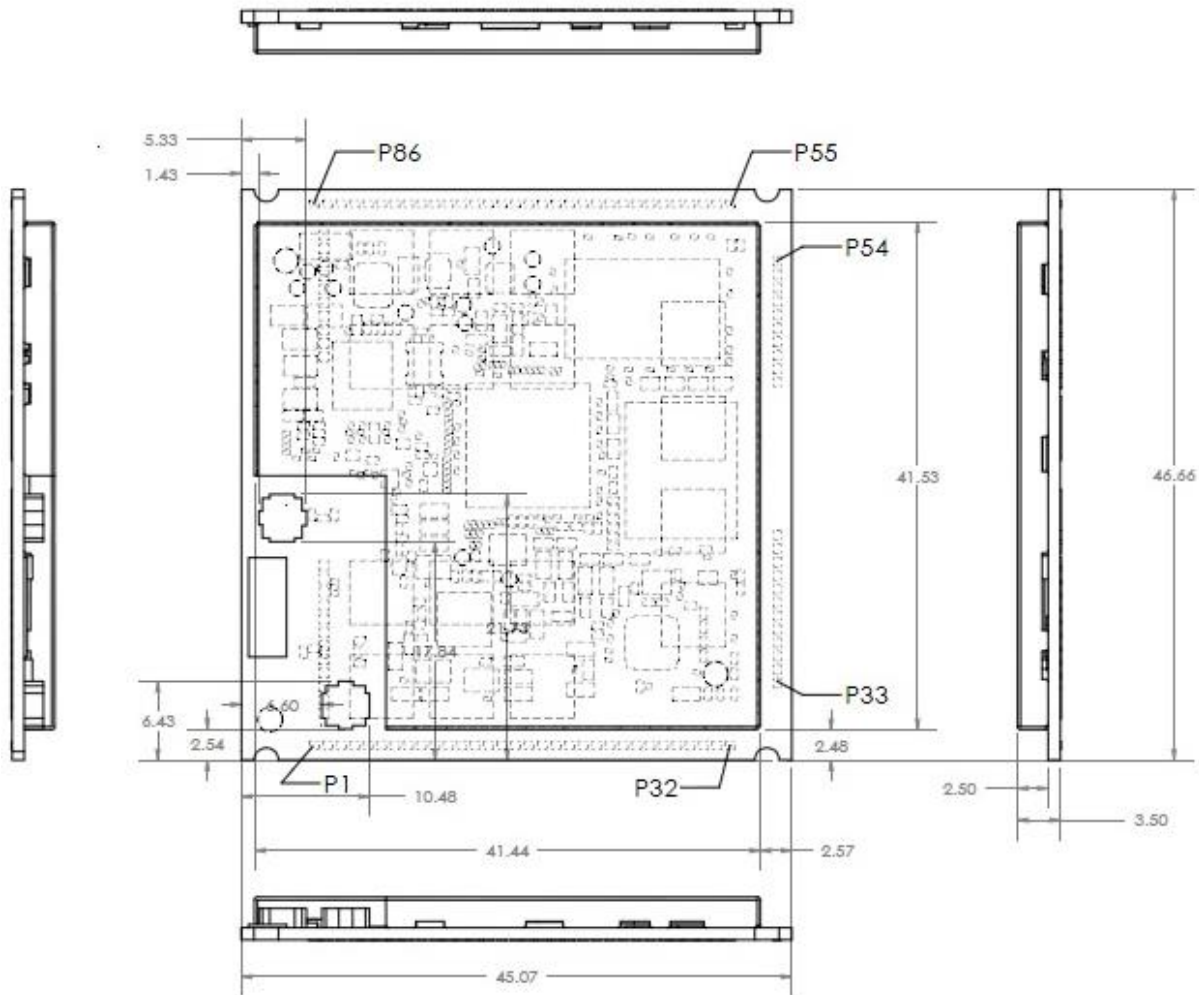
PremierWave 2050 Block Diagram

The following drawing is a block diagram of the PremierWave 2050 gateway showing the relationships of the components.

Figure 2-2 PremierWave 2050 Block Diagram
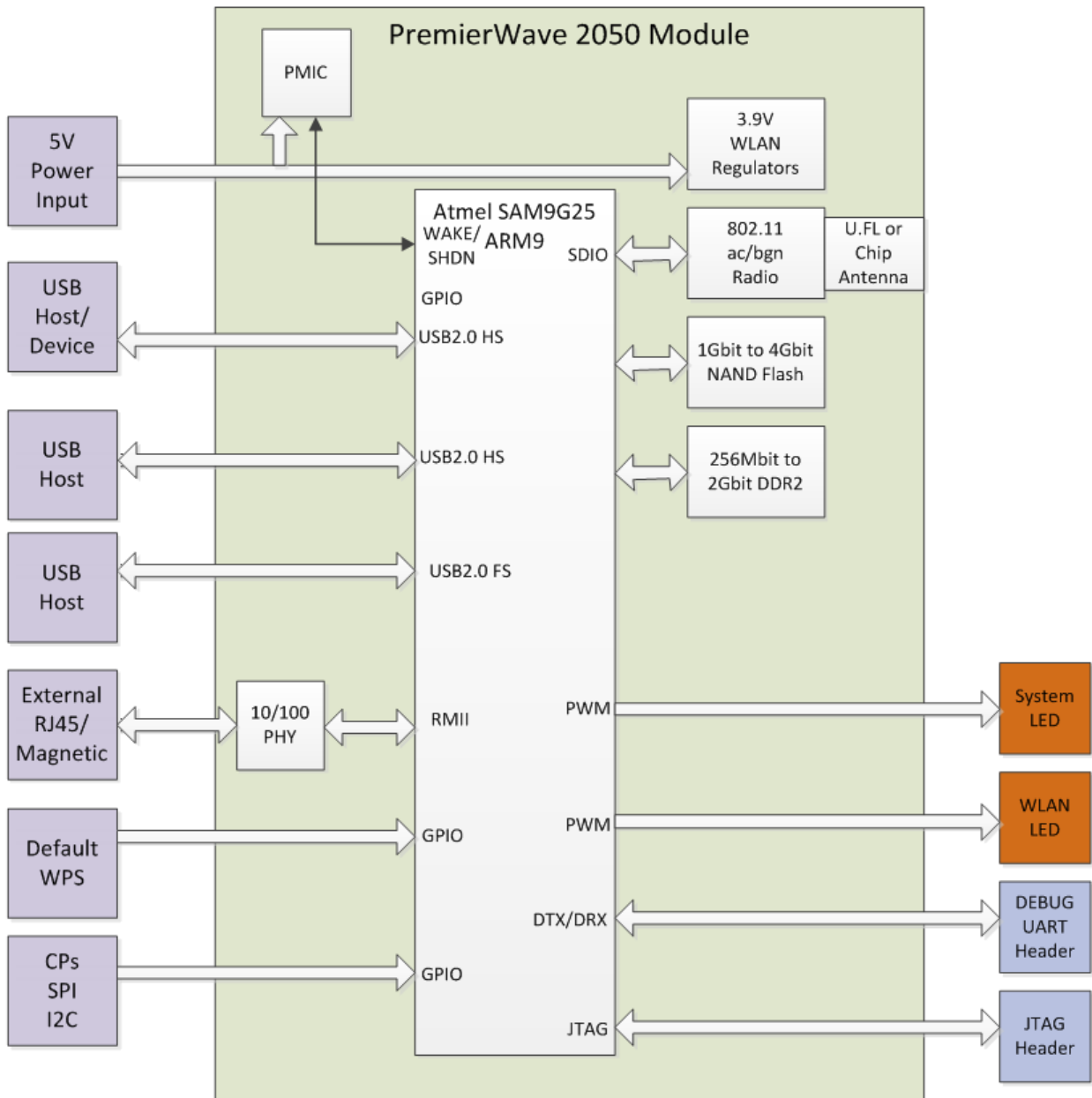
Signal Descriptions

The PremierWave 2050 gateway has a serial interface compatible with data rates up to 921,600 bps. All of the logic IO pins are 3.3V tolerant. The serial signals usually connect to an internal device, such as a UART. For applications requiring an external cable running with RS-232 or RS422/485 voltage levels, the PremierWave 2050 must interface to a serial transceiver chip.

An on-gateway 10/100 Mbps Ethernet MAC and PHY are included on the PW2050 gateway. For connection to an external Ethernet network, external magnetics and an RJ45 are required.

The gateway has options for an on-gateway chip antenna and an external antenna via an on-gateway U.FL connection.

Table 2-2 PremierWave 2050 PCB Interface Signals

Signal Name	PremierWave 2050 Pin #	Primary Function	Reset State	Internal Pull-up /Pull-down	Driver Strength
RF1	2	Reserved for future use. Do not connect			
RF2	4	Reserved for future use. Do not connect			
CP3/MISO	12	Configurable GPIO / SPI master serial data input, SPI slave serial data output			
CP4/MOSI	13	Configurable GPIO / SPI master serial data output, SPI slave serial data input			
CP7/SCK	14	Configurable GPIO / SPI clock			
CP8/CS	15	Configurable GPIO, multiplexed with SPI interface chip select			
CP5	16	Configurable GPIO / I2C data		10K PU	
CP6	17	Configurable GPIO / I2C clock		10K PU	
USB1+/DDP	18	USB (Positive) USB high speed host/device port			
USB1-/DDM	19	USB (Negative) USB high speed host/device port			
USB2+	21	USB (Positive) USB high speed host port			
USB2-	22	USB (Negative) USB high speed host port			
RTS2	24	UART2 serial ready to send output			
CTS2	25	UART2 clear to send input			
CP9	26	Configurable GPIO			
DBTX	27	Debug UART serial transmit data output			

Signal Name	PremierWave 2050 Pin #	Primary Function	Reset State	Internal Pull-up /Pull-down	Driver Strength
DBRX	28	Debug UART serial receive data input		10K PU	
ETXP (ETH1+)	34	Ethernet TX (Positive) Future Gbit pair 1 (pos)			
ETXM (ETH1-)	35	Ethernet TX (Negative) Future Gbit pair 1 (net)			
TXCT (ECT1)_	37	Center tap connection for Ethernet TX pair			
RXCT (ECT2)	38	Center tap connection for Ethernet RX pair			
ERXP (ETH2+)	40	Ethernet RX (Positive) Future Gbit pair 2 (pos)			
ERXM (ETH2-)	41	Ethernet RX (Negative) Future Gbit pair 2 (neg)			
ETH3+	43	Reserved for future Gbit Ethernet pair 3 (Positive)			
ETH3-	44	Reserved for future Gbit Ethernet pair 3 (Negative)			
ETH4+	46	Reserved for future Gbit Ethernet pair 4 (Positive)			
ETH4-	47	Reserved for future Gbit Ethernet pair 4 (Negative)			
ECT3	49	Reserved for future Gbit center tap 3 connection			
ECT4	50	Reserved for future Gbit center tap 4 connection			
USB3+	52	USB (Positive) USB full speed host port			
USB3-	53	USB (Negative) USB full speed host port			
SPEED_LED	56	Ethernet speed LED, active low for 100 Mbps			
CP13	57	Configurable GPIO			
CP12	58	Configurable GPIO			
CP11	59	Configurable GPIO			
CP10	60	Configurable GPIO			
WAKE	65	CPU wake up input. PW2050 gateway wakes from low power state on a rising edge		100K PU	
DEFAULT#	66	Unit reset to default, active low. Drive low for xx seconds to reset unit to default settings.			

Signal Name	PremierWave 2050 Pin #	Primary Function	Reset State	Internal Pull-up /Pull-down	Driver Strength
SYS_LED	67	System status LED, active high			
CP2/INT	68	Configurable GPIO / SPI interrupt external interrupt input			
CP1	71	Configurable GPIO			
LINK_ACT	72	Ethernet link/activity LED active low for link. toggle for activity.			
WLAN LED	73	LED function for WLAN link indication, active low			
RESET#	77	Unit hardware reset, active low. Drive low to reboot unit		35K PU	
RXD2	78	UART2 serial receive data input			
TXD2	79	UART2 serial transmit data output			
CTS1	80	UART1 clear to send input			
RTS1	81	UART1 serial ready to send output			
RXD1	82	UART1 Serial receive data input			
TXD1	83	UART1 serial transmit data output			
SHDN	88	Indicates when gateway is in standby state. Use to power off external devices			
RF1_CTL	97	Reserved for future use. Do not connect			
TRST	100	TRST signal for external debugger			
TDO	101	TDO signal for external debugger			
TDI	104	TDI signal for external debugger			
TCK	105	TCK signal for external debugger			
TMS	106	TMS signal for external debugger			
VCC	29,30,31	5V power input			
GND	1,3,5,20,23,32, 33,36,39,42,45, 48,51,54,55,61, 64,84,86,87,94, 95,96,98,99,102, 103,107,108,109, 110,111,112,113,	Signal ground			

Signal Name	PremierWave 2050 Pin #	Primary Function	Reset State	Internal Pull-up /Pull-down	Driver Strength
	114,115,116,117, 118,119,120,121, 122,123,124				
RSVD	2,4,6,7,8,9,10,11, 43,44,46,47,49,50, 62,63,69,70,74, 75,76,85,89,90, 91,92,93,	Reserved for future use. Leave disconnected.			

Note1: The current the PW2050 gateway supports 10/100 Mbps Ethernet. Additional pins have been called out for a future Gigabit Ethernet gateway.

Note2: The logic IO pins are 3.3V tolerant.

Note3: Pins 109 to 124 are the large ground pads under the the PW2050 gateway. These pads should be connected to ground. These pads also provide thermal relief for the gateway. It is recommended that multiple vias for each pad be used to connect the ground pads to the ground plane.

Figure 2-3 PremierWave 2050 Pin Locations

Note: Pins 109 to 124 are the large pads under the the PW2050 gateway. Pins 109 to 124 should be connected to GND. The pads in yellow are for future gateway revisions and should be left disconnected.
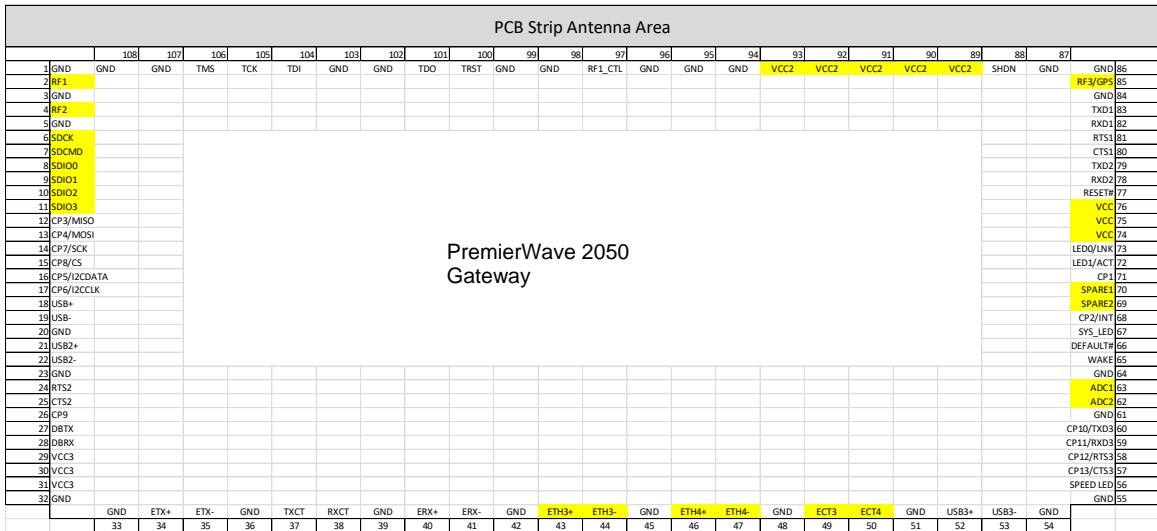
Antenna Interface

The PremierWave 2050 gateway has been certified using the external antennas listed below. Per FCC guidelines, the PremierWave 2050 Wi-Fi certification remains valid if using an antenna of similar type to the antennas below. If using an antenna of similar type to one of the antennas below, but from a different manufacturer part number the antenna gain must be equal to or less than specified in the table. Refer to the *PremierWave 2050 802.11ac Embedded Wi-Fi IoT Gateway Datasheet*, available at www.lantronix.com/support/documentation, for full compliance instructions and information. Consult with your certification lab for more details.
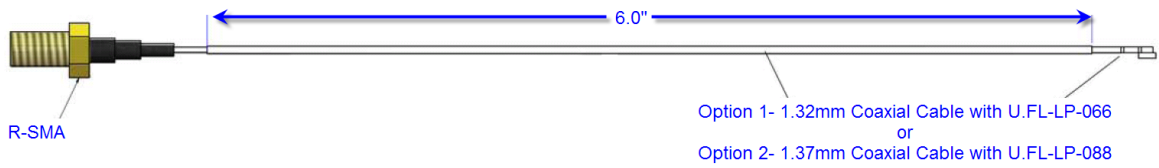
Table 2-3 PremierWave 2050 Wi-Fi On-Gateway Antenna

Antenna Type	Peak Gain Typical	Lantronix Part Number	Vendor	Vendor Part Number	Approved Region
Ceramic Antenna	2.17dBi, 2.4 GHz to 2.5 GHz 2.74 dBi, 4.9 GHz to 5.8 GHz	N/A	N/A	N/A	FCC, IC, EU, AUS/NZS, JPN, China, Mexico

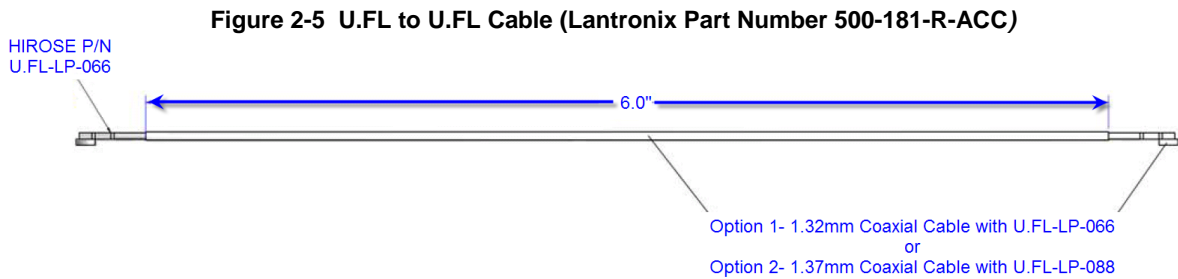*Table 2-4 PremierWave 2050 Wi-Fi External Antenna Options via On-Gateway U.FL*

Antenna Type	Peak Gain Typical	Lantronix Part Number	Vendor	Vendor Part Number	Approved Region
PCB Strip Antenna with 50 mm cable to U.FL connector With tape backing	2.5dBi, 2.39 GHz to 2.49 GHz 5 dBi, 4.9 GHz to 5.9 GHz	XPW100A003-01-B 50 piece bulk pack	Ethertronics®	1001077	FCC, IC, EU, AUS/NZS, JPN, China, Mexico
PCB Strip Antenna with 50 mm cable to U.FL connector Without tape backing	2.5dBi, 2.39 GHz to 2.49 GHz 5dBi, 4.9Ghz to 5.9Ghz		Ethertronics	1000668	FCC, IC, EU, AUS/NZS, JPN, China, Mexico
Swivel type antenna, with RP-SMA(M) connector	2 dBi, 2.4 GHz to 2.5 GHz, 2 dBi, 5.15 GHz to 5.85 GHz	930-033-R-ACC 50 piece bulk pack	Wanshih	WSS002	FCC, IC, EU, AUS/NZS, JPN, China, Mexico
Swivel type antenna, with RP-SMA(M) connector	3.8 dBi, 2.4Ghz to 2.5Ghz, 5.5 dBi, 4.9 GHz to 5.8Ghz		Taoglas	GW.71.5153 (Not for EU use)	FCC, IC, AUS/NZS, JPN, China, Mexico

Note: The PCB strip antenna is available from Ethertronics with or without adhesive tape backing for mounting to a plastic case. The antennas Lantronix supplies include an adhesive backing. For the component without tape backing a non-conductive double sided adhesive tape can be used to fix the antenna in place. The Ethertronics part numbers listed above come with a 50 mm U.FL cable attached to the PCB strip antenna. The 50 mm cable length is the minimum allowed cable length for use with the PremierWave 2050 gateway. For similar PCB strip antennas with longer cables consult with Ethertronics (www.ethertronics.com).

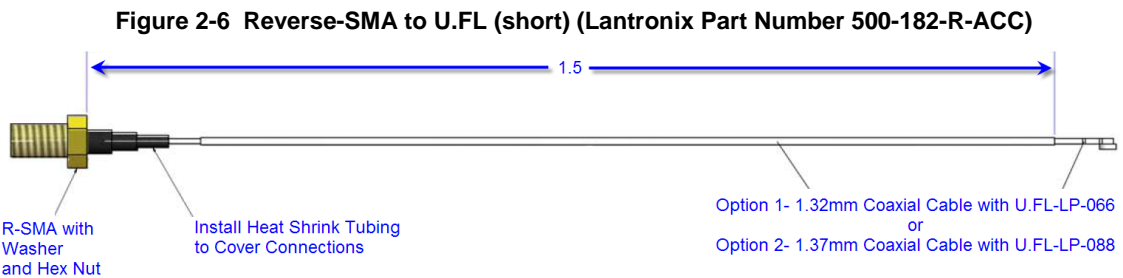Lantronix provides a U.FL to Reverse SMA antenna cable in with the evaluation board and sample kits for development work. These cables can be purchased from Lantronix for production or supplied by an RF cable manufacturer. External antennas can be purchased from an antenna vendor. Components for cable design should be selected for low loss over the entire 2.4 GHz to 5.9 GHz signal range. The cable target impedance should be 50 ohms.

R-SMA

6.0"

Option 1- 1.32mm Coaxial Cable with U.FL-LP-066
or
Option 2- 1.37mm Coaxial Cable with U.FL-LP-088

Figure 2-4 Reverse-SMA to U.FL (Long) (Lantronix Part Number 500-180-R-ACC)

Figure 2-5 U.FL to U.FL Cable (Lantronix Part Number 500-181-R-ACC*)*

HIROSE P/N
U.FL-LP-066

6.0"

Option 1- 1.32mm Coaxial Cable with U.FL-LP-066
or
Option 2- 1.37mm Coaxial Cable with U.FL-LP-088

Figure 2-6 Reverse-SMA to U.FL (short) (Lantronix Part Number 500-182-R-ACC)

1.5

R-SMA with
Washer
and Hex Nut

Install Heat Shrink Tubing
to Cover Connections

Option 1- 1.32mm Coaxial Cable with U.FL-LP-066
or
Option 2- 1.37mm Coaxial Cable with U.FL-LP-088

Antenna Placement

When designing the PremierWave 2050 gateway to a mating board, it is important to consider the final installation of the gateway and its location with respect to connecting access points. The antenna should be placed so that it has as clear as possible path to the connecting access point for maximum range. Avoid placing the antenna such that it is blocked by metal walls or ground planes of adjacent circuit boards.

When using the on board chip antenna it is recommended to place the gateway such that the antenna region is along the edge of the board or extending outward from the edge of the board. The area under the chip antenna region should be voided of all signals and planes

See the figure images below showing recommended placement with the gateway chip antenna.

Figure 2-7 PW2050 Gateway with Chip Antenna Board Edge Mounting
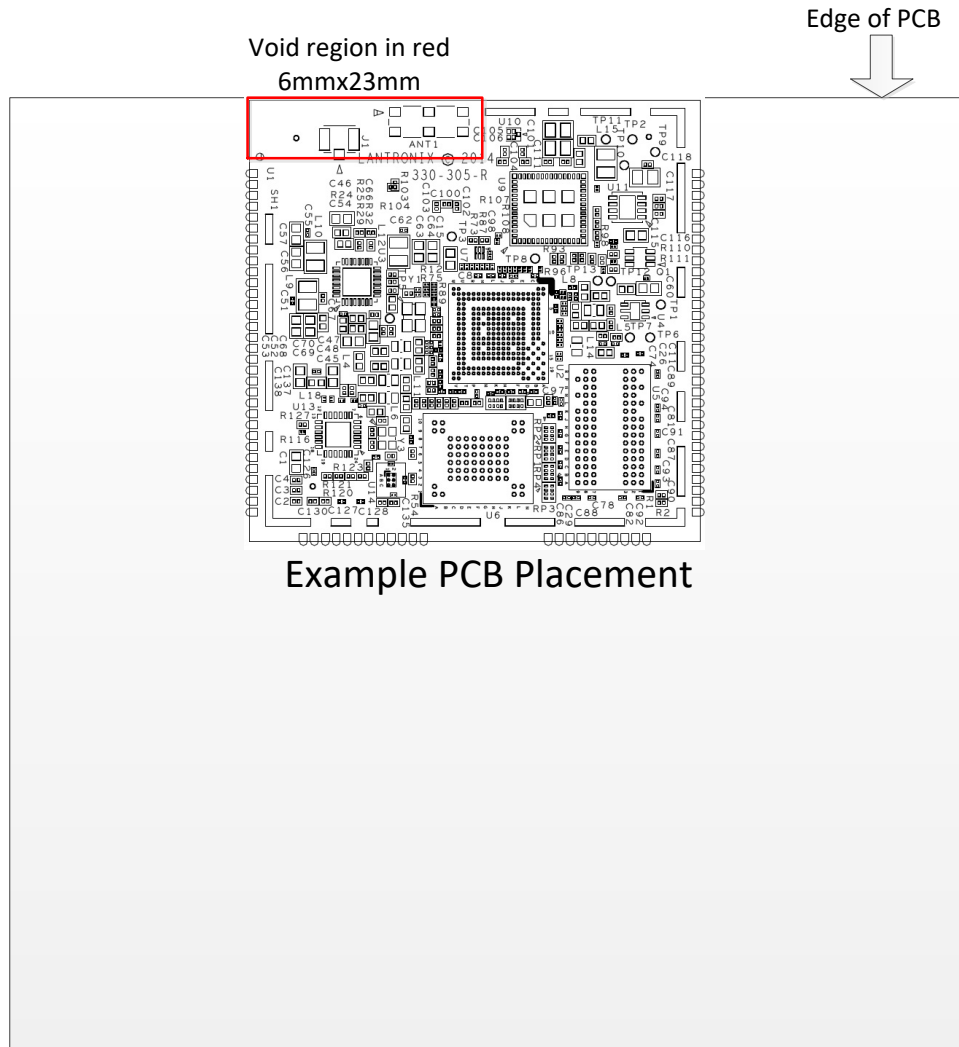
Note: *The chip antenna region of the the PW2050 gateway shown in red above is at the top edge of the PCB. The area in red should be voided to optimize antenna performance.*

Serial Interface

The PremierWave 2050 gateways has two external serial interfaces. The signal levels on the serial interface are 3.3V tolerant. The serial interfaces require an external transceiver in order to connect to external RS232, RS485, or RS422 networks. The signals of the Serial Ports may be connected as shown in the reference schematic below. The transceiver shown in the

reference schematic is of type Exar, part number SP336. This transceiver is a multiprotocol RS232, RS485, RS422 transceiver. Single protocol transceivers may be used as required. The PremierWave 2050 interface may also be directly connected to the UART interface of an external CPU.

Table 2-5 PremierWave 2050 Serial Port Signals

| Signal	Gateway Pin	Description
TXD1	83	Serial transmit data output
RTS1	81	Serial ready-to-send / serial transmit enable output
RXD1	82	Serial receive data input
CTS1	80	Serial clear-to-send input
TXD2	79	Serial transmit data output 2
RTS2	24	Serial ready-to-send / serial transmit enable output
RXD2	78	Serial receive data input 2
CTS2	25	Serial clear-to-send input

Figure 2-8 Serial Port Example
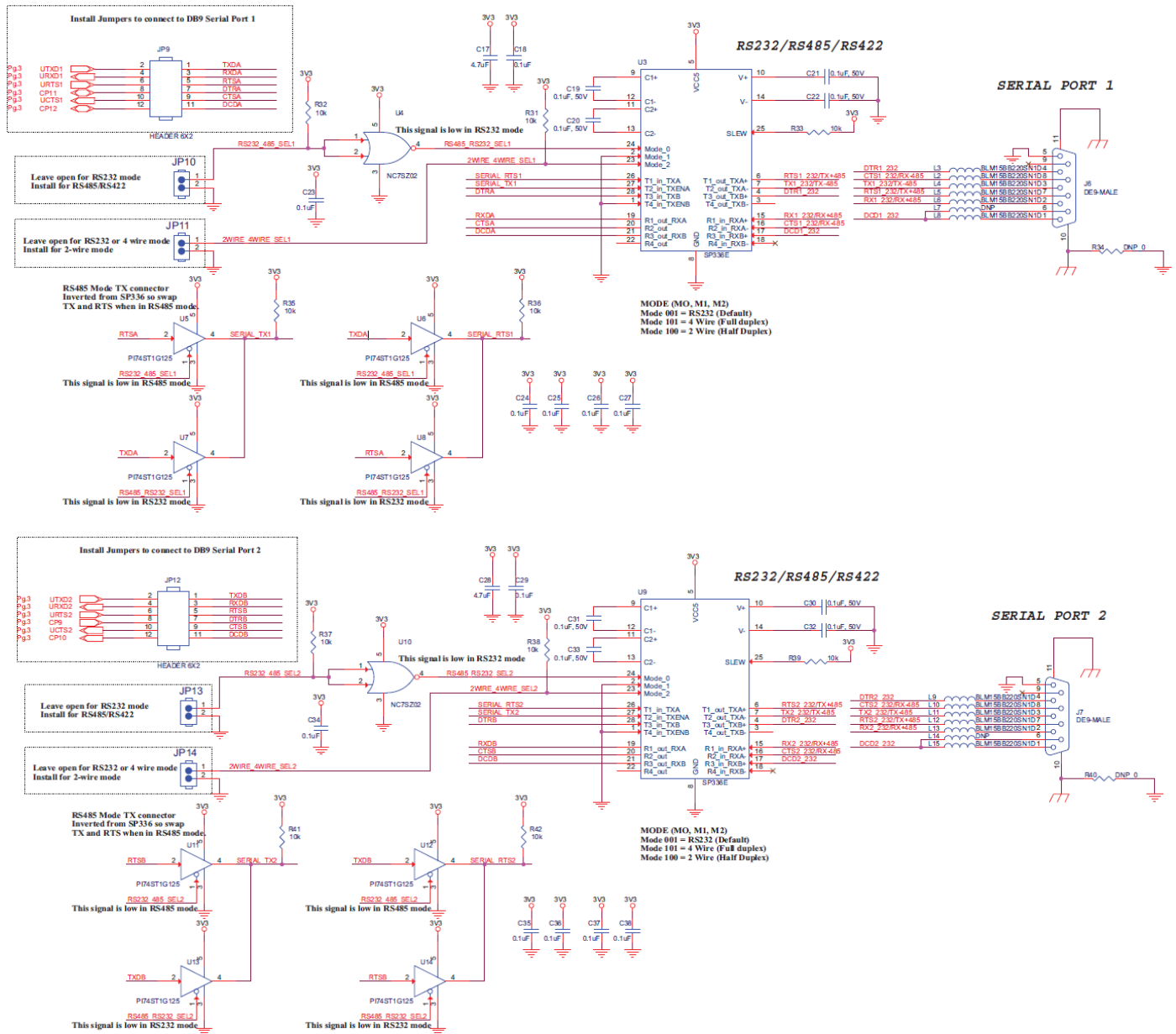
Table 2-6 Example RS232 Connections (Serial Transceiver Required)

PremierWave 2050 Signal		DTE Connector			DCE Connector		
Signal (Logic)	Description	DB9	DB25	Signal	DB9	DB25	Signal
RXDx	Data In	2	3	RXDx	3	2	TXDx
TXDx	Data Out	3	2	TXDx	2	3	RXDx
RTSx	H/W Flow Control Output	7	4	RTSx	8	5	CTSx
CTSx	H/W Flow Control Input	8	5	CTSx	7	4	RTSx
CPx	Modem Control Input	1	8	DCDx	4	20	DTRx
CPy	Modem Control Output	4	20	DTRx	1	8	DCDx

Table 2-7 Example RS422/485 Connections (Serial Transceiver Required)

PremierWave 2050 Signal (logic)	Description	RS485 Signal	DB25 4 Wire	DB25 2 Wire	DB9 4 wire	DB9 2 wire
TXDx	Data Out	TX+485	14	14	7	7
TXDx	Data Out	TX-485	15	15	3	3
RXDx	Data In	RX+485	21	14	2	7
RXDx	Data In	RX-485	22	15	8	3
RTSx	TX Enable					
CPx	RS485 Select					
CPy	RS485 2-wire					

Note: The IO pins for PremierWave 2050 gateway are set to floating input on power up until configured by unit firmware. An external 100K ohm pull-up may be required on the serial transmit signal to prevent downstream UART devices from detecting false characters on initial power up.

Ethernet Interface

The unit provides a 10/100 Mbps Ethernet interface for connection to an external network through external magnetics and an external RJ45. The figure below shows the Ethernet connections to a 10/100 Ethernet RJ45 Jack with Magnetics, J5 in the figure. The RJ45 Magnetic Jack is Belfuse part number 08B0-1D1T-06-F.

The Ethernet differential pair signals, ERXM/ERXP and ETXM/ETXP should be routed as 100-ohm differential pairs on a layer next to the signal ground plane. The use of vias on these signals should be minimized. Center tap signals RXCT and TXCT should be routed with at least 20 mil trace thickness. The area underneath the RJ45 magnetic jack should be void of all signals and planes. The connector shield should be connected to chassis. It is recommended that 1206 resistor pads from chassis ground to signal ground be placed next to each of the shield tabs. The resistor pads allow for 0 ohm jumper, ferrite beads, or decoupling caps to be installed as needed for EMI/EMC improvement.

The Ethernet LED signals should be routed to discrete LEDs or to the LED pins on the RJ45 through 220 ohm or larger resistors. The LED signals are active low.

Also shown in the figure is an optional active choke that can be used to improve ESD, EFT, and EMI/EMC performance in harsh environments. The device is shown as U22 in the figure and is Akros part number AS1602. This device features route through pin assignments allowing for the Ethernet differential signal pairs to be routed without altering the trace impedance or adding vias. Due to this routing the device could be installed or depopulated as needed. Lantronix has performed all certification to FCC Class B without U22 populated.

The Ethernet signals may be left disconnected if unused.

See the Lantronix app note*, How to Connect a Lantronix Embedded Module to a Wired Ethernet Port* for more details on Ethernet connection and routing, http://www.lantronix.com/pdf/appnotes/Connect-LTRX-Embed-Module-to-Wired-Ethernet_AN.pdf.

Table 2-8 Ethernet Port Signals

Pin Name	Description	PremierWave 2050 Pins	Signal Requirement	RJ45 MagJack Belfuse, 08B0-1D1T-06-F Pin assignment
ERXM	Ethernet Receive Negative signal.	41	100 ohm differential pair with ERXP	5
EXRP	Ethernet Receive Positive signal.	40	100 ohm differential pair with ERXM	4
ETXM	Ethernet Transmit Negative signal.	35	100 ohm differential pair with ETXP	3
ETXP	Ethernet Transmit Positive signal.	34	100 ohm differential pair with ETXM	2
RXCT	Center tap for receive pair.	38	Route > 20 mil width	6
TXCT	Center tap for transmit pair	37	Route > 20 mil width	1
Chassis	Unit chassis	-	RJ45 connector shield	Shield tabs
E_LNKACT	Link / activity LED. Active low. Solid for link, blink for activity.	72	Route to LED cathode through 220 ohm or greater.	9
E_SPEED	Link Speed Active low for 100Mbps, Off (high) for 10Mbps.	56	Route to LED cathode through 220 ohm or greater.	7
3V3	3.3 V power	3V3	3.3V power, connect to LED anodes.	8, 10

**Figure 2-9 Ethernet Connections to an External 10/100 RJ45 Magnetic Jack (J5)**
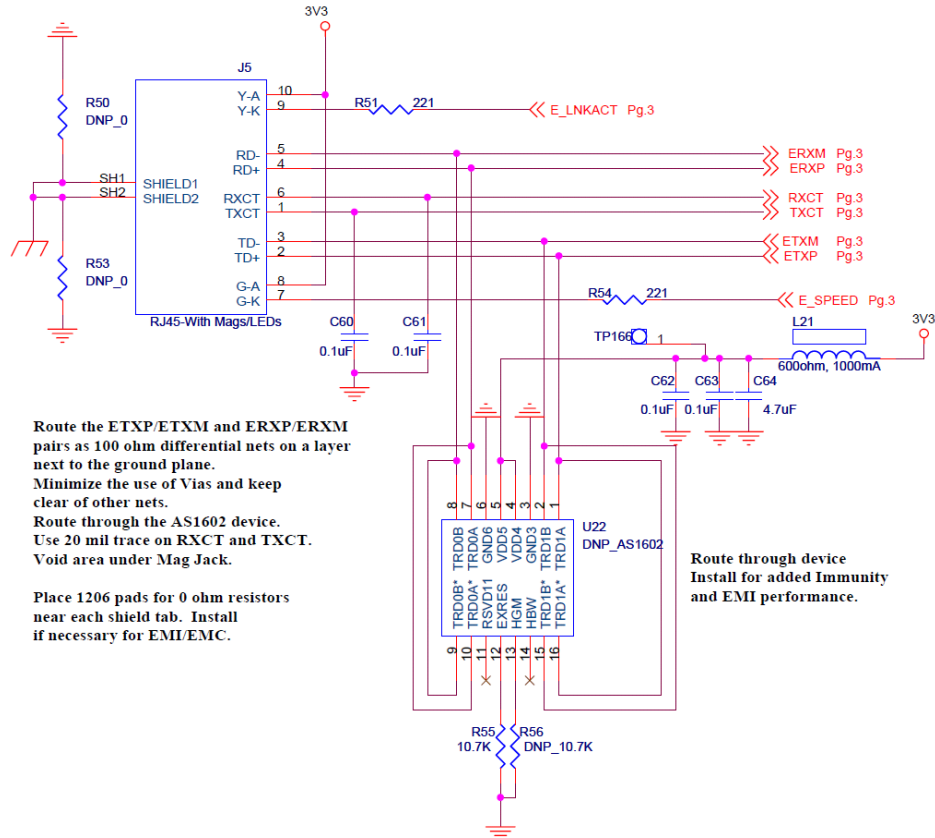
USB Device Port

The PremierWave 2050 gateway has one USB 2.0 device port interface for connection to an upstream USB device. The port consists of a differential pair, signals DDP and DDM. These signals should be routed as a 90 ohm differential pair on a signal layer next to the signal ground plane. The use of vias should be minimized on these signals. The USB signals can be connected to a USB Mini Type B USB port or directly to an IC with a USB host port. If connecting to an external port that is user accessible it is recommended to add a TVS diode array to the signal nets for ESD protection. The ESD array shown in the figure is of type SEMTECH RCIamp0502A. This device features through pin routing to minimize trace impedance changes and simplify routing. The footprint for the TVS array can be added to the PCB and the part can be depopulated if it is not needed. It is recommended that the power drawn off the USB Mini Type B connector be limited to less than 500 mA per USB requirements. If the USB device port is unused the DDP and DDM pins may be left disconnected.

Table 2-9 USB Device Port Signals

Pin Name	Description	Gateway Pins	Signal Requirement	Mini Type B USB Device Connector Pin
USB+/DDP	USB Device Port Positive pin	18	Route as 90 ohm differential pair with DDM signal	3
USB-/DDM	USB Device Port Negative pin	19	Route as 90 ohm differential pair with DDP signal	2
5V	5V power from USB cable		Current limit to 500 mA per port	1
Ground	Signal Ground	Ground	Ground plane	5

*Figure 2-10 USB Device Interface Example (PremierWave 2050 Wi-Fi only)*
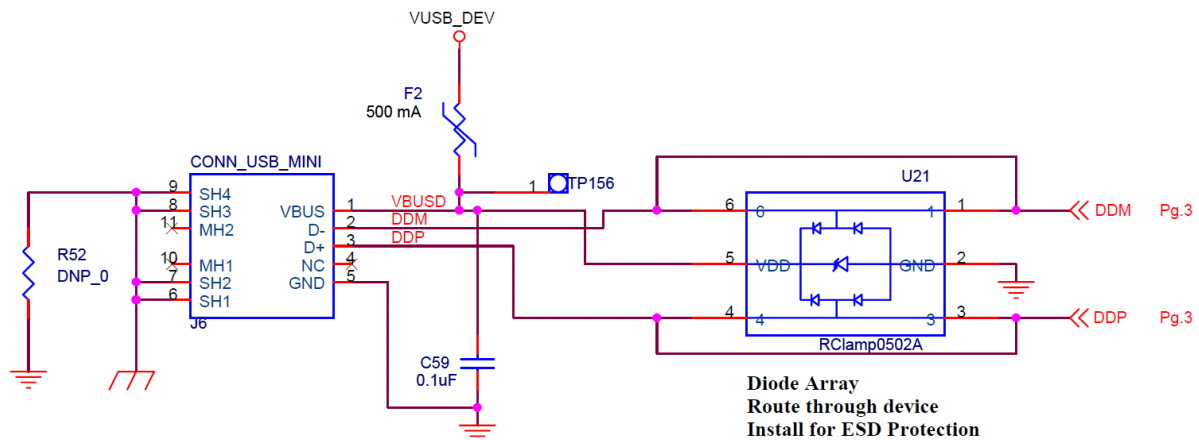
USB Host Port

The PremierWave 2050 gateway has two USB 2.0 host port interfaces for connection to downstream USB devices. Each port consists of a differential pair. Port USB 2 is a high speed port and port USB 3 is a full speed port. These signals should be routed as 90 ohm differential pairs on a signal layer next to the signal ground plane. The use of vias should be minimized on these signals. The USB signals can be connected to a USB type A dual USB port as shown in the figure below or directly to an IC with a USB device port. If connecting to an external port that is user accessible it is recommended to add a TVS diode array to the signal nets for ESD protection. The ESD array shown in the figure is of type NXP, IP4234CZ6. If connecting to an off board device that needs power add a USB power switch to current limit the 5V power connection at the connector. USB requires that each port be limited to 500 mA maximum sustained current. If using the USB host ports the end system must take into account the amount of power consumed by the PremierWave 2050 gateway and each USB device connected to the host ports. The schematic below shows how to connect 5V to a USB host connector using an ST, STMPS2151 power distribution switch. The USB host port 5V power is not provided by the PremierWave 2050 gateway. If the USB host ports are unused their pins may be left disconnected.

Table 2-10 USB Host Port Signals

Pin Name	Description	PremierWave 2050 Pins	Signal Requirement	Type A USB Host connector pin
USB2+/HHSDPB	USB HS Host Port A Positive pin	21	Route as 90 ohm differential pair	B3
USB2-/HHSDPM	USB HS Host Port A Negative pin	22	Route as 90 ohm differential pair	B2
USB3+/HFSDPC	USB FS Host Port B Positive pin	52	Route as 90 ohm differential pair	A3
USB3-/HFSDMC	USB FS Host Port B Negative pin	53	Route as 90 ohm differential pair	A2
5V(User supplied)	5V power for USB connector		Current limit to 500 mA per port	A1, B1
Ground	Signal Ground	Ground	Ground plane	A4, B4

Figure 2-11 USB Host Interface Connections
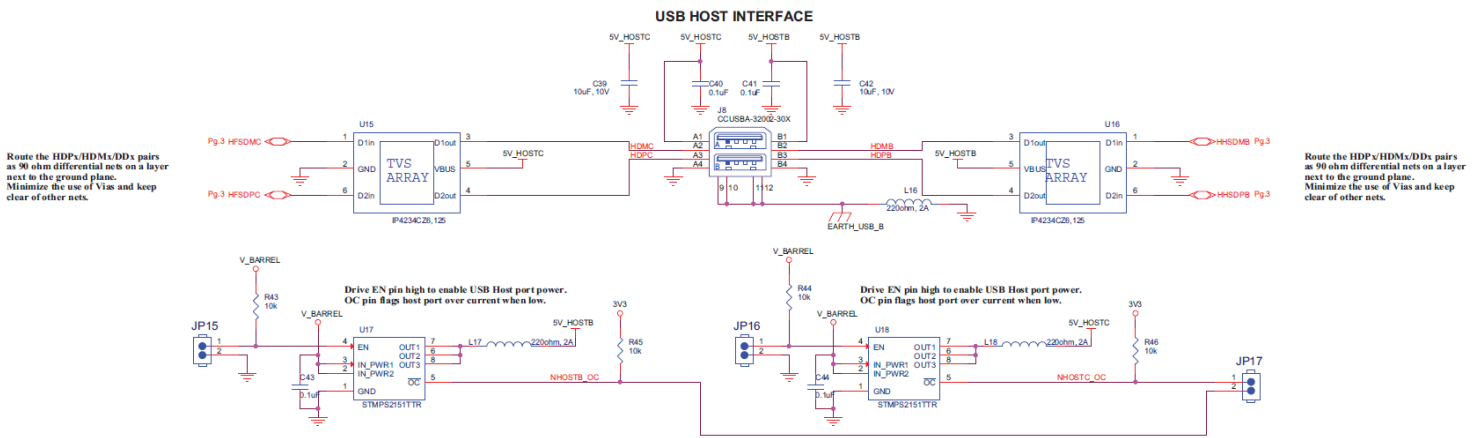
Integrating Secure Element in Your Designs

The PremierWave 2050 module can be connected to an external Microchip ATECC508A Crypto Authentication device for secure boot and secure OTA updates as well as for securely storing keys/credentials for edge applications. The device will connect to the module on the CP5 and CP6 pins as shown in the image below.

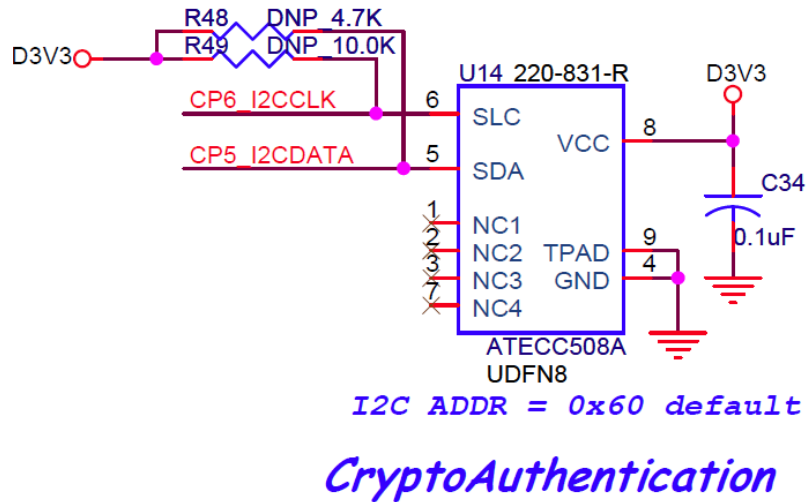**Figure 2-12 External Security Chip Connections**

Table 2-11 I2C Connections to External ATECC508A Device

Pin Name	Description	PW2050 Pin	ATECC508A Pin
CP6_I2CCLK	Configurable pin/ I2C clock	17	6
CP5_I2CDATA	Configurable pin/ I2C data	16	5

Note: Refer to the user guide for details on using the secure boot functions and for enabling access via provided APIs to keys/credentials stored within the Secure Element.

LEDs

The PremierWave 2050 gateway contains several external signals that are intended to drive external status LEDs. The LEDs are listed below. The signals may be connected as shown in the reference schematic figure below.

Table 2-12 PremierWave 2050 Wi-Fi Status LED Output Signals

Signal	Pin	Description
WI-FI LED	73	Wi-Fi Status LED, active low
SYS_LED	67	System status LED, active high
ETH SPEED	56	Ethernet 100Mbps ON (Active low), 10Mbps OFF
ETH LINK/ACT	72	Ethernet link ON (Active low) Ethernet activity Blink (toggle)

General Purpose I/O Pins

PremierWave 2050 gateway contains 13 pins which may be used as configurable inputs or outputs. Listed below are the configurable I/O pins. These pins are 3.3V tolerant.

Table 2-13 Ethernet Interface PremierWave 2050 Serial Port Signals

Signal	Pin	Description PremierWave 2050	Reset State
CP1	71	Configurable I/O	Input
CP2/INT	68	Configurable I/O-SPI interrupt input	Input
CP3	12	Configurable I/O- SPI MISO	Input
CP4	13	Configurable I/O-SPI MOSI	Input
CP5	16	Configurable I/O	Input
CP6	17	Configurable I/O	Input
CP7	14	Configurable I/O-SPI Clock	Input
CP8	15	Configurable I/O-SPI Chip Select	Input
CP9	26	Configurable I/O	Input
CP10	60	Configurable I/O	Input
CP11	59	Configurable I/O	Input
CP12	58	Configurable I/O	Input
CP13	57	Configurable I/O	Input

Reset Pins

PremierWave 2050 gateways have two signals for use as reset signals. Signal EXT_RESET# is a hardware controlled input signal that will reboot the PremierWave 2050 processor when asserted low. Signal DEFAULT# is polled by the PremierWave 2050 software. When DEFAULT# is asserted low for six seconds, the unit will reset the system to the default manufacturing settings and reboot the unit. PremierWave 2050 has an additional signal that can be used to wake up the unit processor when the unit is in a sleep or power down state. The SHDN signal is active when the gateway is in the shutdown state. Use the SHDN signal to gate off external logic when the gateway is in the shutdown state to minimize power

Table 2-14 PremierWave 2050 Reset Signals

Signal	Pin	Description	Reset State
EXT_RESET#	77	Unit hardware reset, active low. Drive low for 50ms to reboot unit. Signal should be driven high or left floating after reset.	Input
DEFAULT#	66	Unit reset to default, active low. Drive low for 6 seconds or longer to reset unit to default settings.	Input
WAKE	65	CPU wake up input. The PW2050 gateway wakes from low power state on a rising edge. Refer to user guide for WAKE pin configuration options.	Input

SHDN	88	Indicates when the gateway is in Standby state. Use to power off external devices. See evaluation board schematic for recommended connections.	

Figure 2-13 Recommended Use of SHDN Signal to Shut Off External Power Rail
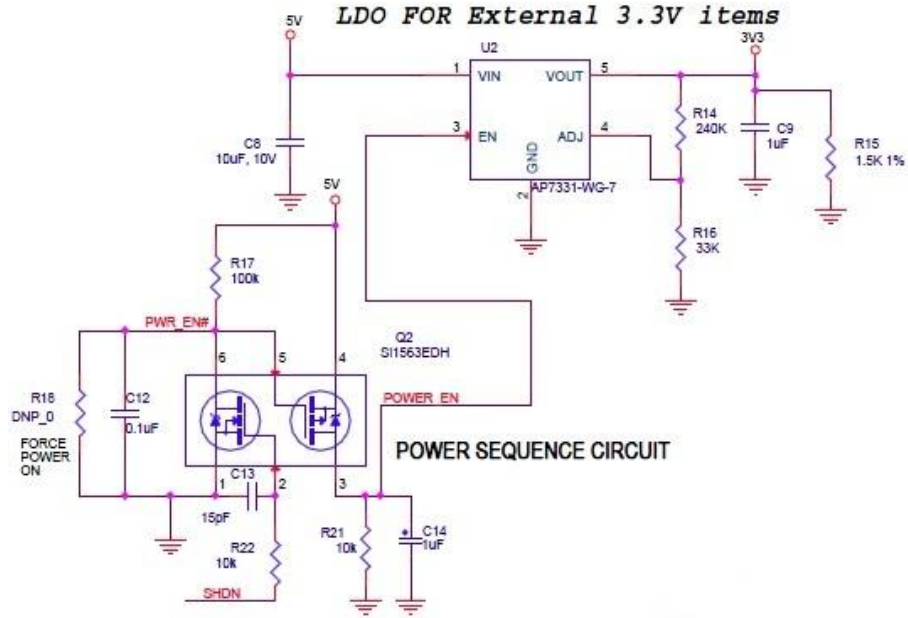
3: PCB Footprint and the PW2050 Dimensions

The gateway recommended footprint is shown below. The antenna region should ideally be placed on the edge of the board. The area under the antenna region should be void of all signals and planes. The antenna location inside of the end unit and installation should be chosen such that the antenna has as clear as possible line of site to the connecting WLAN devices. The antenna path should be as clear as possible from metal, ground and power planes from adjacent PCBs and other objects that can interfere with the signal path to the connecting WLAN devices.

Access CAD Files

1. Go to http://www.lantronix.com/products/cad-visio.html.

2. Click **Download CAD files here** to access the **Registration Form**.

Figure 3-1 PremierWave 2050 Gateway Dimensions
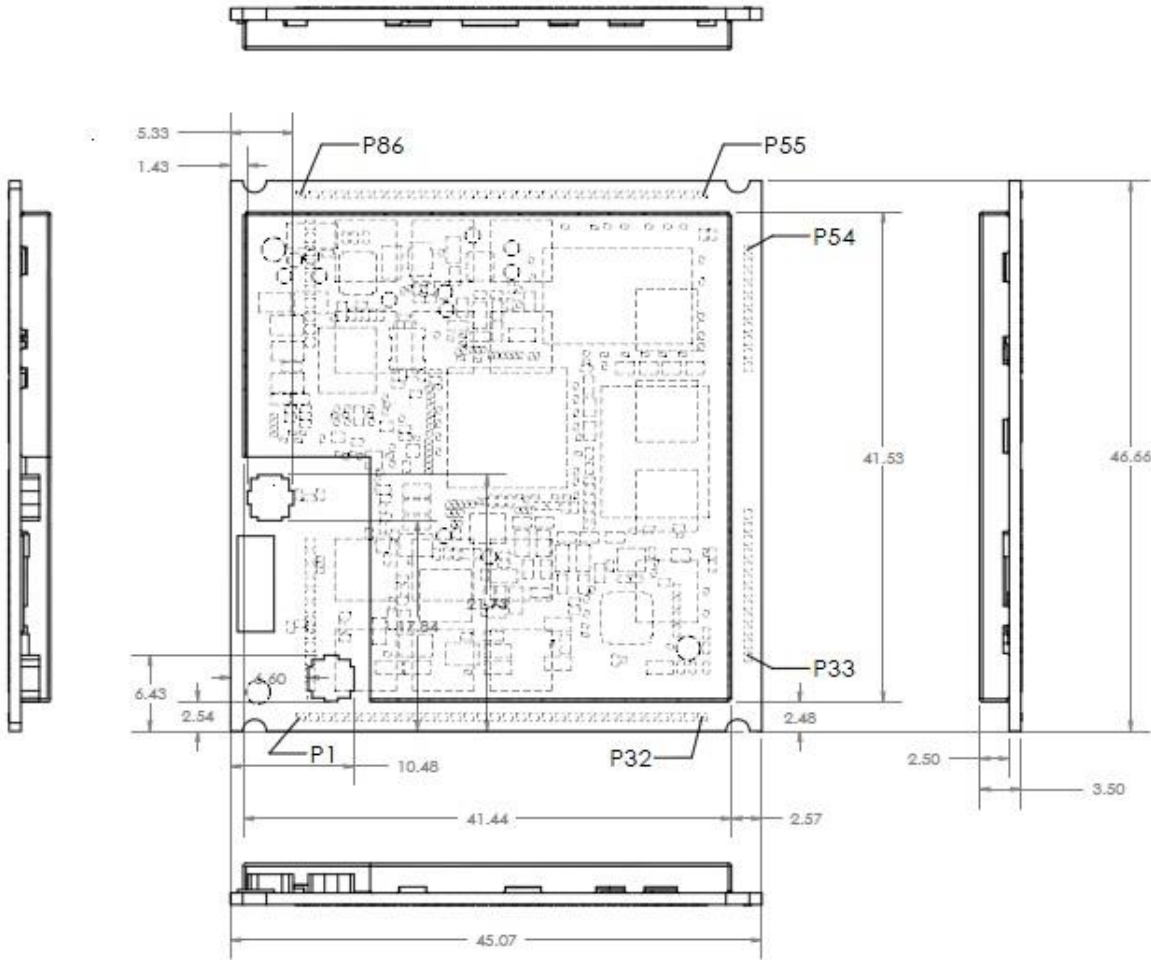
Figure 3-2 PremierWave 2050 Recommended Footprint
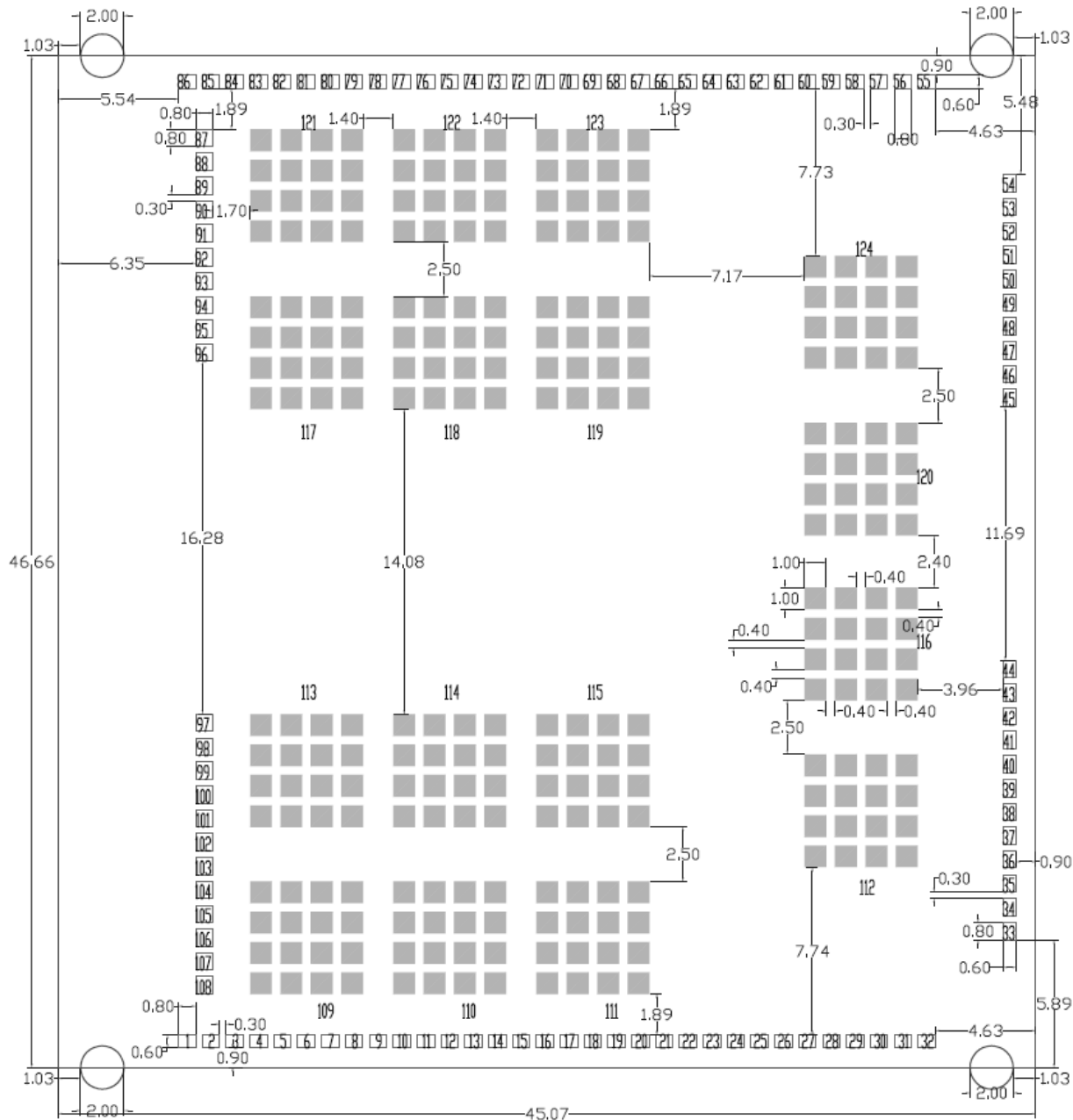
Module Top View(Unit=mm)

The pads on the PremierWave 2050 gateway are pre-bumped with solder. Lantronix recommends using non-solder-mask defined pads (NSMD). Lantronix recommends using ENIG finish for the PremierWave 2050 gateway pads.

The internal ground pads are used for gateway signal ground and thermal relief. The outer layers should be flooded with ground and the ground pads should have many vias to the internal ground layers.

Soldering coverage should be maximized and checked via x-ray for proper design. There is a trade-off between providing enough soldering for conductivity and applying too much, which allows the gateway to "float" on the pads creating reliability issues. Lantronix recommends 80% or more full contact solder coverage on each of the internal ground pads after reflow.

Note: *The recommended stencil thickness is 4-5 mil. The stencil aperture should not exceed the size of the pad. Solder volume must be controlled. It is recommended that the aperture be set to 1:0.8 of the pad size. For example, the 0.8x0.6 mm pad would use a 0.64x0.48 mm stencil. Thicker stencils will require further reduction in stencil aperture. First article and routine inspection of the printing quality is necessary to ensure high yield. At a minimum, visually inspect the unit utilizing a magnifier with 10x magnification; otherwise inspection with a solder paste inspection (SPI) machine is preferred. Lantronix recommends a final standoff height after reflow of 75 to 100 um.*

Reflow Profile Guideline

The reflow profile is dependent on many factors including flux selection, solder composition, and the capability of the user's reflow equipment.

Lantronix does not recommend a specific reflow profile but provides the following general guidelines:

♦ The solder composition typically sets the peak temperatures of the profile.

♦ Lantronix recommends lead free solder pastes SAC305: Type 4. Water soluble or no-clean solder pastes are acceptable.

♦ Reflow equipment is needed at nine heater zones at minimum. Lantronix recommends a forced air type reflow oven with nitrogen.

♦ Lantronix recommends that the peak temperature at the solder joint be within 235°C ~ 245°C, and the maximum component temperature should not exceed 260°C.

♦ Lantronix recommends that the solder joint heating time above 217°C last between 40-90 seconds, and at a minimum of 40 seconds.

♦ Excessive ramp/cooling rates (>3°C/s) should be avoided.

♦ To develop the reflow profile, Lantronix recommends that the user place thermocouples at various locations on the assembly to confirm that all locations meet the profile requirements. The critical locations are the gateway solder joints.

♦ When developing the reflow profile, Lantronix recommends that a fully loaded assembly be used to assure that the total thermal mass is accounted for.

Figure 3-3 Recommended Reflow Profile
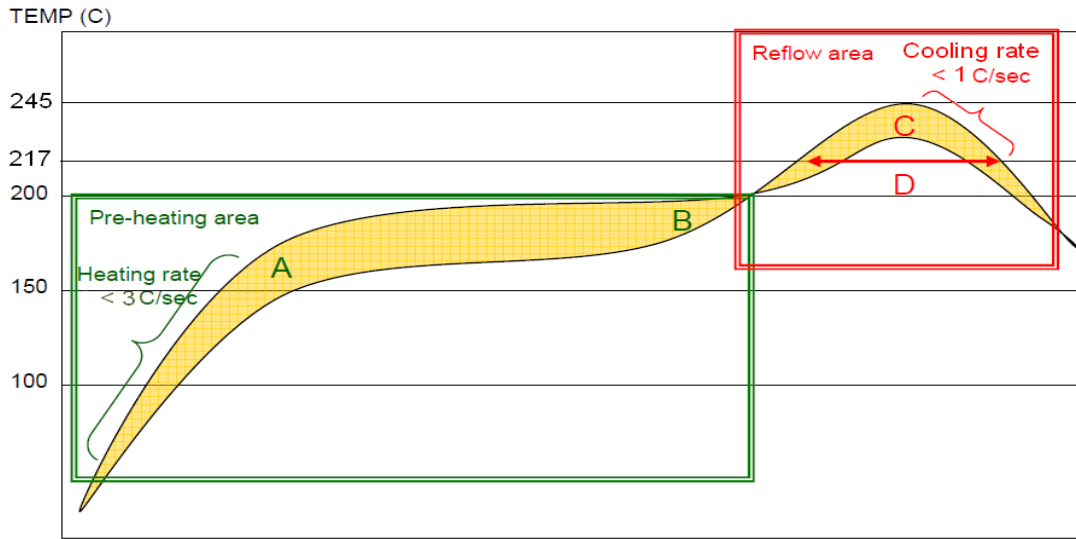
(1) Solder paste alloy: SAC305(Sn96.5/Ag3.0/Cu0.5)(Lead free solder paste is recommended by Lantronix.)
(2) A-B. Temp.(Pre-heat): 150~200 °C; soak time:60~120 seconds.
(3) C. Peak temp: <245 °C
(4) D. Time above 217 °C: 40~90 sec.
(5) Suggested optimal cooling rate is <1 °C /sec. from peak to 217 °C.
(6) Utilize a minimum of nine heater zones for Reflow equipment.
(7) Nitrogen usage is recommended when the oxygen concentration is controlled at less than 1500 ppm.

Note: *Need to inspect solder joint by X-ray post reflow for voiding and solder shorts.*

Sample Solder Process Using 5 Mil Stencil

1. Introduction

This application note provides a general guideline for assembling a PremierWave 2050 gateway on a reference PCB.

2. Scope

Contains generic information for PremierWave 2050 packages assembled internally. An actual experiment on a larger sample size is required to optimize the assembly process.

3. Assembly Process

Due to package layout and dimension, standard pick and place process is highly recommended. Manual soldering should be avoided.

Figure 3-4 SMT Process Flow
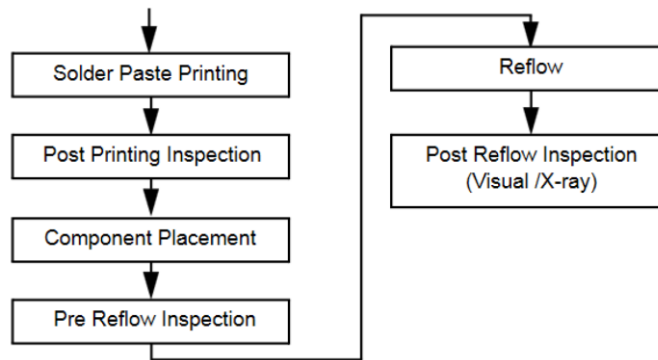
4. Solder Paste and Stencil Design

Senju SAC305 Type 4 No-Clean was used in this experiment.

Aperture for the PremierWave 2050 gateway was opened 25 mil x 23 mil for rectangle pads and 25 mil x 31 mil for square pads.

Thickness of stencil: 5 mil

5. Solder Paste Printing

Solder paste printing was done with the following parameters:

- Printing speed forward/backward: 10 mm/s
- Printing Pressure forward/backward: 25 N
- Snap off: -0.50 mm
- Separation speed: 1.0 mm/s

The expected volume of solder paste for Rectangle pads per stencil design:
25 mil x 23 x 5 mil = 2875 mil^3

Inspection result from SPI for Rectangle pad: 2876.5 mil^3

Figure 3-5 SPI Rectangle Pad 2876.5 mm Inspection Result
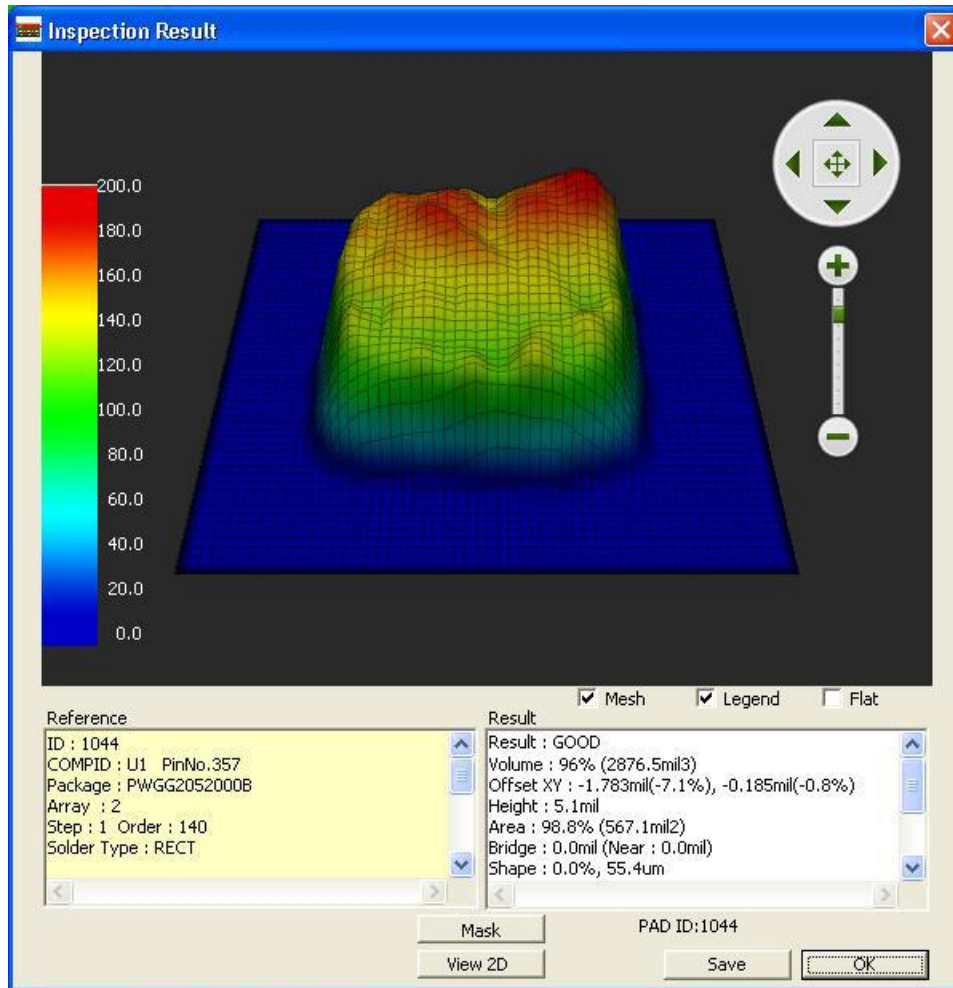
The expected volume of solder paste for Square pads per stencil design:
25 mil x 31 x 5 mil = 3875 mil^3

Inspection result from SPI for Square pads: 3850.7 mil^3

Figure 3-6 SPI Square Pad 3850.7 mm Inspection Result
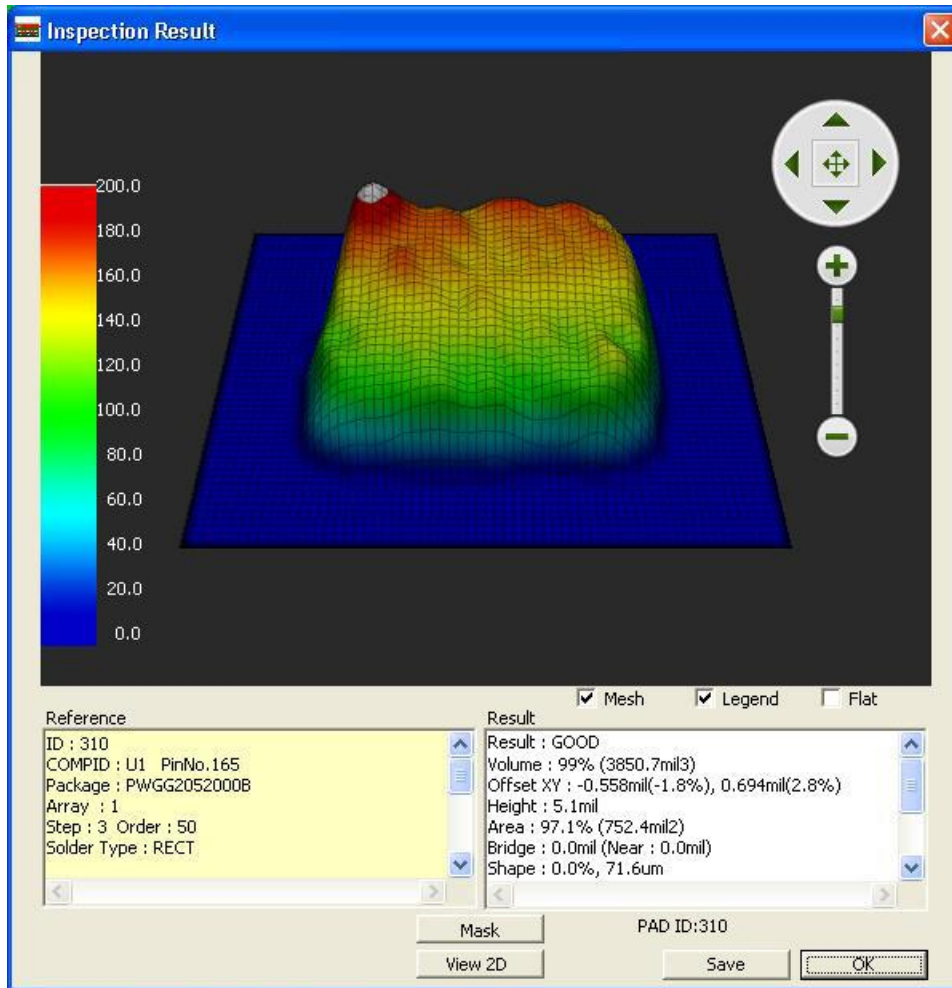
6. Component placement

The component must be programmed correctly for pick and place machine to ensure the vision system is able to inspect all the pads before placement. Placement accuracy plays an important role to get success on installing the gateway on this assembly.

Placement speed: Should be at a slowest speed possible to avoid rotation when spindle is traveling.

Placement force: 150 grams.

7. Pre-Reflow Inspection

Inspection after placement under X-Ray machine

The result shows that the placement is accurate and ready for reflow.

Figure 3-7 X-Ray Machine Pre-Reflow Inspection
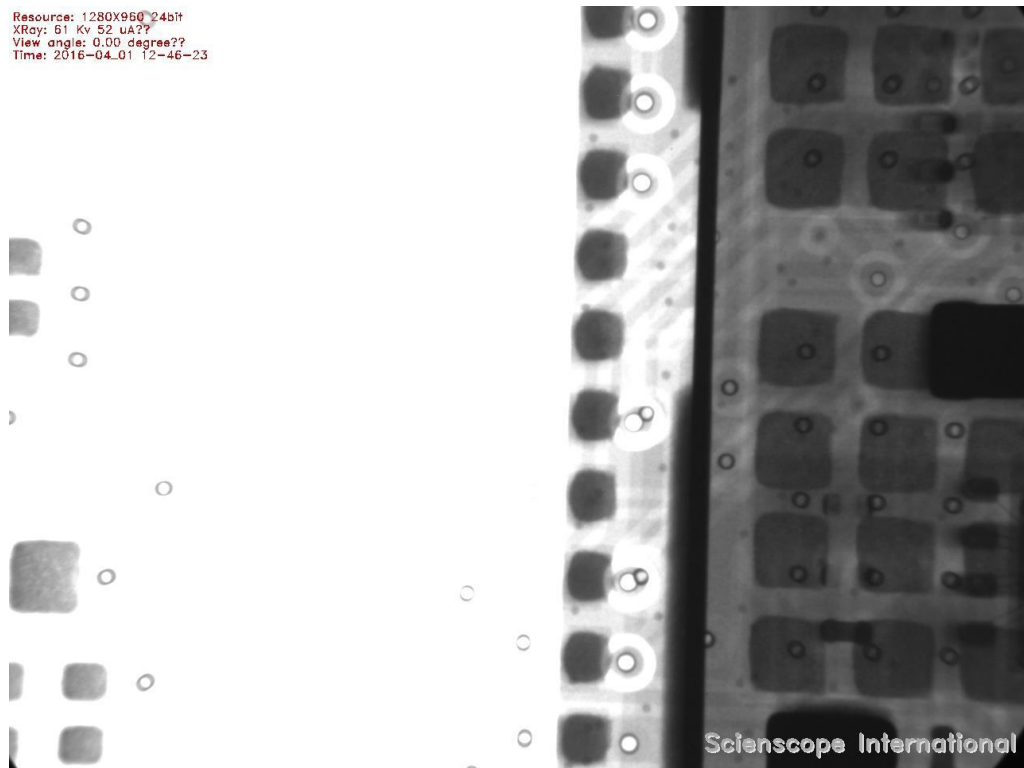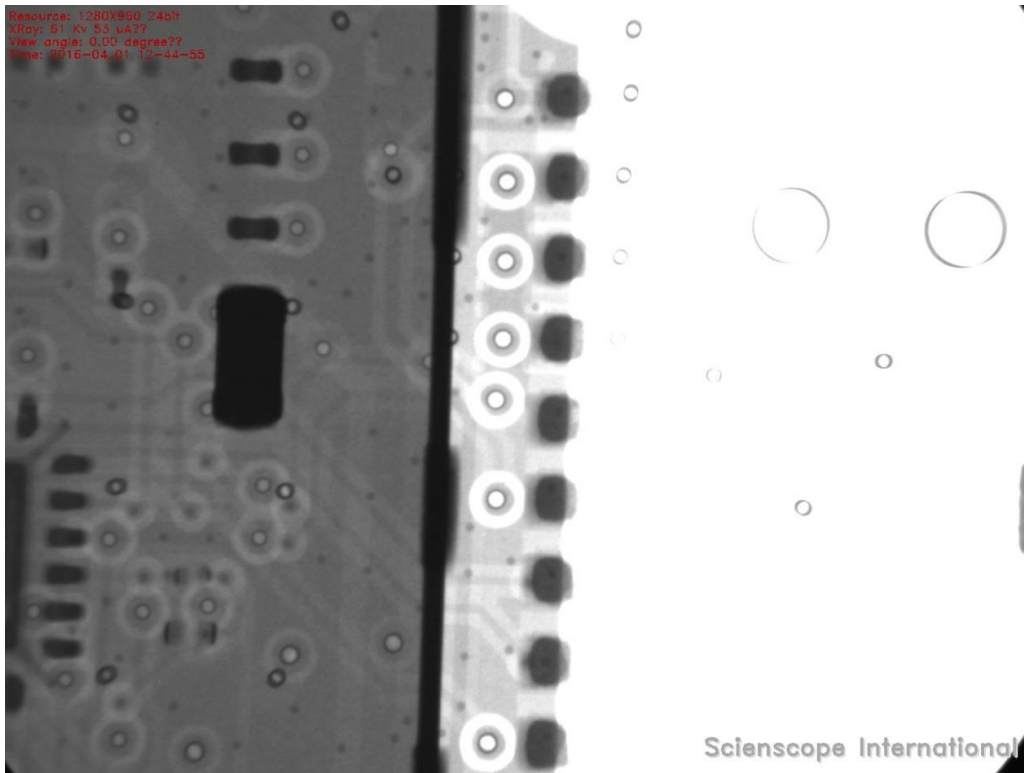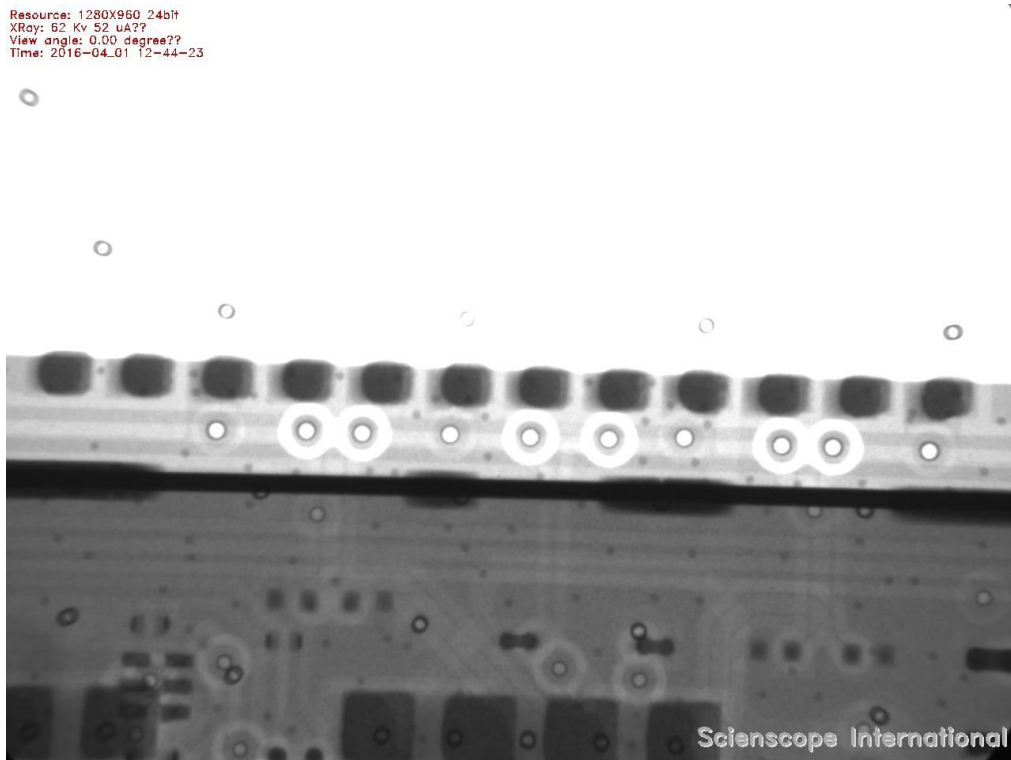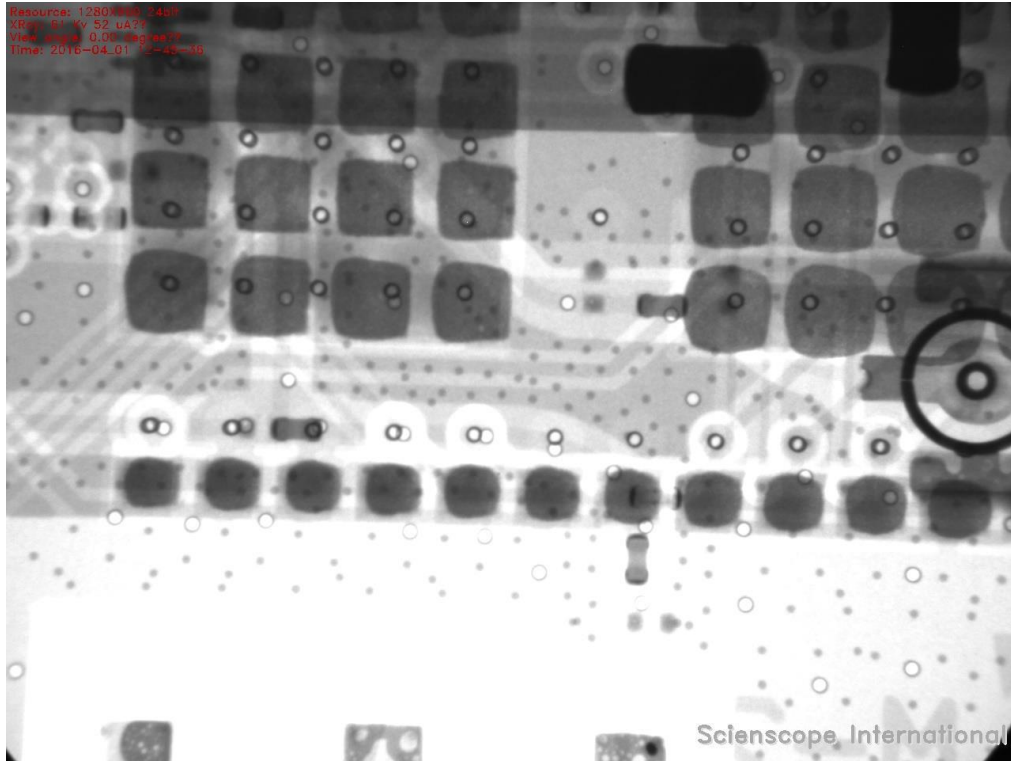
8. Reflow

Table 3-1 Oven Setting

	Zone 1	Zone2	Zone 3	Zone 4	Zone 5	Zone 6	Zone 7	Zone8
Top	140	155	165	175	190	250	265	265
Bottom	140	155	165	175	190	250	265	265

Belt Speed: 24 in/min

9. Post Reflow Inspection

X-Ray results show a very normal and standard solder fill and voiding is acceptable per IPC-A-610 class 2.

Figure 3-8 X-Ray Machine Post Reflow Inspection
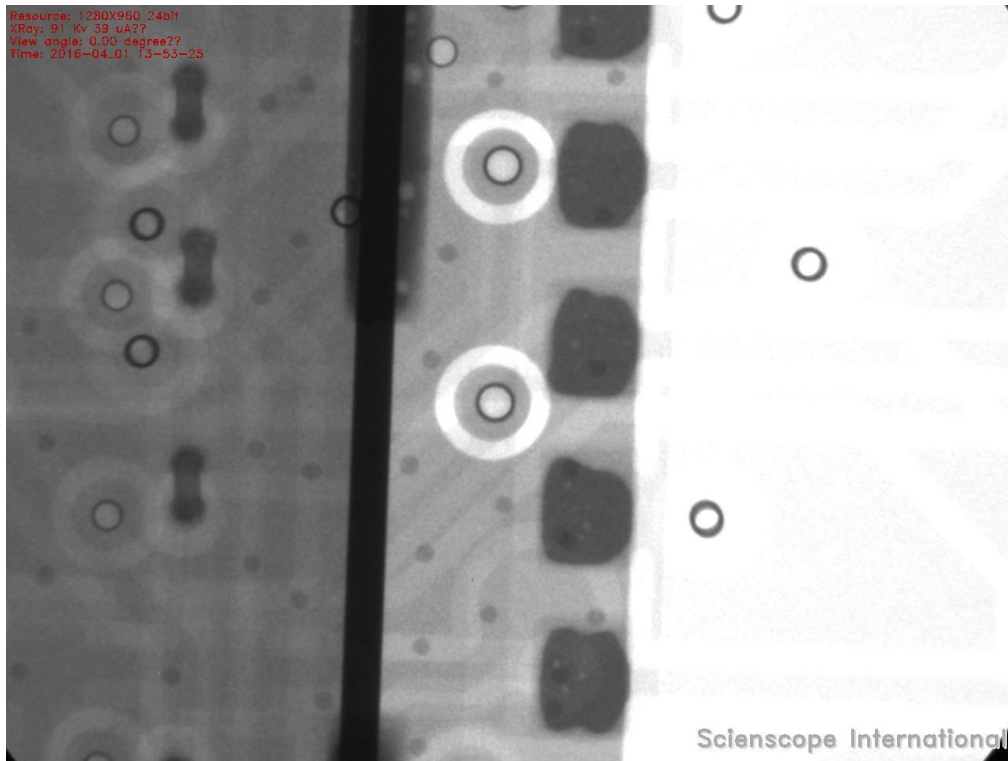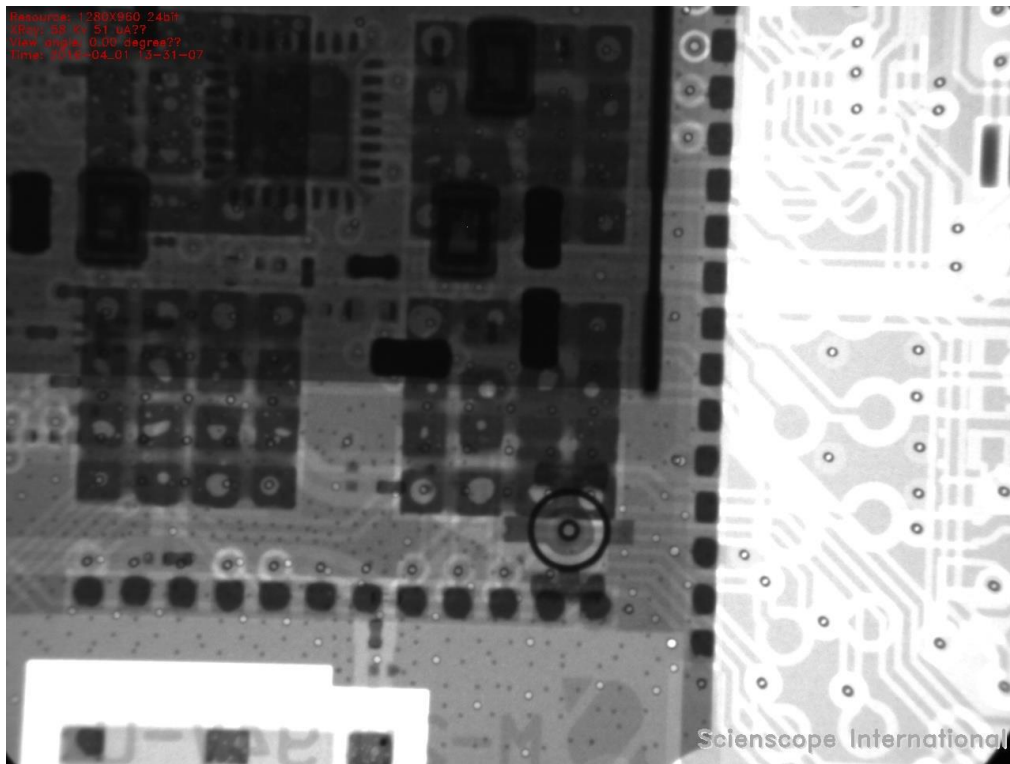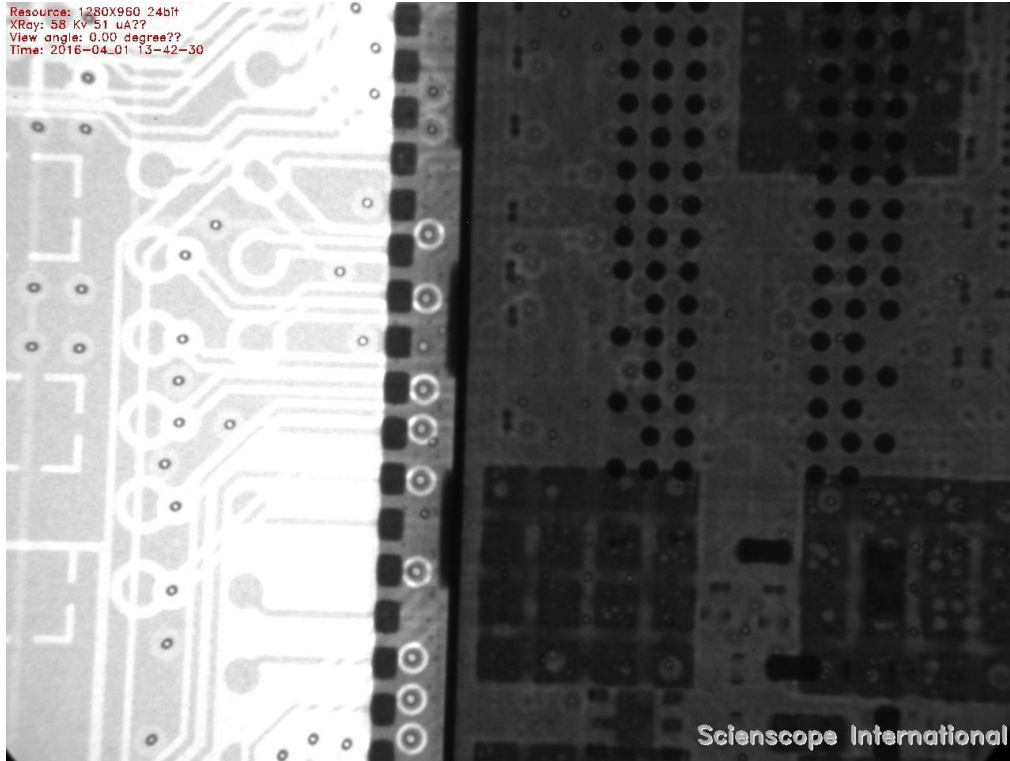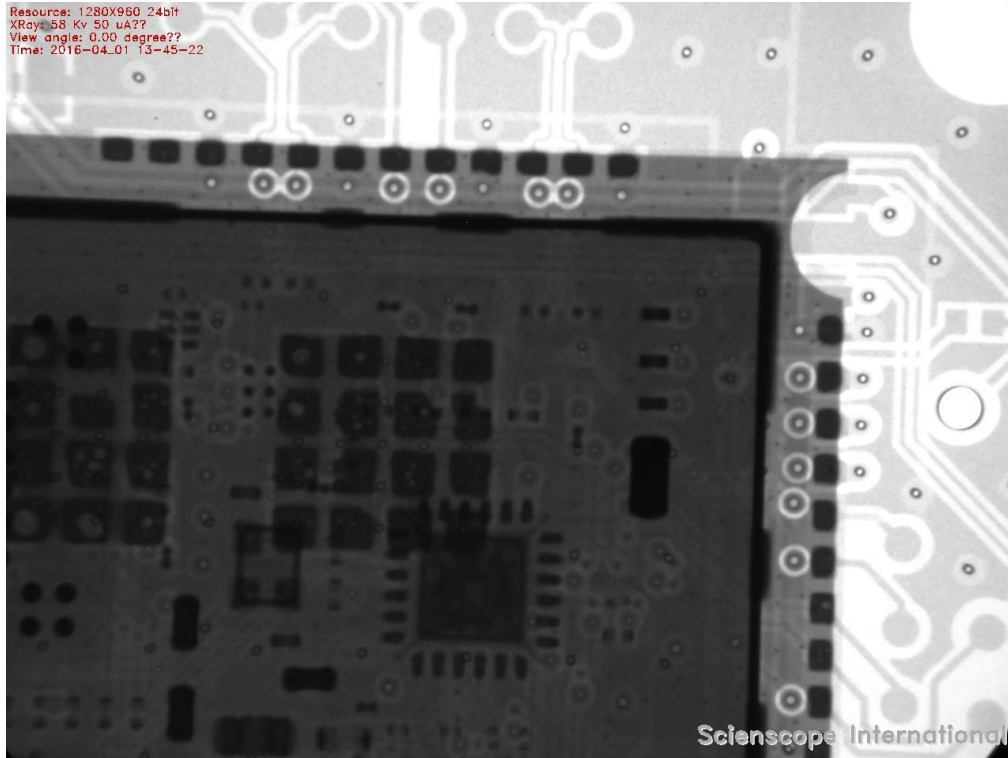
MSD (Moisture Sensitive Device) Control for the PW2050 Gateway

1. The PremierWave 2050 gateway is a moisture sensitive device; the MSL level is 3.

2. Gateways to be subjected to reflow solder or other high temperature processes must be mounted within 168 hours of opening the vacuum containment bag in factory conditions.

3. The gateway requires baking before mounting, if:

    a. The Humidity Indicator Card reads >10% when read at 23± 5°C

    b. The MSL3 are not met

4. If baking is required, optional condition as below (refer to IPC/JEDEC J-STD-033):

    a. Bake 9 hours @ 125°C (Tray base)

    b. Bake 33 hours @ 90°C/≦5%RH (Tray base)

    c. Bake 13 days @ 40°C/ ≦5%RH (Tape/Reel base)

    Note: After baking, the floor time of gateway should be recalculated.

Product Information Label

The product information label contains important information about your specific unit, such as its part number, revision, manufacturing date code, product model, country of origin, datamatrix barcode and MAC address.

Figure 3-9 PremierWave 2050 Product Label

Evaluation Board Schematic
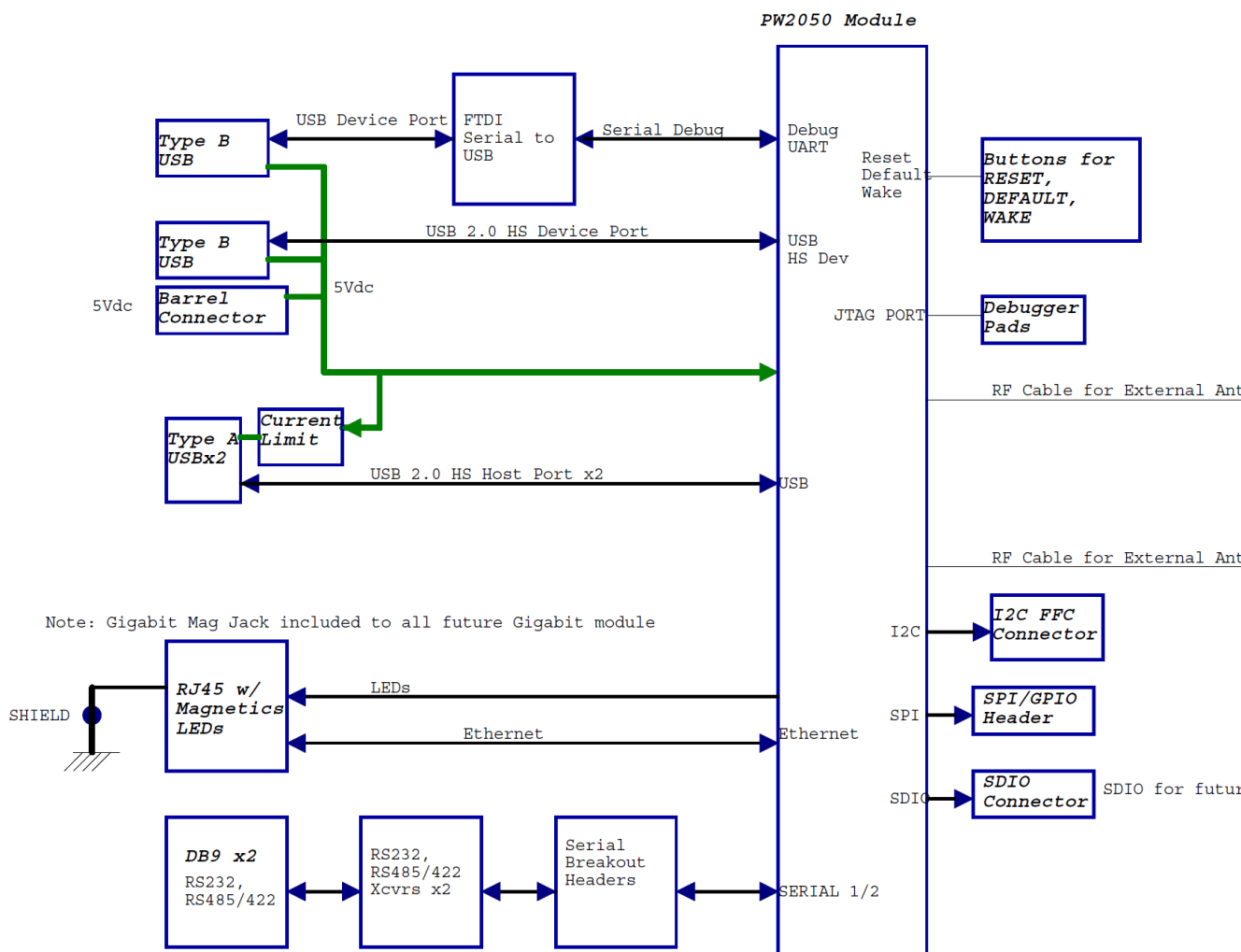
Figure 3-10 Evaluation Board Schematic (1 of 7)

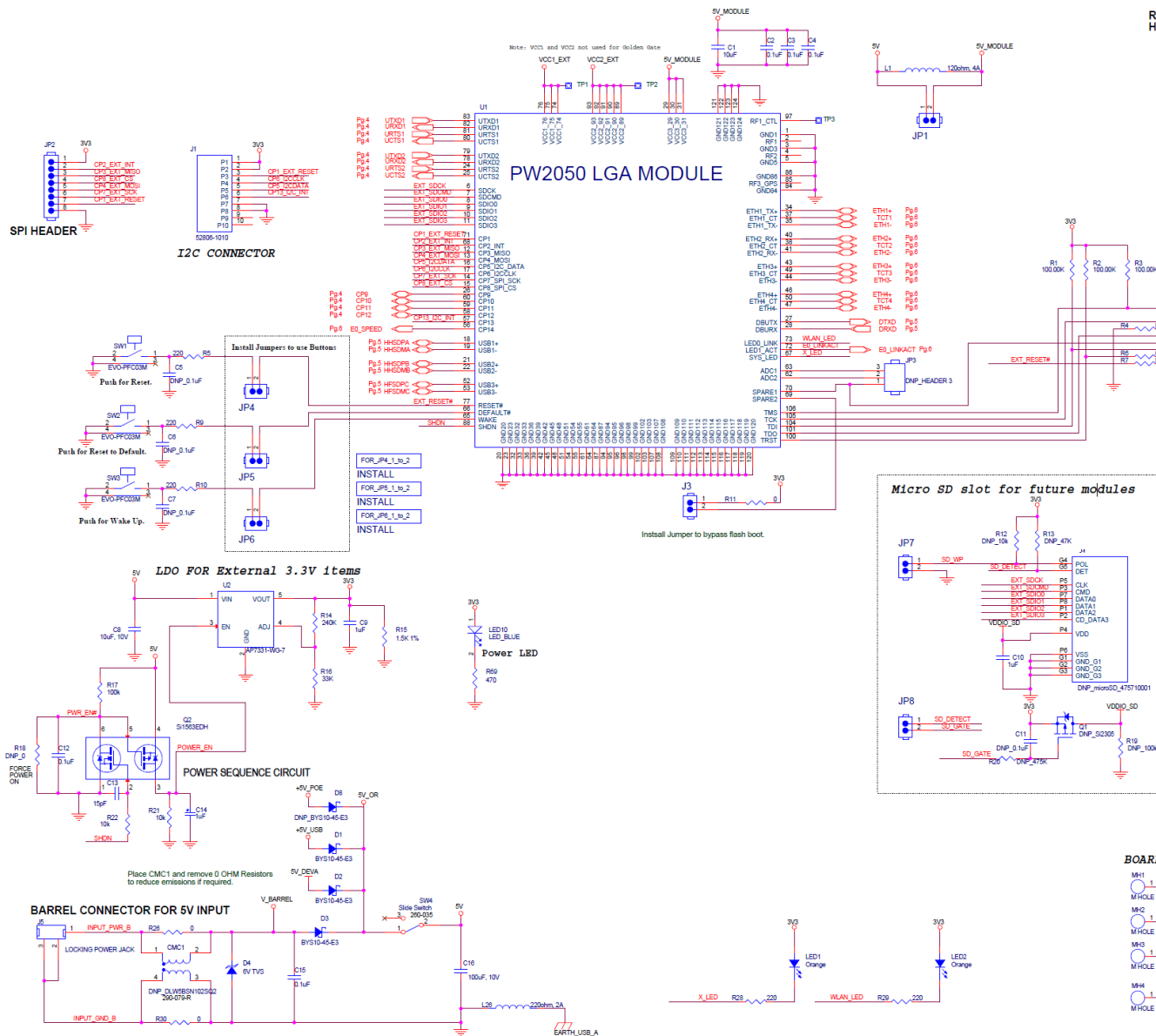**Figure 3-11 Evaluation Board Schematic (2 of 7)**
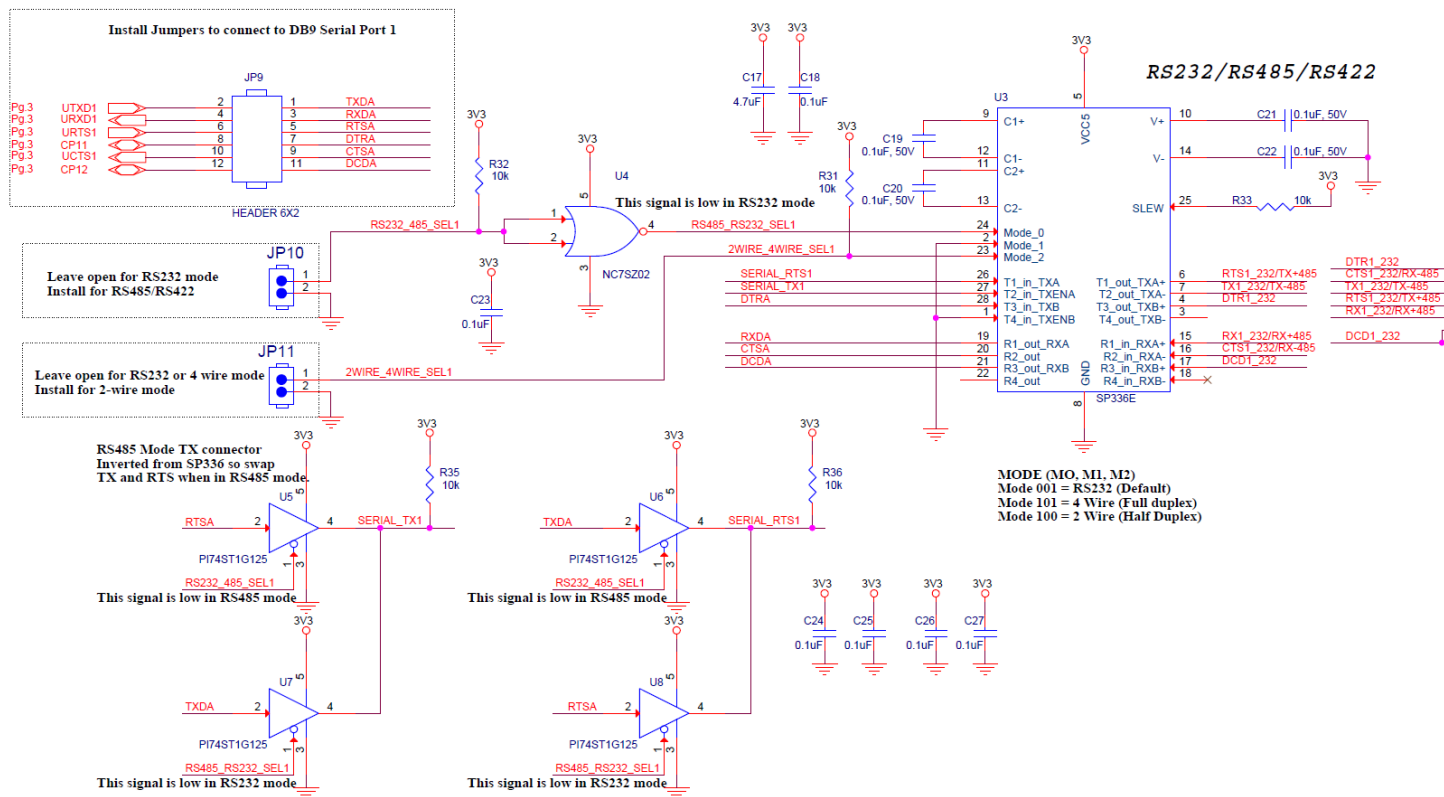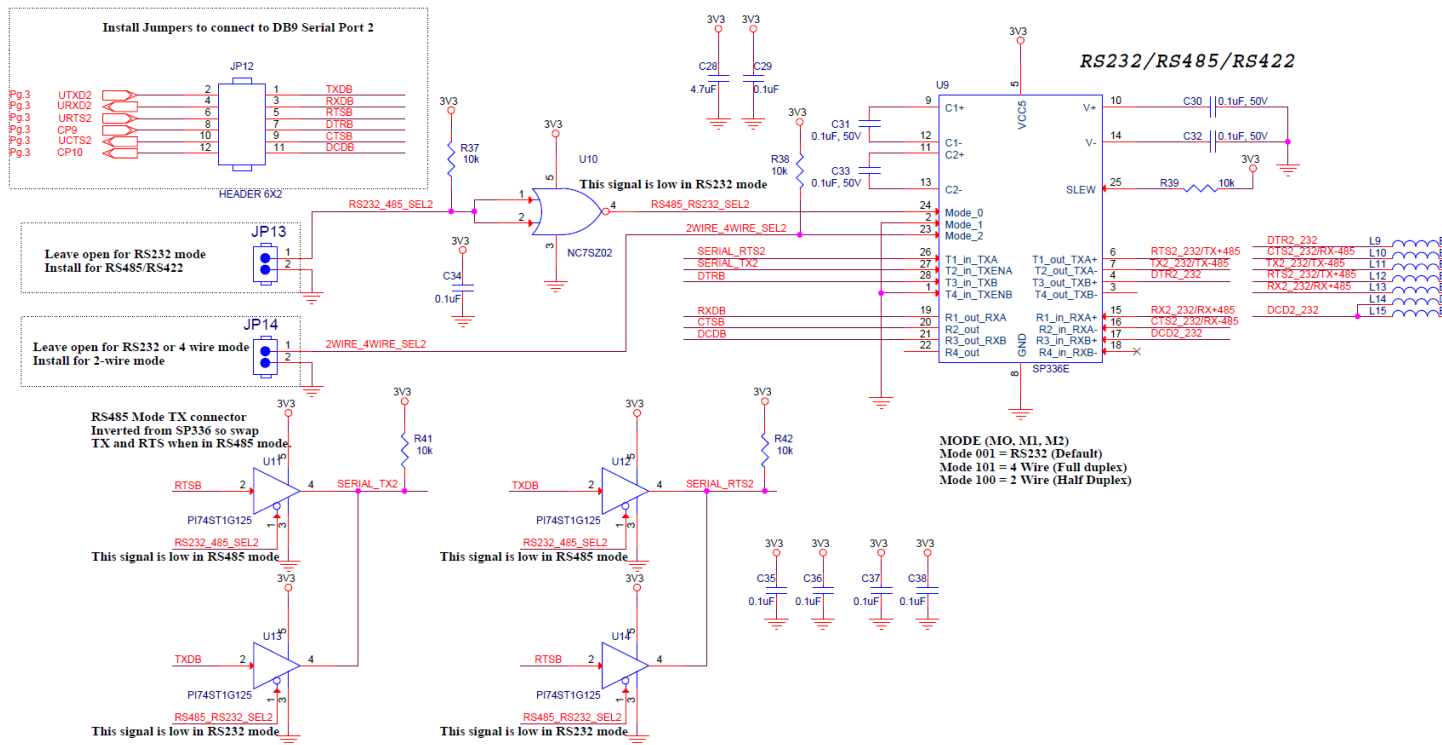
Figure 3-12 Evaluation Board Schematic (3 of 7)

Figure 3-13 Evaluation Board Schematic (4 of 7)
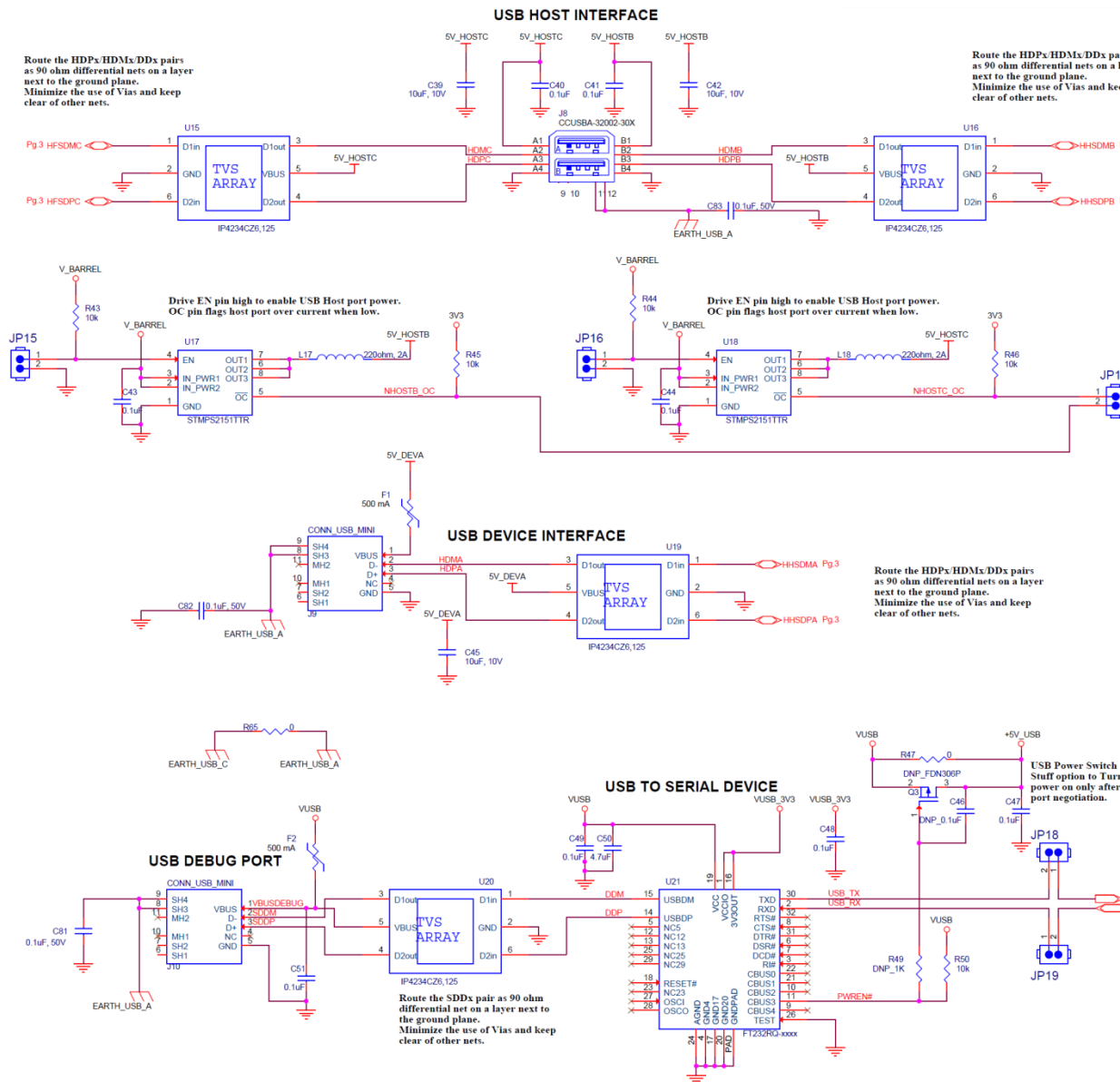
Figure 3-14 Evaluation Board Schematic (5 of 7)

Figure 3-15 Evaluation Board Schematic (6 of 7)
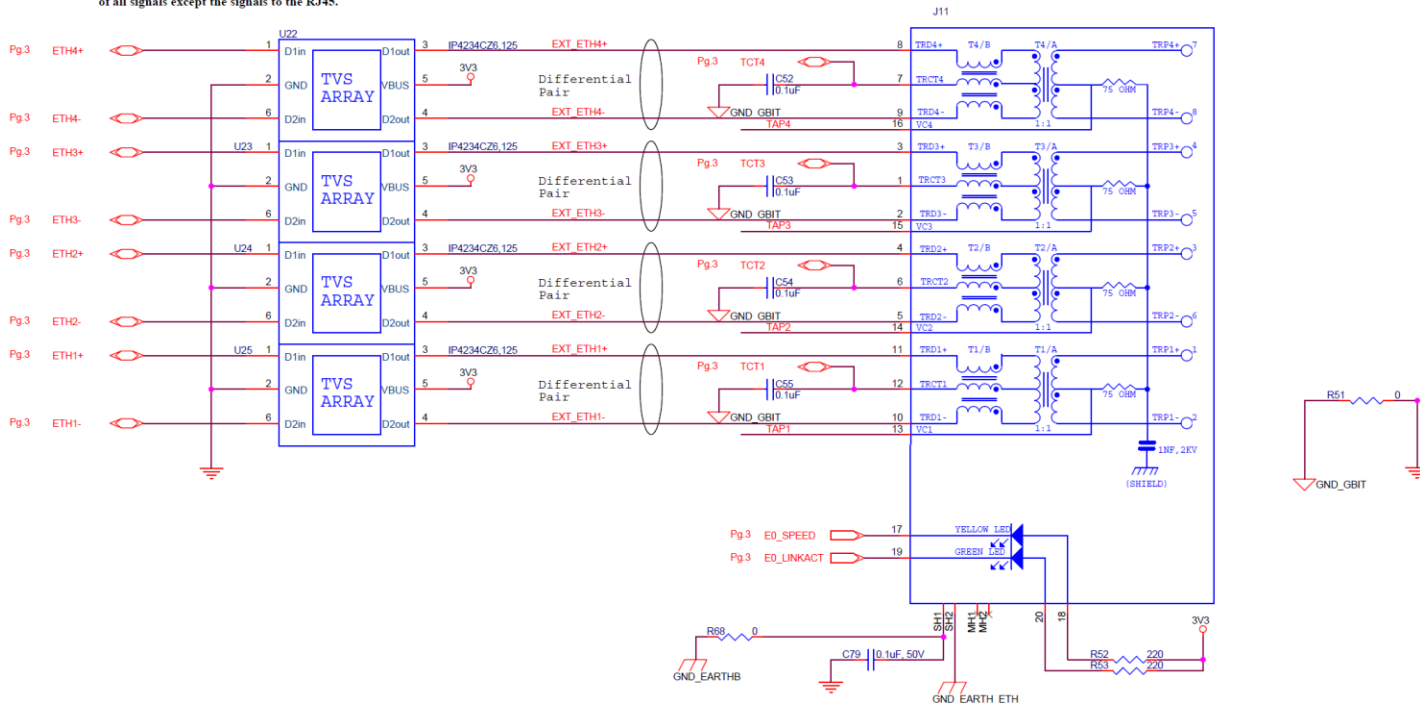
Figure 3-16 Evaluation Board Schematic (7 of 7)

POE Regulator

Signals in this box need to be isolated by
1500Vrms to all other signals.

RCL Class Resistor
Open, Class 0 = 12.95W max
127 ohm, Class 1 = 3.84W max
69.8 ohm, Class 2 = 6.49W max
45.3 ohm, Class 3 = 12.95W max
30.9 ohm, Class 4 = POE+ 17W max
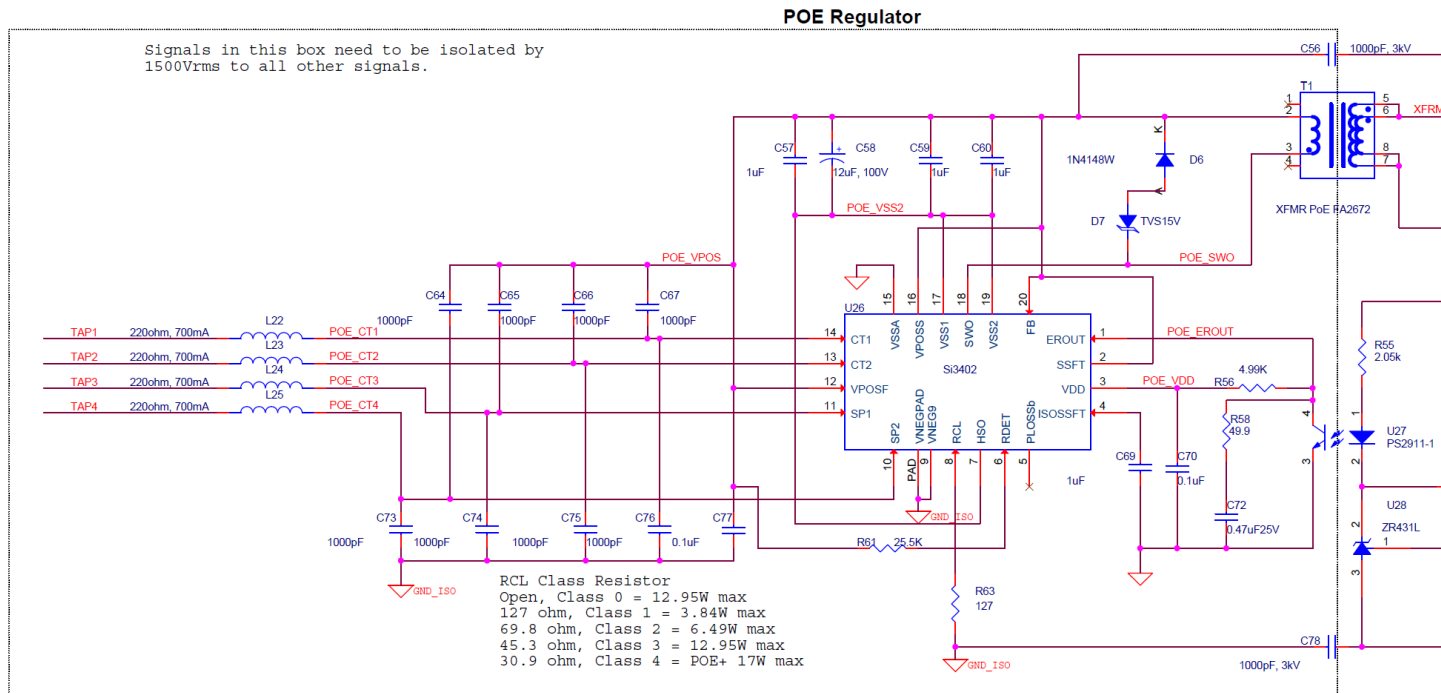
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