CSI-2/DSI D-PHY Rx IP Core - Lattice Radiant Software

User Guide

FPGA-IPUG-02081-1.3

November 2020

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AXI	Advance eXtensible Interface
CIL	Control and Interface Logic
CSI-2	Camera Serial Interface-2
DSI	Digital Serial Interface
EoTP	End of Transmission Packet
FIFO	First In First Out
FPGA	Field-Programmable Gate Array
HS	High-Speed
LMMI	Lattice Memory Mapped Interface
LP	Low Power
SoT	Start of Transmit
SoTp	Start-of-Sync Pattern

1. Introduction

The Lattice Semiconductor CSI-2/DSI D-PHY Receiver IP Core converts DSI or CSI-2 data to 8-bit, 16-bit, 32-bit, or 64-bit data for Lattice Semiconductor CrossLink™-NX and Certus™-NX family devices as indicated in the dark gray boxes in Figure 1.1.

The CSI-2/DSI D-PHY Receiver IP Core is intended for use in applications that require a D-PHY receiver in the FPGA logic. D-PHY Rx IP includes in it both the high speed and low power modules. The payload data (image data) uses the high-speed mode whereas the control and status information are sent through low power mode. The number of D-PHY data lanes to be used for the transmission of data is configurable and supported 1, 2, 3, or 4 data lanes.

The IP design is implemented in Verilog HDL language.

The Lattice Radiant® Place and Route tool integrated with the Synplify Pro® synthesis tool is used for implementation of the design. The design can be targeted to all CrossLink-NX and Certus-NX family devices.

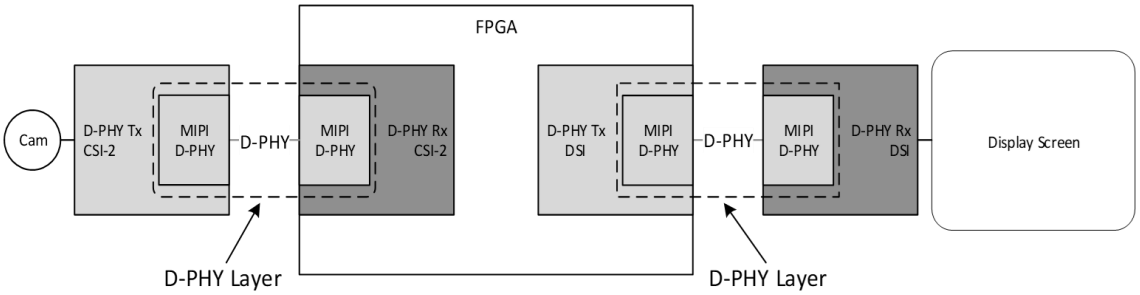

Figure 1.1. D-PHY Rx IP

1.1. Quick Facts

Table 1.1 presents a summary of the CSI-2/DSI D-PHY Rx IP Core.

Table 1.1. CSI-2/DSI D-PHY Rx IP Core Quick Facts

IP Requirements	Supported FPGA Family	CrossLink-NX, Certus-NX
Resource Utilization	Targeted Devices	LIFCL-40, LIFCL-17, LFD2NX-40
	Supported User Interfaces	LMMI/LINTR/AXI4 Stream Interface/ADC IP Core Native Interface
	Resources	See Table A.1.
Design Tool Support	Lattice Implementation	IP Core v1.0.x – Lattice Radiant Software 2.0 IP Core v1.1.x – Lattice Radiant Software 2.1 or later
	Synthesis	Lattice Synthesis Engine (LSE)
		Synopsys® Synplify Pro for Lattice
	Simulation	For a list of supported simulators, see the Lattice Radiant Software User Guide.

1.2. Features

- Compliant with MIPI D-PHY v1.1, MIPI DSI v1.1 and MIPI CSI-2 v1.1 Specifications.
- Selection between Hard Rx D-PHY or Soft Rx D-PHY implementation. Hard Rx D-PHY is only available for Crosslink-NX devices.
- Supports MIPI DSI and MIPI CSI-2 interfacing up to 6 Gb/s for Soft D-PHY and up to 10 Gb/s for Hard D-PHY.
- Supports 1, 2, 3, or 4 data lanes and one clock lane.
- Supports continuous and non-continuous MIPI D-PHY clock.
- Supports all MIPI DSI Video Mode of operation.
  - Non-Burst Mode with Sync Pulses
  - Non-Burst Mode with Sync Events
  - Burst Mode
- Optional packet parsing or parallel data translation only
- Supports optional periodic deskew detection
- Supports all MIPI DSI compatible video formats
- Supports all MIPI CSI-2 compatible video formats

1.3. Hard CSI-2/DSI D-PHY Rx IP Core Features

- Maximum rate is up to 2500 Mbps per lane
- Supports 8x or 16x gearing
- Option to use internal or external clock source
- Option to use hardened Control and Interface Logic (CIL) or Fabric Logic

1.4. Soft CSI-2/DSI D-PHY Rx IP Core Features

- Maximum rate is up to 1500 Mbps per lane
- Supports 8x gearing only
- External clock source

1.5. Conventions

1.5.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.5.2. Signal Names

Signal names that end with:

- *_n* are active low (asserted when value is logic 0)
- *_i* are input signals
- *_o* are output signals

2. Functional Description

The D-PHY Rx IP core consists of the Common Interface Wrapper module, Global Operations Controller module, optional Packet Parser, optional AXI4 Device Master, and optional LMMI Device Slave.

The D-PHY Rx IP block diagram configured with the AXI4-Stream OFF and the Packet Parser is OFF is shown in Figure 2.9.

The D-PHY Rx IP block diagram configured with the AXI4-Stream ON and the Packet Parser is OFF is shown in Figure 2.10.

The D-PHY Rx IP block diagram configured with the AXI4-Stream OFF and the Packet Parser is ON is shown in Figure 2.12.

The D-PHY Rx IP block diagram configured with the AXI4-Stream ON and the Packet Parser is ON is shown in Figure 2.13.

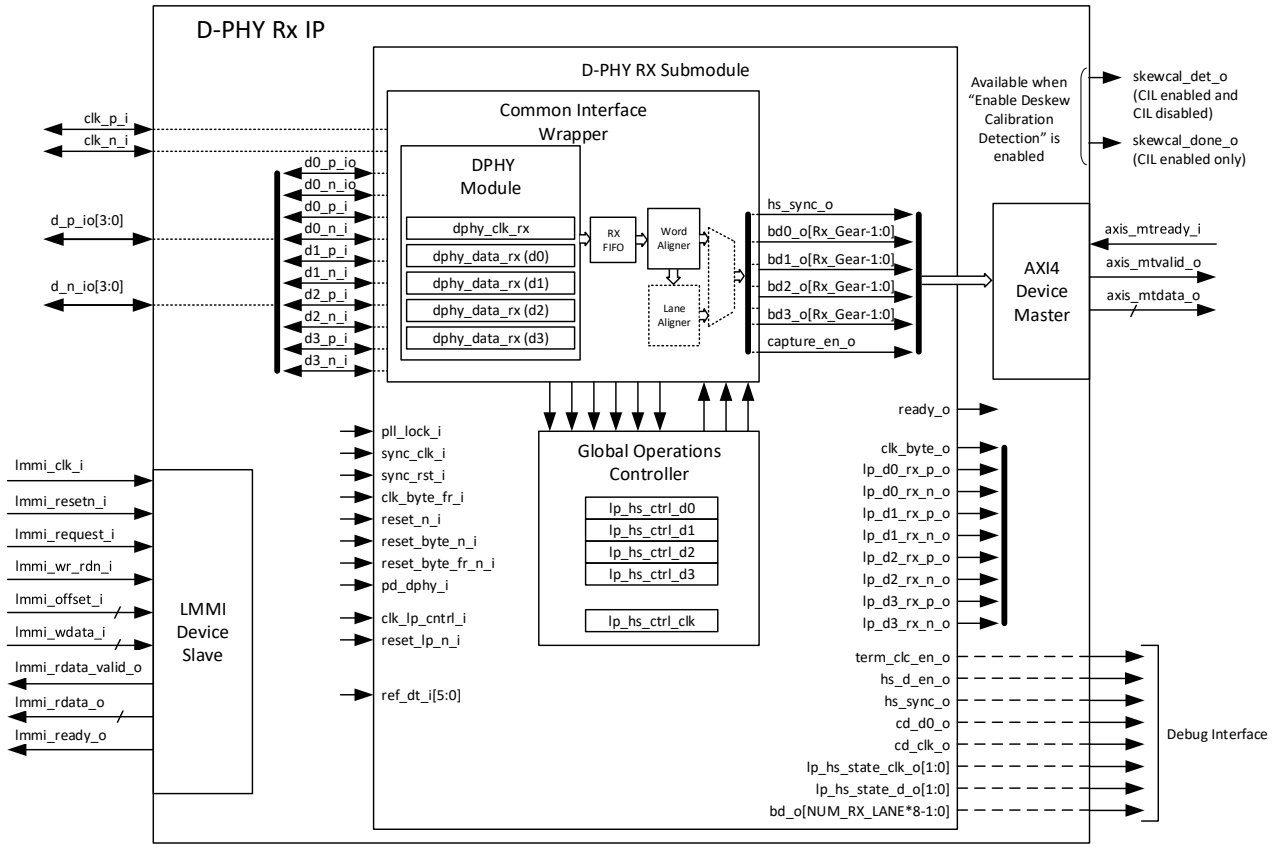

Figure 2.1. D-PHY Rx IP Block Diagram with AXI4-Stream Enabled, LMMI Enabled and Packet Parser OFF

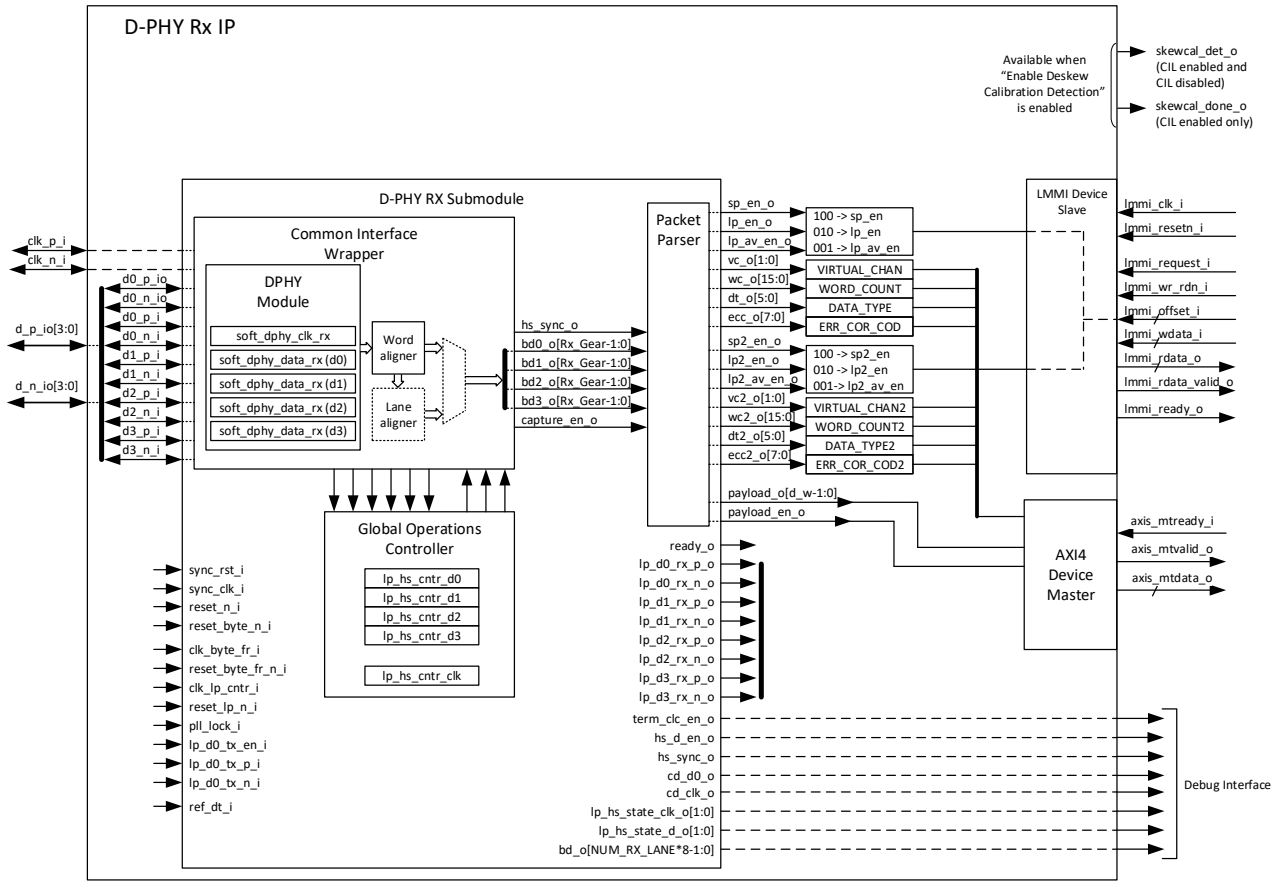

Figure 2.2. D-PHY Rx IP Block Diagram with AXI4 Stream Enabled and LMMI Disabled

2.1. D-PHY Rx Common Interface Wrapper

The Common Interface Wrapper module instantiates either the hard or the soft D-PHY module to receive MIPI D-PHY data from all enabled data lanes.

When soft D-PHY is used, this module also includes the Word Aligner module and optionally a Lane Aligner to ensure the correct alignment of bytes among the D-PHY data lanes. See Word Aligner and Optional Lane Aligner for more details regarding these modules.

2.2. D-PHY Module

The D-PHY module instantiates either the hardened D-PHY module or a soft logic equivalent using the FPGA fabric and generic blocks.

The hardened PHY module divides the high-speed D-PHY clock to create the output byte clocks clk_byte_o and clk_byte_hs_o. The clk_byte_hs_o is toggling when the D-PHY clock lane is active, therefore, this can be used as the input clock clk_byte_fr_i when the source D-PHY clock is continuously running. The clk_byte_o, on the other hand, is active only after the deserializer within the hard PHY block detects the Start-of-Sync pattern (SoTp) and stops when the data lanes go out of high-speed mode. This clock is used as strobe to latch the parallel byte data from the hardened D-PHY block. Due to its dependence on the SoTp detection, the clk_byte_o is out of phase with the clk_byte_hs_o.

When the soft PHY is used, the clk_byte_o is the same as the clk_byte_hs_o. Both are the outputs of a clock divider with the D-PHY clock as its input.

2.3. RX_FIFO

As mentioned in the D-PHY Module section, the data words from the D-PHY module is synchronous with the output clock clk_byte_hs_o. The rest of the data path, including the soft aligner modules, are clocked by the input clk_byte_fr_i. An rx_fifo module is used to cross the data between these two clock domains. When the hardened Control Interface Logic (CIL) is enabled, the RX_FIFO Module is not used. Instead, a single 1024-deep dual-clock FIFO is used.

In the case of the soft PHY implementation, the RX_FIFO is instantiated before the D-PHY module and the Word Aligner module. Data being buffered includes the hs-zero bytes before the SoTp, the actual packets, the trail bits, and the data lane value right before the D-PHY lanes transition to LP-11.

The various implementation types are discussed below.

2.3.1. RX_FIFO OFF

If the clk_byte_fr_i has the same frequency and is synchronous with the clock strobe clk_byte_o, then the RX_FIFO can be removed. In the actual generated design, there is still a fixed 4-deep single clock FIFO implemented as LUTs.

This is the recommended setting when the D-PHY module is using Soft D-PHY implementation with the D-PHY clock running continuously in high-speed mode and the clk_byte_fr_i is driven by the clk_byte_hs_o.

2.3.2. RX_FIFO_TYPE = SINGLE

The RX_FIFO Single Type is primarily intended as an elastic FIFO to buffer the frequency or phase difference between the stoppable byte clock domain (clk_byte_o) and the continuous byte clock domain.

The MIPI D-PHY protocol itself does not allow data throttling when high speed transfer is already on-going. Full or empty FIFO condition does not halt the data stream. Therefore, it is important that the depth of the FIFO and the packet delay be configured properly to ensure it does not overflow or underflow.

When the two byteclocks have slightly different frequency (such as using two different oscillators with ppm tolerance), it is recommended to increase the buffered data before reading out from the FIFO using the packet delay parameter. If the continuous clock is slightly slower than the strobe clk_byte_o and the Low-Power period between high speed transfers is enough to absorb the time difference, the delay value can be set to 1; depth depends on the amount of possible accumulated data due to the clock difference.

When the frequency of both clocks are exactly the same but are out-of-phase, as in the case when the input clock clk_byte_fr_i is driven by the clk_byte_hs_o from the Hard D-PHY module in continuous clock mode, the delay value can be set to 1 and depth should be set to 16, which is the minimum depth due to the FIFO control signals crossing clock boundaries.

In all cases of the Single Type RX_FIFO, the read from the FIFO would continue until the empty flag asserts. The interval between high speed transactions (low-power blanking) must be long enough to ensure the FIFO is already empty before the next one is written, otherwise, the FIFO assumes it is still part of the previous data stream. This causes the word aligner to miss the SoTp of the second data stream and interpret the packets erroneously.

Figure 2.3 illustrates the contents of the FIFO when a high-speed blanking DSI stream is being buffered using the RX_FIFO SINGLE.

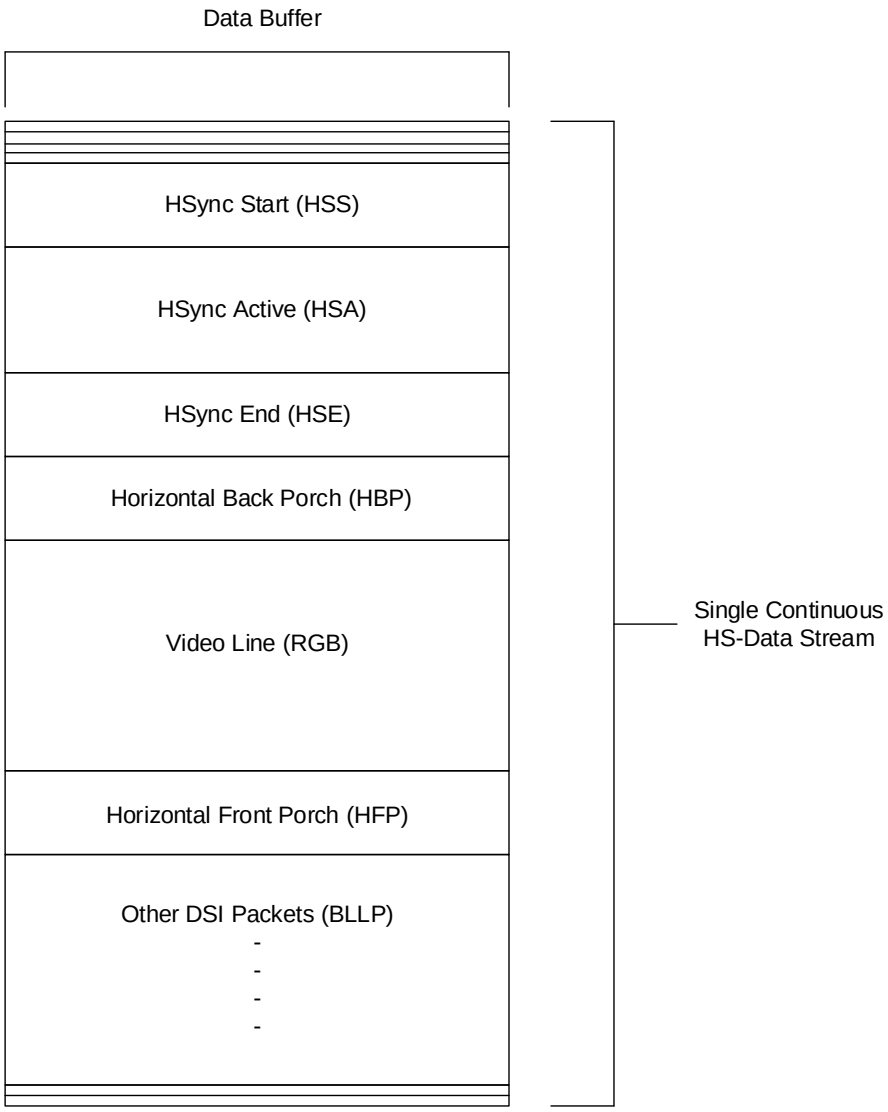

Figure 2.3. RX_FIFO SINGLE

2.3.3. RX_FIFO_TYPE = PINGPONG

This FIFO instantiates two dual_clock FIFOs that alternately stores data every high-speed transaction. Each data buffers must be good enough to hold the largest data within a high-speed transaction, including the hs-zero, SoTp, and trail bits.

Similar with the single type, this also has a parameterized delay before reading out from the buffer to maintain intervals between packets. If packet delay = 0, read starts once its empty signal deasserts and the other one is not busy with read. If packet delay is non-zero, read from that buffer starts once the delay value is met and the other one is not busy with read. This implementation does not track the number of entries within the buffers; read stops once it sees the empty flag. Each buffer is reset after its read operation.

This type is more suitable for high-speed transfers with short intervals because data is written alternately between the two buffers. This is recommended for DSI with low power blanking.

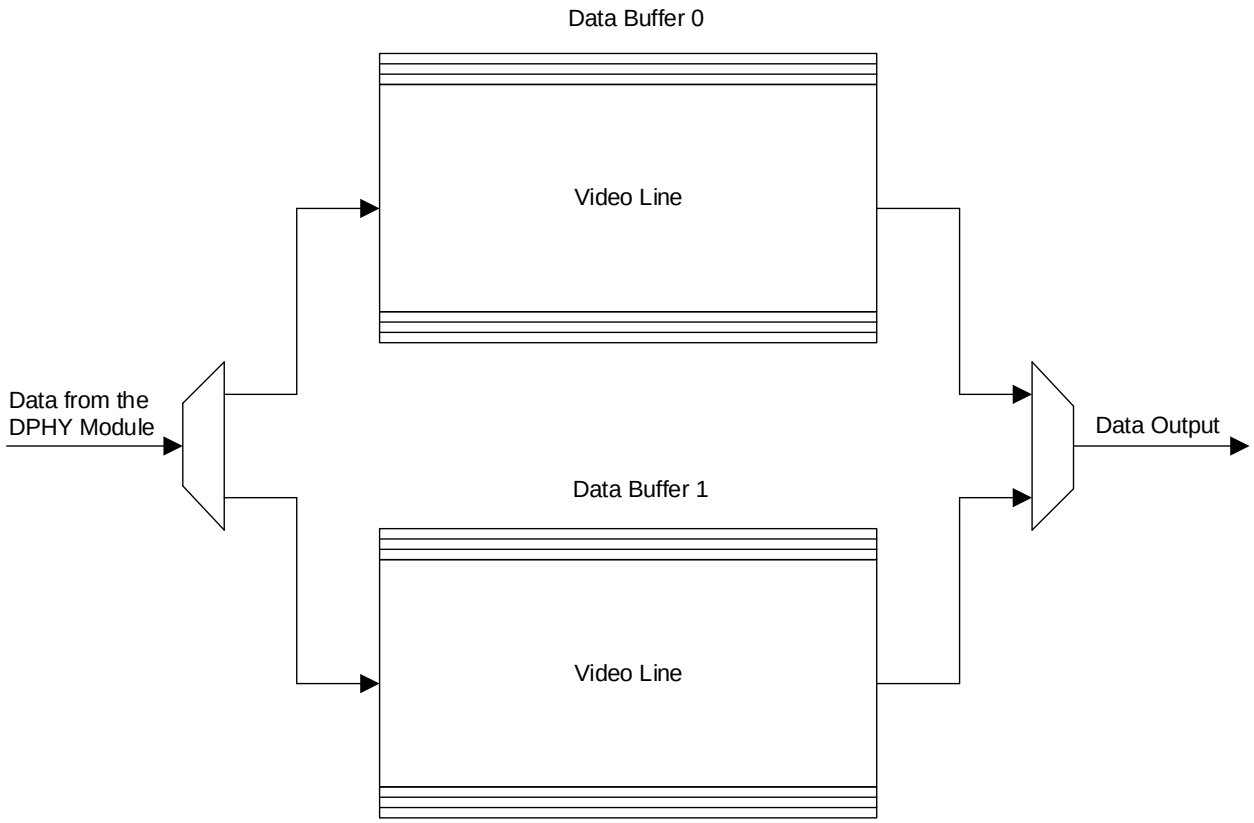

Figure 2.4. RX_FIFO PINGPONG

2.3.4. RX_FIFO_TYPE = Queue

This FIFO instantiates one dual-clock FIFO. This also acts as a circular buffer that must be able to hold data from multiple high-speed transactions.

Unlike the other two types, this does not have a delay counter. Instead, HS data is buffered completely and a counter tracks the number of rows written during the high-speed transaction. This count is stored in an entry queue.

When there is a valid entry in the entry queue, read from the data buffer is triggered. The number of read cycles from the data buffer corresponds to the entry read from the entry queue. This enables the FIFO controller to distinguish the boundaries between successive HS transactions. This introduces significant latency on the first video line, but this also enables the IP to support short intervals between HS transactions.

This is suitable for CSI-2, wherein the packet intervals are not critical, but the intervals between successive high-speed transactions are short.

Figure 2.5 illustrates a sample entry within a 4-deep entry queue for a CSI-2 sequence.

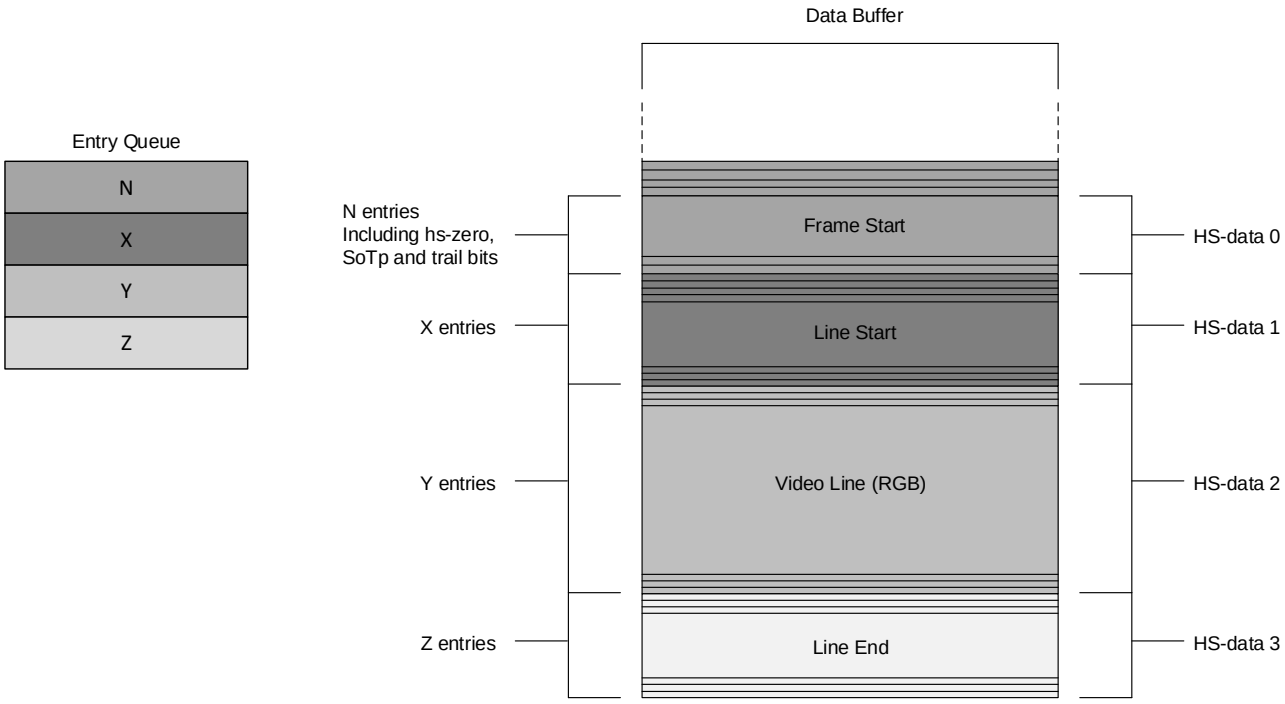

Figure 2.5. RX_FIFO QUEUE

2.4. Global Operations Controller

This block controls the high-speed termination enable of MIPI D-PHY IP clock and data lanes. Figure 2.6 shows the LP-to-HS transition flow diagram for data lanes.

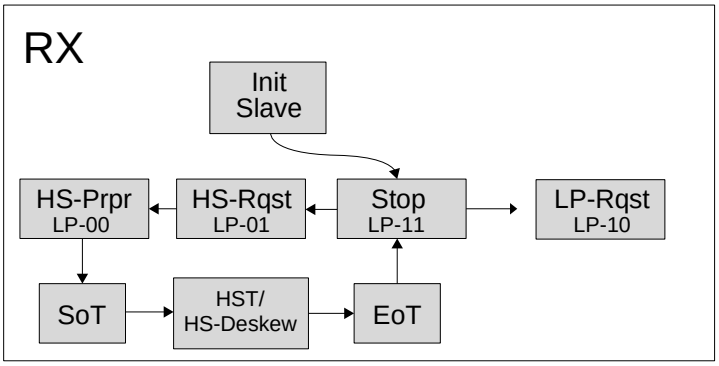

Figure 2.6. MIPI D-PHY Rx LP to HS Transition Flow Diagram on Data Lanes

When the MIPI D-PHY clock is continuous, the HS termination enable of clock lane is tied to VCC. When the MIPI D-PHY clock is non-continuous, the HS termination enable of clock lane becomes active right after proper LP to HS transition is observed. A reference clock input is required for this function. Figure 2.7 shows the required LP to HS transition on clock lane as per MIPI D-PHY Specification version 2.1.

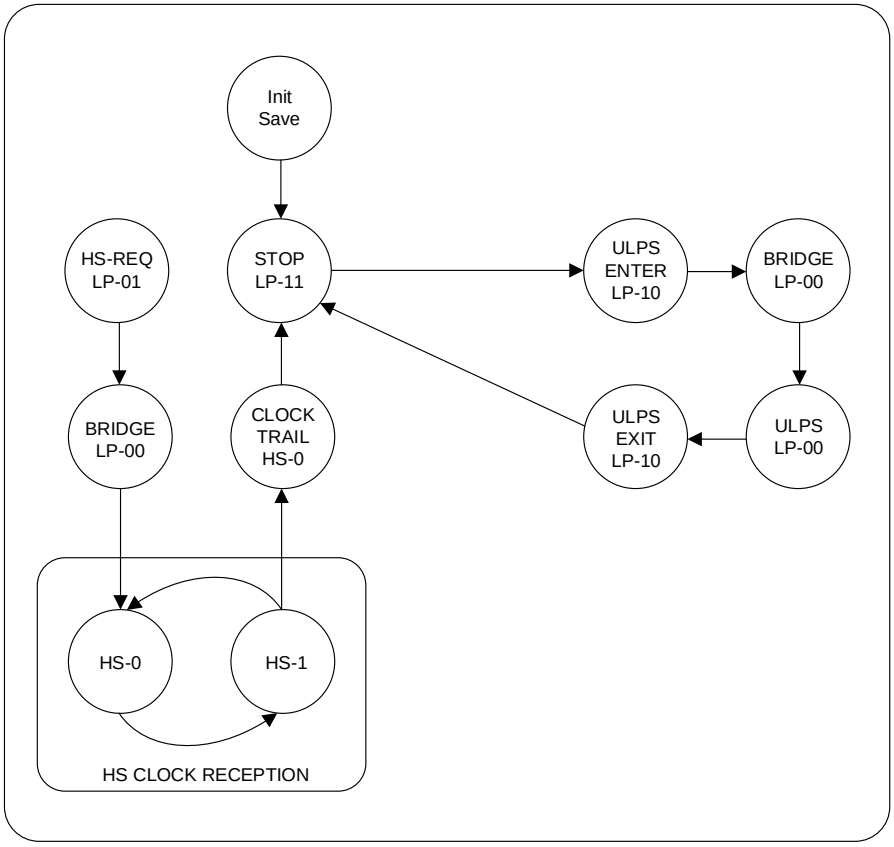

Figure 2.7. MIPI D-PHY Rx LP to HS transition on Clock Lane

During normal operation, a Data Lane is either in Control or in High-Speed (HS) mode.

From a low-power (control) mode, the D-PHY transmitter performs the high-speed entry sequence on the data lanes which consists of driving LP11->LP01->LP00 as shown in the Figure 2.8. Upon successful detection of this sequence, the Global Operations Controller enables the differential resistor termination to receive the high-speed data. A free-running byte clock is used during HS mode.

Once enabled, HS receiver termination continues to receive the data until it encounters the LP11 state on the lanes, which is also known as the Stop State. The Stop State brings back the data lane from high-speed mode to low power mode.

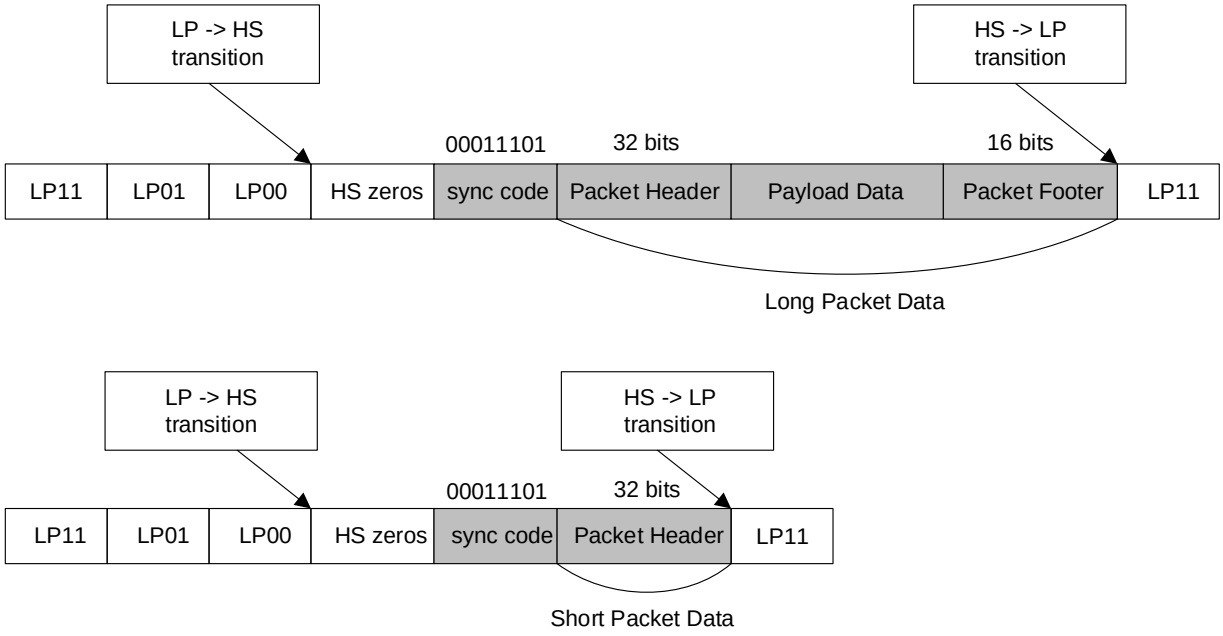

Figure 2.8. High Speed Entry Sequence and Payload Data Transmission Cycle on Data Lanes

2.5. D-PHY Rx IP without Packet Parser

When D-PHY Rx IP is configured without the packet parser, as shown in Figure 2.9 and Figure 2.10, the output is the received bytes from the D-PHY Rx IP starting from the reception of the Start of Transmit (SoT) code in all the active data lanes until the detection of the LP-11 signifying the end of high-speed transmission.

In the case of D-PHY Rx IP configured without Packet Parser, the obtaining and decoding the valid data packets from the trail is the task of interfacing logic. This configuration is useful for bridging D-PHY packets without going to the protocol level.

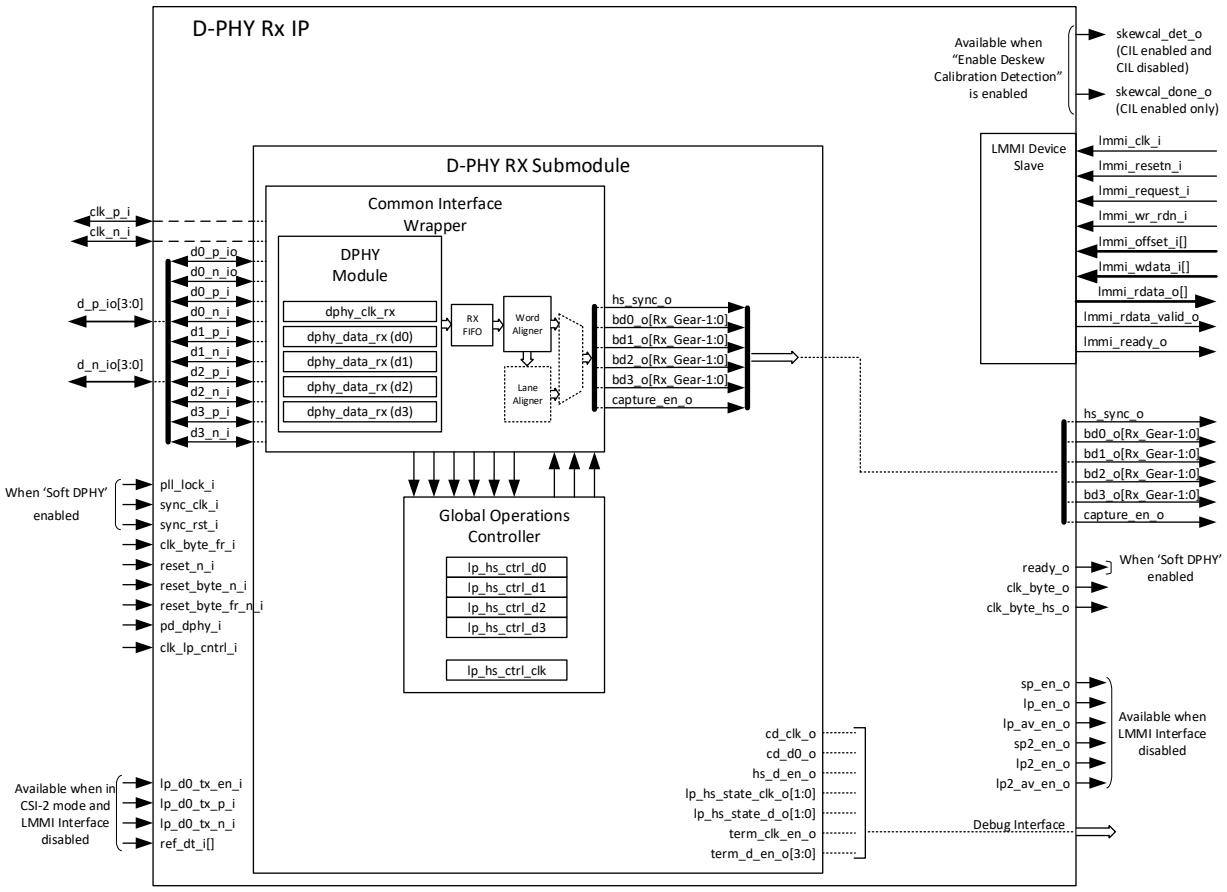

Figure 2.9. D-PHY Rx IP Configuration with AXI4-Stream Disabled and Packet Parser Disabled

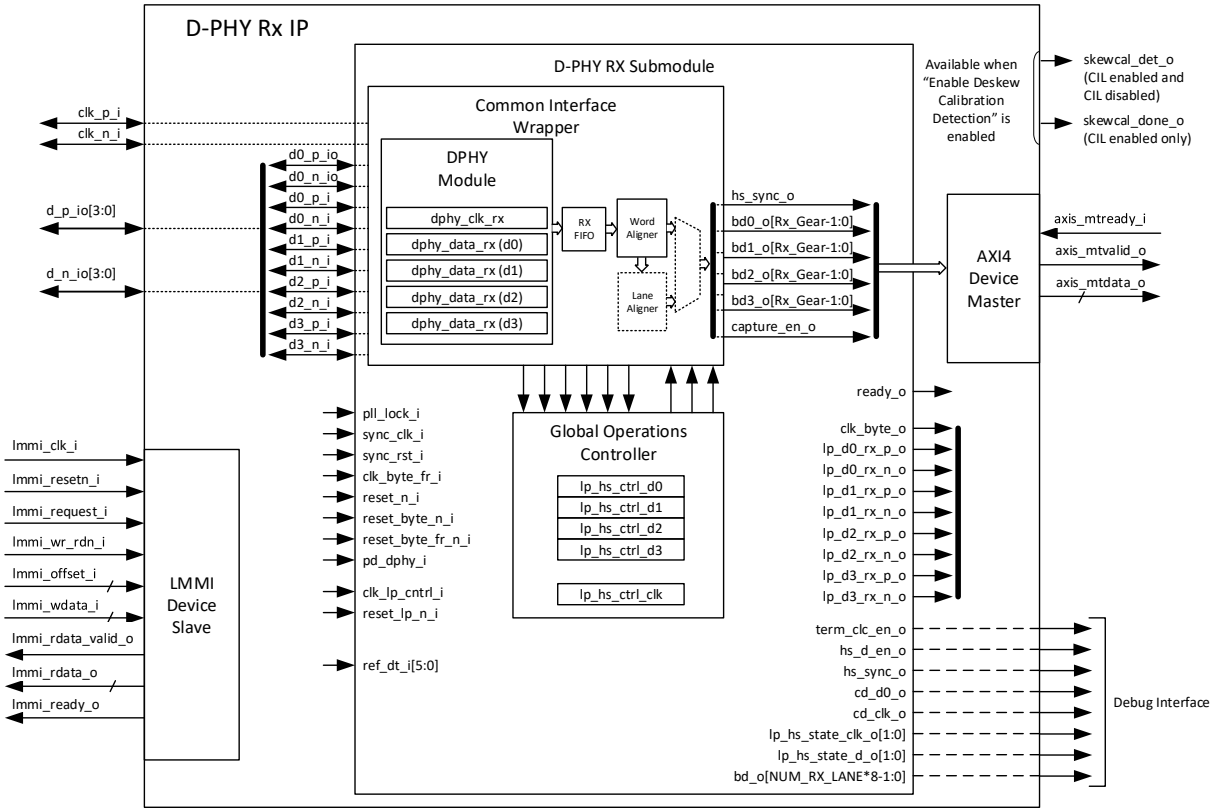

Figure 2.10. D-PHY Rx IP Configuration with AXI4-Stream Enabled and Packet Parser Disabled

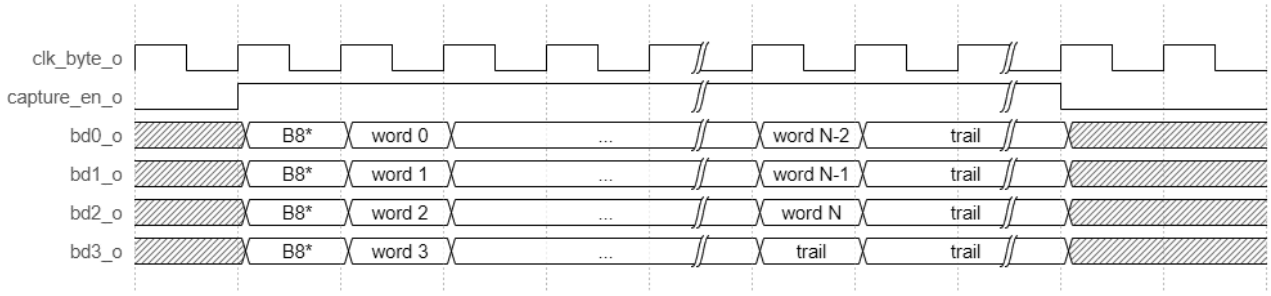

Figure 2.11. D-PHY Rx IP Output Timing Diagram without Packet Parser

2.6. D-PHY Rx IP with Packet Parser

When D-PHY Rx IP is configured with the DSI/CSI-2 Packet Parser included, as shown in Figure 2.12 and Figure 2.13, the parser checks the incoming data for a valid data type and the corresponding packet fields.

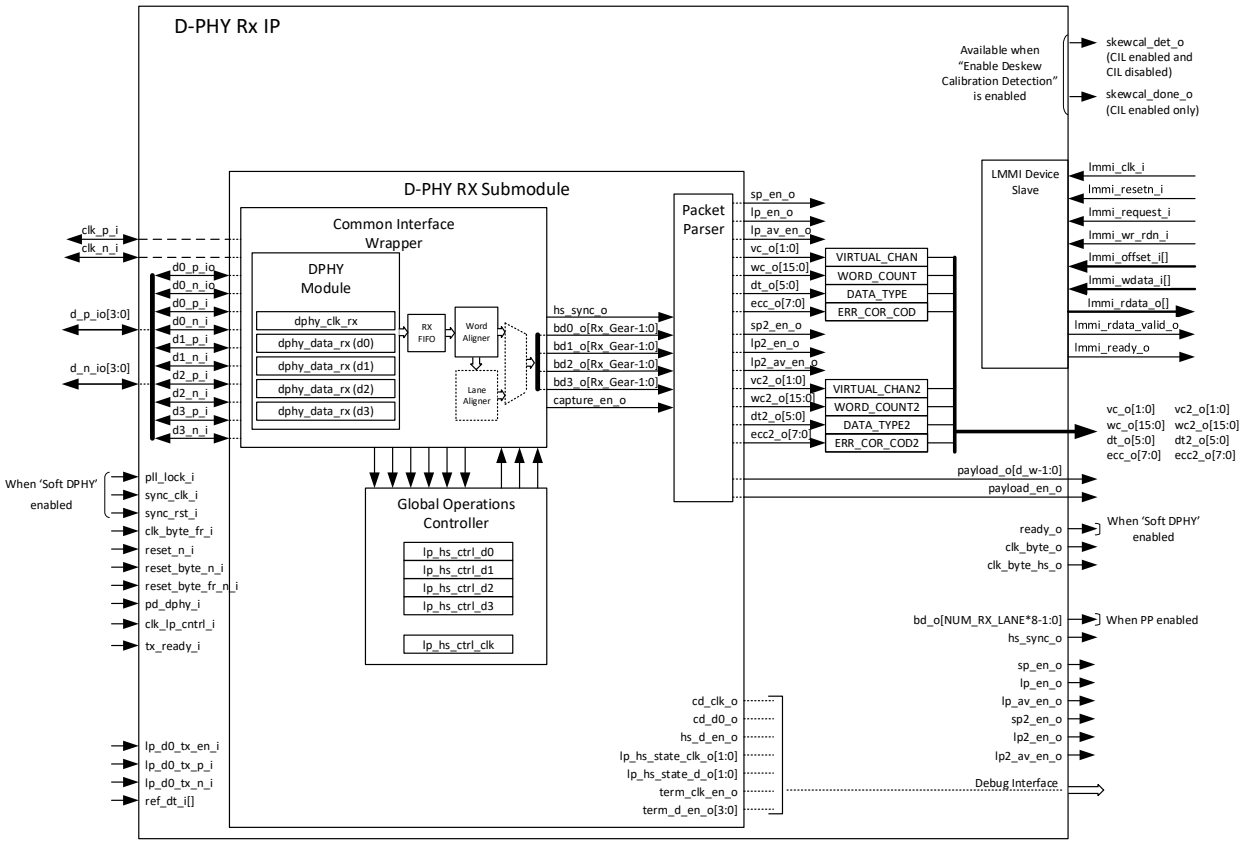

Figure 2.12. D-PHY Rx IP Configuration with AXI4-Stream Disabled and Packet Parser Enabled

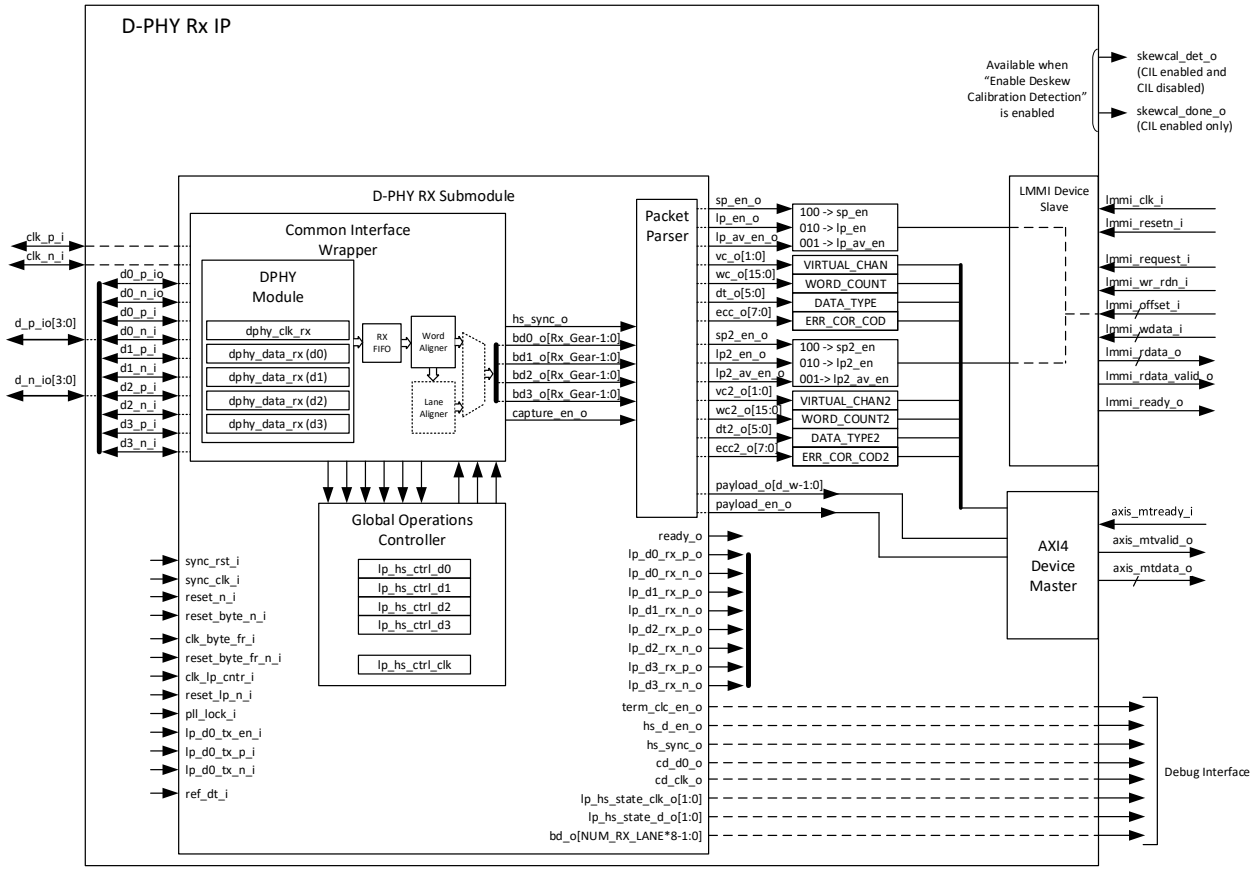

Figure 2.13. D-PHY Rx IP Configuration with AXI4-Stream Enabled and Packet Parser Enabled

2.7. Packet Parser

The Packet Parser module parses the data bytes from D-PHY Common Interface Wrapper, and detects short and long packets defined by MIPI DSI or MIPI CSI-2. This block extracts video data and other control parameters from the packets. There are no signals from the external logic to this block to control the flow of output data. The interfacing logic must provide ample buffering to ensure the continuous flow of data from this submodule is transferred correctly. The output-timing diagram of DHPY-Rx IP interface with the packet parser enabled is shown in Figure 2.14.

The lp_en_o or sp_en_o signal asserts when a valid data type is received. These signals also indicate the valid data type, virtual channel ID, wordcount, and ECC fields. The lp_av_en_o only asserts with the lp_en_o, if the long packet received is the same as the input reference data type ref_dt_i. This is to differentiate active video packets from other long packets, such as null or blanking. Consequently, this signal does not assert on any video data type other than the defined ref_dt_i value. The payload_en_o signal indicates that the data in the payload_o bus contain the valid payload bytes. The width of the payload, data_width, is the number of gear bits multiplied by the number of data lanes. Upper data bytes for the last payload data must be ignored if the wordcount is not a multiple of data_width/8. The interfacing module should be responsible for extracting the correct payload bytes based on the valid output wordcount wc_o.

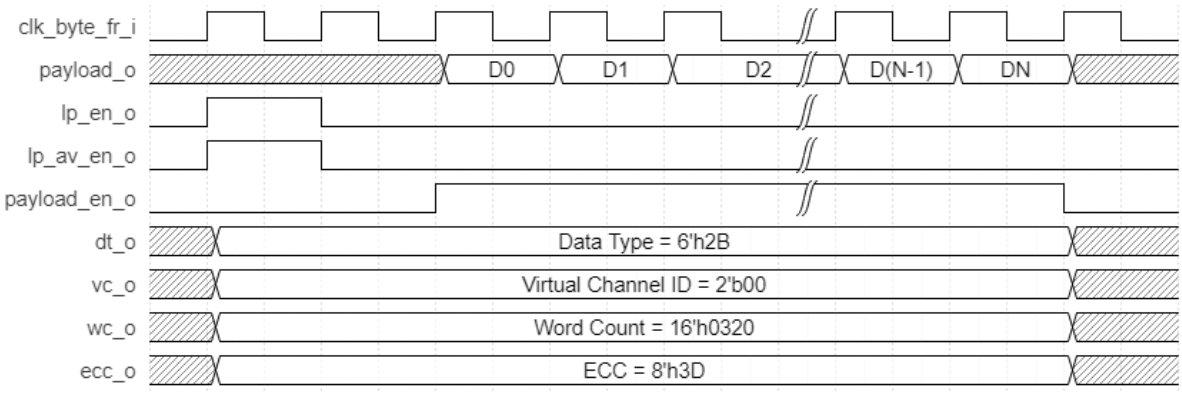

Figure 2.14. D-PHY Rx IP Output Timing Diagram with Packet Parser

When the input data bus going to the packet parser is greater than 32 then the Second Set of Packet is valid. In this configuration, two packet headers may simultaneously be decoded within the same byte clock cycle.

The Packet Parser input and output Timing Diagram with valid Second Set of Packet Information is shown in the Figure 2.15.

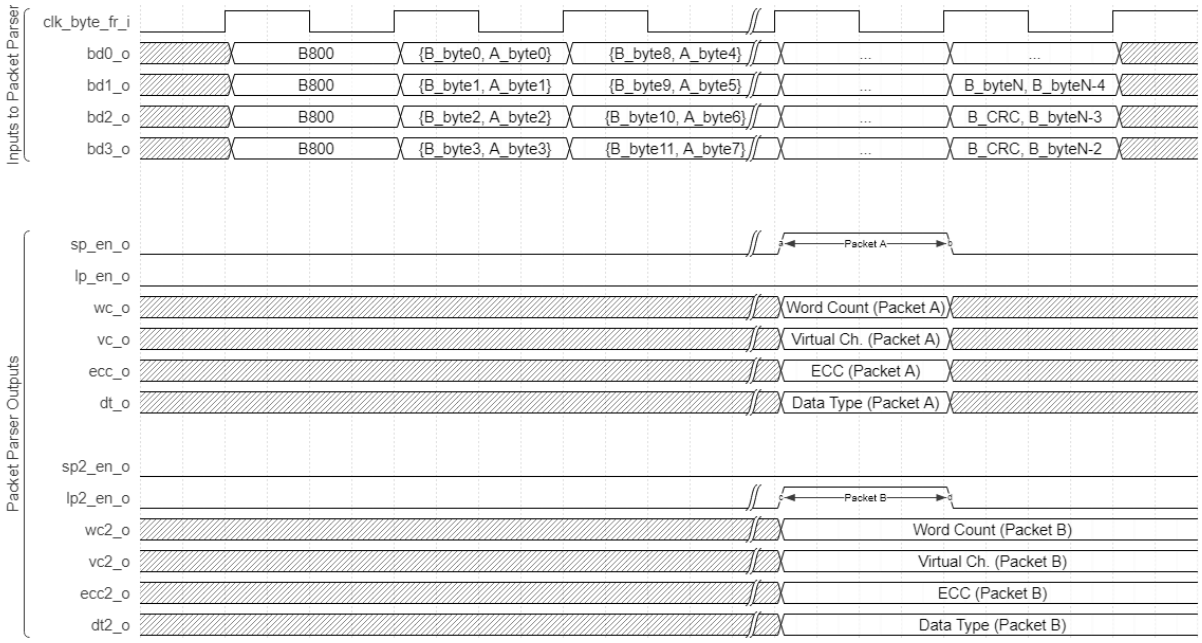

Figure 2.15. Output Timing Diagram with Valid Second Set of Packet Information

2.8. Word Aligner and Optional Lane Aligner

Before the payload data of every HS burst on each lane, the transmitting D-PHY inserts a sync sequence Start-of-Transmit (SoT) pattern. In the case of the hardened PHY, the hard deserializer already checks for the sync pattern on each lane. In the case of the soft PHY, a Word Aligner module is to detect the pattern in the deserialized data and establish the correct byte boundary on the high speed payload data.

The Word Aligner logic detects the SoT pattern from each lane and ensures the parallel data are word (byte) aligned. The design assumes that input data lanes are driven at the same time, and skew between data lanes are less than 1 UI. However, due to deserialization, data buffering and handling of clock domain crossing signals, the detection of the aligned data from all the lanes may not happen at the same cycle. An optional lane aligner module may be instantiated to rectify this issue, see Figure 2.16.

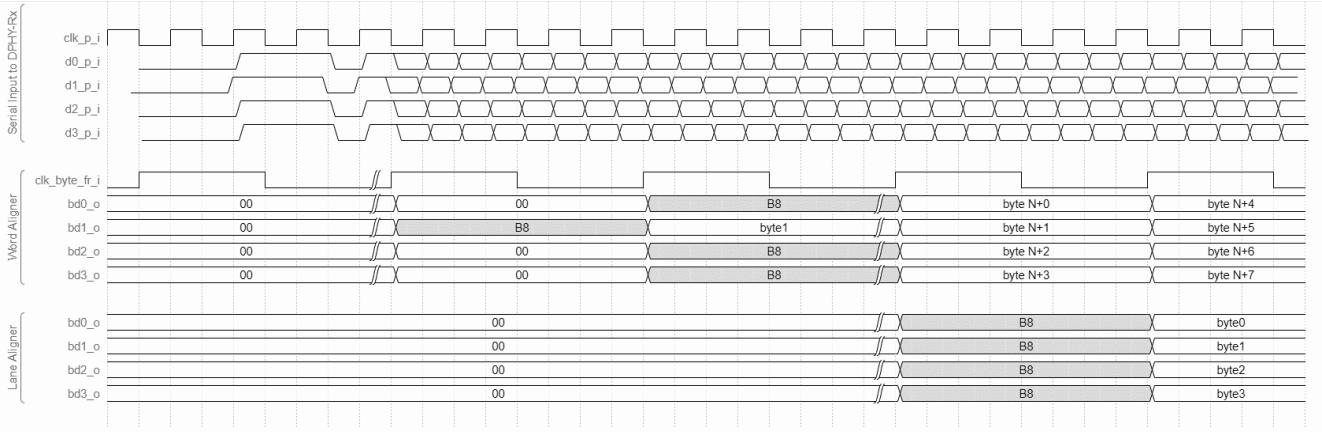

Figure 2.16. Lane Data Alignment

2.9. AXI4-Stream Device Master

AXI4-STREAM Device Master provides an interface for transmitting payload data (Byte Data or Packet Data with Virtual Channel, Data Type and Word Count). Figure 2.17 shows data format when AXI4-Stream is enabled.

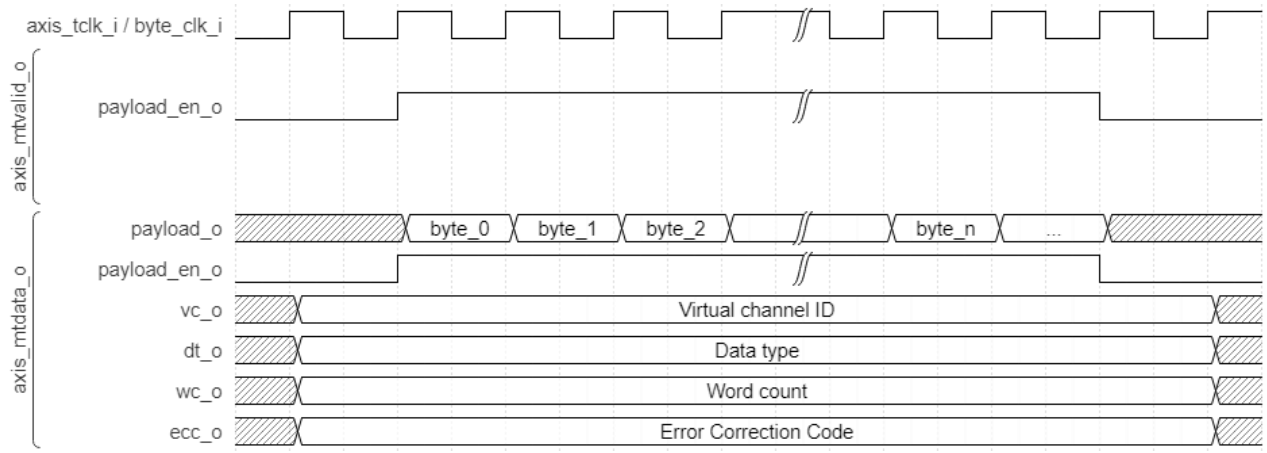

Figure 2.17. AXI4-Stream is ON and Packet Parser is ON Data Format

If the AXI4 Stream Device is not enabled and the D-PHY Rx IP is configured with Packet Parser (see Figure 2.12 and Figure 2.13), then the internal signals listed below turn to top level input signals as shown in Figure 2.14.

- payload_o[*NUM_Rx_LANES*Rx_Gear*-1:0]
- payload_en_o
- vc_o[1:0]
- wc_o[15:0]
- dt_o[5:0]
- ecc_o[7:0]
- vc2_o[1:0]
- wc2_o[15:0]
- dt2_o[5:0]
- ecc2_o[7:0]

If the AXI4 Stream device is not enabled and the D-PHY Rx IP is configured without Packet Parser (see Figure 2.10 and Figure 2.11), then the internal signals listed below turn to top level input signals.

- capture_en_o
- bd0_o[*Rx_Gear*-1:0]
- bd1_o[*Rx_Gear*-1:0]
- bd2_o[*Rx_Gear*-1:0]
- bd3_o[*Rx_Gear*-1:0]

2.10. LMMI Device

The LMMI Device Slave module (Lattice Memory Mapped Interface) is used for configuring the control registers of the Hard D-PHY Rx IP.

For more information on LMMI, refer to Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039).

3. Signal Description

D-PHY Rx IP Input and Output signals and their description are shown in Table 3.1.

Table 3.1. D-PHY Rx Port Description

Port Name	Direction	Mode/Configuration	Description
LMMI			
lmmi_clk_i	In	—	LMMI Interface clock
lmmi_resetn_i	In	—	Active low signal to reset the configuration registers
lmmi_wdata_i[*LDW1* – 1:0]	In	—	Start transaction
lmmi_wr_rdn_i	In	—	Write = HIGH, Read = LOW
lmmi_offset_i[*LOW2* – 1:0]	In	—	Register offset, starting at offset 0
lmmi_request_i	In	—	Write data
lmmi_ready_o	Out	—	Read data
lmmi_rdata_o[*LDW1* – 1:0]	Out	—	Read transaction is complete and lmmi_rdata_o[] contains valid data.
lmmi_rdata_valid_o	Out	—	Ready to start a new transaction
AXI4 Master Stream			
axis_mtready_i	In		Indicates that the module at the receiving end is ready to receive the data from the CSI-2/DSI D-PHY RX IP module.
axis_mtvalid_o	Out		AXI4-Stream indicates that data to be transmitted is valid.
axis_mtdata_o[N-1:0]*	Out		Payload data transmitting channel (Byte Data or Packet Data with Virtual Channel and Data Type and Word Count).
D-PHY Rx			
tx_ready_i	In	Available when AXI-4 stream is disabled	Indicates that the module at the receiving end is ready to receive the data from the the CSI-2/DSI D-PHY RX IP module.
ref_dt_i[5:0]	In	Available when LMMI is disabled	Reference Data Type
lp_d0_tx_en_i		Available in DSI mode and CIL Bypass is checked	Active high Enables low power transmit back to the DSI host. Data lane 0 goes out of differential mode and switch to low power signaling.
lp_d0_tx_p_i		Available in DSI mode and CIL Bypass is checked	This is the transmit value for the low power data lane 0 p-channel.
lp_d0_tx_n_i		Available in DSI mode and CIL Bypass is checked	This is the transmit value for the low power data lane 0 n-channel.
sync_rst_i		—	Active high, synchronized reset
sync_clk_i	In	—	Low speed or oscillator clock
ready_o	Out	—	Indicates the state of gddr_sync
pll_lock_i	in	—	PLL lock indicator, if a PLL is used to generate a free-running byte clock. Set this to 1 if a PLL is not used. This is also used to reset rx_fifo and connected to start_i pin of the gddr_sync.
reset_n_i	In	—	Active low asynchronous system reset.
clk_lp_ctrl_i	In	—	Clocks the logic that detects the Rx D-PHY clock lane LP<->HS transitions. The frequency of this clock should be at least twice the low-power clock frequency of the Rx D-PHY clock, that is clock period of clk_lp_ctrl_i should at most be a half of TLPX to properly sample the LP to HS clock lane transitions. No need to drive this clock if the Rx clock mode is HS_ONLY.

Port Name	Direction	Mode/Configuration	Description
clk_byte_fr_i	In	—	Continuously running byte clock. This should be div8 (in gear16) or div4 (in gear8) of the input D-PHY clock. This also clocks the logic that detects the Rx D-PHY data lane transitions (lp_hs_ctrl_d0-3 modules). This is also used by the word_align, lane_align and capture_control modules. Payload output is also in this clock domain.
reset_lp_n_i	in	—	Low asserted reset for the nets in the clk_lp_hs_ctrl clock domain. The signal driving this port must already be synchronized to the clk_lp_hs_ctrl.
reset_byte_n_i	in	—	Low asserted reset for the logic clocked by the clk_byte_o.
reset_byte_fr_n_i	in	—	Low asserted reset for the nets in the clk_byte_fr clock domain. The signal driving this port must already be synchronized to the clk_byte_fr.
pd_dphy_i	in	--	This powers down the hardened D-PHY block. This can be used as a high asserted hard reset of the hardened D-PHY block.
clk_p_io, clk_n_io	In/Out	—	MIPI D-PHY clock lane (positive and negative signals)
d_p_io[*BUS_WIDTH* – 1:0], d_n_io[*BUS_WIDTH* – 1:0]	In/Out	—	MIPI D-PHY data lanes
lp_p_rx_o[*BUS_WIDTH* – 1:0], lp_n_rx_o[*BUS_WIDTH* – 1:0]	Out	—	Low-power data lanes
bd_o[31:0]	Out	Available, when Enable Packet Parser is checked	Valid only for Rx gear 8 This is the D-PHY byte data.
clk_byte_o	Out	—	Generated byte clock from the D-PHY module based on the input D-PHY clock lane, used to latch the internal parallel byte data from dphy_rx_wrap. This is div4 or div8 of the D-PHY clock lane frequency. This is only active when the data lanes are in high-speed mode.
clk_byte_hs_o	Out	—	Generated byte clock from the D-PHY module based on the input D-PHY clock lane, active only when the clock lanes are in high-speed mode. This clock is the same as the clk_byte_o when the D-PHY implementation is Soft D-PHY.
hs_sync_o	Out	—	This indicates the successful detection of the synchronization code ‘B8 in the data lanes. This signal asserts from the start of synchronization pattern ‘B8 up to the last data captured before detecting LP-11 state (of any lane, if Soft D-PHY; of data lane0 for Hard D-PHY).
payload_en_o	Out	Available, when Enable Packet Parser is checked	This signifies the arrival of valid payload data without the CRC
payload_o[dw-1:0]	Out	Available, when Enable Packet Parser is checked	This is the payload of a long packet, excluding the CRC bits, arranged the way it is received in the data lanes. The width of this bus is the number of gear bits multiplied by the number of lanes (RX_GEAR*NUMBER_OF_LANE).
dt_o[5:0]	Out	Available, when Enable Packet Parser is checked	CSI-2 or DSI 6-bit data type field.
vc_o[1:0]	Out	Available, when Enable Packet Parser is checked	2-bit virtual channel ID of the packet.
wc_o[15:0]	Out	Available, when Enable Packet Parser is checked	16-bit Word Count field. This denotes the number of bytes in the payload of a long packet. In a short packet, this contains a 2-byte data. Enabled when packet formatter is valid.

Port Name	Direction	Mode/Configuration	Description
ecc_o[7:0]	Out	Available, when Enable Packet Parser is checked	This is the received 8-bit error correction code (ECC). The submodule does not detect or correct any ECC errors.
dt2_o[5:0]	Out	Available, when Enable Packet Parser is checked	Same as dt_o but only if NUM_RX_LANE* RX_GEAR == 64
vc2_o[1:0]	Out	Available, when Enable Packet Parser is checked	Same as vc_o but only if NUM_RX_LANE* RX_GEAR == 64
wc2_o[15:0]	Out	Available, when Enable Packet Parser is checked	Same as vc_o but only if NUM_RX_LANE* RX_GEAR == 64
ecc2_o	Out	Available, when Enable Packet Parser is checked	Same as vc_o but only if NUM_RX_LANE* RX_GEAR == 64
bd0_o[rx_gear-1:0]	Out	Available, when Enable Packet Parser is unchecked	Parallel data from lane 0 This is 8-bit wide if the design is configured as gear8, or 16-bit wide if gearing is 16.
bd1_o[rx_gear-1:0]	Out	Available, when Enable Packet Parser is unchecked	Parallel data from lane 1 This is 8-bit wide if the design is configured as gear8, or 16-bit wide if gearing is 16.
bd2_o[rx_gear-1:0]	Out	Available, when Enable Packet Parser is unchecked	Parallel data from lane 2 This is 8-bit wide if the design is configured as gear8, or 16-bit wide if gearing is 16.
bd3_o[rx_gear-1:0]	Out	Available, when Enable Packet Parser is unchecked	Parallel data from lane 3 This is 8-bit wide if the design is configured as gear8, or 16-bit wide if gearing is 16.
capture_en_o	Out	Available, when Enable Packet Parser is unchecked	This functions as a valid signal for bd0_o to bd3_o. This is enabled from the start of synchronization pattern ‘B8 up to the last data captured before detecting LP-11 state (of any lane, if Soft D-PHY; of data lane0 for Hard D-PHY). This is the same as hs_sync_o.
skewcal_det_o	Out	Available when Enable Deskew Calibration Detection is enabled and CIL Bypass is checked or unchecked	Indicates that skew calibration burst is detected.
skewcal_done_o	Out	Available when Enable Deskew Calibration Detection is enabled and CIL Bypass is checked	Indicates that skew calibration of RX is done.
Miscellaneous Status Signals (available when Enable Miscellaneous Status is checked)			
term_clk_en_o	Out	—	Active-high enable signal for the line termination of the D-PHY clock lane. This is asserted on detection of transition from LP-11 to LP-01 of the clock lane, and de-asserts upon detection of LP-11 after a high-speed mode.
term_d_en_o[*NUM_LANES*-1:0]	Out	Depends on the number of lanes chosen	Active-high enable signal for the line termination of the D-PHY clock lane. This is asserted on detection of transition from LP-11 to LP-01 of the lanes, and de-asserts upon detection of LP-11 after a high-speed mode.
hs_d_en_o	Out	—	Active-high high-speed mode enable for data lane d0. For Hard D-PHY IP, this signal is also used for HS mode enable for the other data lanes.

Port Name	Direction	Mode/Configuration	Description
cd_d0_o	Out	—	Contention detection indicator on lane 0
cd_clk_o	Out	—	Contention detection indicator on clock lane
lp_hs_state_clk_o[1:0]	Out	—	2-bit state encoding of the D-PHY clock controller
lp_hs_state_d_o[1:0]	Out	—	2-bit state encoding of the D-PHY data lane 0 controller

***Notes:**

- *BUS_WIDTH* – Number of D-PHY Lanes, 1 to 4 (available on the user interface)
- N depends on configuration:
  - if *Parser = "OFF"*, then N = *NUM_Rx_LANES* * *RX_GEAR*
  - if *Parser = "ON"* AND *NUM_Rx_LANES* * *RX_GEAR* = 64, then N = *NUM_Rx_LANES* * *Rx_GEAR* + 64
  - if *Parser = "ON"* AND *NUM_Rx_LANES* * *RX_GEAR* != 64, then N = *NUM_Rx_LANES* * *Rx_GEAR* + 32

4. Attribute Summary

D-PHY Rx IP Attributes summary is shown in Table 4.1. All attributes can be configured from the General tab of the Lattice Radiant software user interface.

Table 4.1. Attributes Table

Attribute Name	Values	Default	Description
Receiver			
Rx Interface Type	“DSI”, “CSI-2”	“CSI-2”	D-PHY-Rx Interface Type
D-PHY RX IP	“Hard D-PHY”, “Soft D-PHY”	“Hard D-PHY”	Implementation of the PHY layer of the D-PHY Rx. For Certus-NX devices, only “Soft D-PHY” is available.
Number of RX Lanes	1, 2, 3, 4	4	Number of D-PHY-Rx high speed ports. 3-lane configuration is only available when the Packet Parser is disabled.
RX Gear	8, 16	8	Gearing ratio between the ports in fabric and the highspeed I/O. *RX Gear = 16* is available only on *D-PHY RX IP = ‘Hard D-PHY’*
CIL Bypass	’checked’, ‘unchecked’	‘checked’	When using *D-PHY RX IP = ‘Hard D-PHY’*, this option bypasses the built in Control Interface Logic of the Hard D-PHY. Control Interface Logic (CIL) is the hardened block that controls the clock and data lane state transitions. If the CIL is bypassed, then soft logic is used instead.
Enable LMMI Interface	’checked’, ‘unchecked’	‘unchecked’	Enables the LMMI bus
Enable AXI4-Stream Interface	’checked’, ‘unchecked’	‘checked’	Enables the AXI4-Stream bus
Enable Deskew Calibration Detection	’checked’, ‘unchecked’	‘unchecked’	This entry is available when data rate is less than 1.5 Gbps. This is automatically set to enabled (and grayed-out) at data rate more than 1.5 Gbps since this feature is compulsory for data rates more than 1.5 Gbps.
Clock			
RX Line Rate per Lane (Mbps)	160–2500	1000	Maximum bandwidth for *RX Gear = 16*
	80–1500	1000	Maximum bandwidth for *RX Gear = 8*
D-PHY Clock Frequency (MHz)	40–1250	500	Operating frequency of the PHY layer
D-PHY Clock Mode	“Continuous”, “Non-continuous”	“Non-Continuous”	Determines the clock mode of the PHY layer. The D-PHY protocol has an option for the clock lane to go to Low Power in between high speed transfers to reduce power consumption. If the mode selected is non-continuous, the control logic that detects the LP-to-HS and HS-to-LP sequence of the clock lane is enabled. Otherwise, the IP assumes the D-PHY clock lane is always in high speed mode.
Byte Clock Frequency (MHz)	10–187.5	125	Operating frequency of the byte_clock_o of the receiving end. Not editable, for information only.
Sync Clock Frequency (MHz)	24–200	60	Operating frequency of the components interfaced with the fabric

Attribute Name	Values	Default	Description
Timing Parameter			
Customize Data Settle Cycle	'checked', 'unchecked'	'unchecked'	Enables customization of the data settle parameter, when *CIL Bypass* is checked.
Data Settle Cycle	1–27	14	Value of the data settle parameter when *CIL Bypass* is checked.
Customize CIL Data Settle	'checked', 'unchecked'	'unchecked'	Enables customization of the data settle parameter, when *CIL Bypass* is unchecked.
CIL Data Settle Cycle	4 – 10	6	Value of the data settle parameter when *CIL Bypass* is unchecked.
Customize CIL Clock Settle	'checked', 'unchecked'	'unchecked'	Enables customization of the clock settle parameter, when *CIL Bypass* is unchecked.
CIL Clock Settle Cycle	4 – 19	9	Value of the clock settle parameter when *CIL Bypass* is unchecked.
Output			
Enable Packet Parser	'checked', 'unchecked'	'unchecked'	Enables or disables the packet parser function. When the packet parser is enabled, the IP reads through the contents of the packet header and convert them into CSI-2 or DSI related bus/signal outputs. When this is disabled, the deserialized data are sent out without analyzing its contents.
Miscellaneous			
Enable Miscellaneous Status Signals	'checked', 'unchecked'	'unchecked'	Enables or disables the miscellaneous status signals. When enabled, select internal signals such as high speed termination enables are made available to the top level IP wrapper. This may be used for debugging purposes.
Soft IP Implementation Settings			
Enable Lane Aligner Module	'checked', 'unchecked'	'unchecked'	Enables the line Alignment feature, this feature is available when *D-PHY RX IP = "Soft D-PHY"*
RX_FIFO			
RX_FIFO Enable	'checked', 'unchecked'	'checked'	Enables or disables the RX fifo function. When enabled, the FIFO after the PHY may be customized. Otherwise, a 4-register deep buffer is used. When using D-PHY RX IP = *Hard-D-PHY*, this option cannot be disabled.
Implementation	"EBR","LUT"	"EBR"	Selects the memory implementation of the FIFO. This feature is available when *RX_FIFO Enable* is checked.
Depth	16, 32, 64, 128, 256, 512, 1024, 2048, 4096	128	Selects the memory depth of the FIFO. This feature is available when *RX_FIFO Enable* is checked.
Number of Queue Entries	int	2	Determines the amount of Queue Entries available for the RX_FIFO. This option is editable when *Type = "QUEUE"* and *RX_FIFO* is checked.
Type	"PINGPONG", "QUEUE", "SINGLE"	"PINGPONG"	Type of the FIFO implemented. This feature is available when *RX_FIFO Enable* is checked.
Packet Delay (ns)	0–1023	3	Determines the amount of delay of the RX_FIFO, this value is editable when *Type = "PINGPONG" or Type = "SINGLE"* and *RX_FIFO* is checked. When this parameter is set to 0, the entire hs-transaction is buffered before FIFO is read, including the trail bits. For soft D-PHY, this includes the hs-zero bits. Otherwise, it uses delay counter (1–1023) before FIFO is read.
Counter Width (ns)	1–12	12	Determines the width of the Queue. This value is editable when *Type = "QUEUE"* and *RX_FIFO* is checked.

Attribute Name	Values	Default	Description
Clock Mode	“SC”,”DC”	“DC”	Determines if the FIFO would be implemented in Single Clock and Dual Clock. This value is editable when *Type = “SINGLE”* and *RX_FIFO* is checked. The clock mode is always *“DC” w*hen *D-PHY RX IP = “Hard D-PHY”*.
Misc Signals	’checked’, ‘unchecked’	‘unchecked’	Enables or disables the Miscellaneous Signals. This value is editable when *RX_FIFO* is checked.

5. Internal Registers

All registers listed Table 5.1 and Table 5.2 are accessible through LMMI.

5.1. General Configuration Registers

Table 5.1. General Configuration Registers

Offset (6 bits)	Access Type	Register Name	Description
Always Available			
0x31	R	VC_DT_ADDR	Virtual channel and Data type register address
0x32	R	WCL_ADDR	Word count low register address
0x33	R	WCH_ADDR	Word count high register address
0x34	R	ECC_ADDR	ECC register address
Available for *Gear x16* and *NUM_RX_LANE x4*			
0x35	R	VC_DT2_ADDR	Virtual channel and Data type 2 register address
0x36	R	WC2L_ADDR	Word count 2 low register address
0x37	R	WC2H_ADDR	Word count 2 high register address
0x38	R	ECC2_ADDR	ECC 2 register address
0x39	W	REFDT_ADDR	Reference data type

5.2. Hard D-PHY Configuration Registers/Bits for Hard MIPI D-PHY IP

Table 5.2. Configuration Registers (MIPI Programmable Bits)

ADDR [5:0]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x00	HSEL RX High Speed Select. [0] – Less than <=1.5Gbps [1] – Higher than 1.5Gbps	AUTO_PD_EN Powers down inactive lanes. [0] – lanes are kept powered up and at LP11. [1] – lanes powered down.	MASTER_SLAVE Selects the PHY IP Configuration. [0] – Slave [1] – Master	DSI_CSI Selects the PHY IP Application. [0] – CSI2 [1] – DSI
0x01	RXCDRP[1:0] LP-CD threshold voltage. Default is 2'b01. Min – 200mV, Max – 450mV		00*	
0x02	EN_CIL Enables or disables CIL. [0] – CIL Bypassed. [1] – CIL Enabled	RXLPRP[2:0] Adjust the threshold voltage and hysteresis of LP-RX, default setting 2'b001		
0x03	010*			DESKEW_EN Enables Deskew feature affects ERRSYNC/NOSYNC. [0] – Deskew Disabled [1] – Deskew Enabled
0x09	Lane0_sel[0] *(See MSB below)*	RxDataWidthHS[1:0] High-Speed Receive Data Width Select. 2'b00 – 1/8 the HS bit rate 2'b01 – 1/16 the HS bit rate 2'b10 – 1/32 the HS bit rate		0*
0x0A	uc_PRG_RXHS_SETTLE[0] *(See MSB below)*	cfg_num_lanes[1:0] Sets the number of active lanes. Value from 0 to 3		Lane0_sel[1] This determines which lane acts as data lane0 in HS Operation mode. Value from 0 to 3.

ADDR [5:0]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x0B	uc_PRG_RXHS_SETTLE[4:1] Bits used to program T_HS_SETTLE. For *clock* pin. *T_HS_SETTLE* = (*uc_PRG_RXHS_SETTLE* + 1) * (Tperiod of sync_clk_i)			
0x0C	000*			uc_PRG_RXHS_SETTLE[5] *(See LSB above)*
0x0F	u_PRG_RXHS_SETTLE[1:0] *(See MSB below)*		00*	
0x10	u_PRG_RXHS_SETTLE[5:2] Bits used to program T_HS_SETTLE. For *data* pins. *T_HS_SETTLE* = (*uc_PRG_RXHS_SETTLE* + 1) * (Tperiod of sync_clk_i)			
0x14	TEST_ENBL[1:0] *(See MSB above)*		00*	
0x15	TEST_ENBL[5:2] Six-bit signal that enables the testing modes.			
0x16	TEST_PATTERN[3:0]			
0x17	TEST_PATTERN[7:4]			
0x18	TEST_PATTERN[11:8]			
0x19	TEST_PATTERN[15:12]			
0x1A	TEST_PATTERN[19:16]			
0x1B	TEST_PATTERN[23:20]			
0x1C	TEST_PATTERN[27:24]			
0x1D	TEST_PATTERN[31:28] TEST_PATTERN[31:0] is the programmable pattern used by BIST pattern generator and pattern matcher.			
0x1E	000*			cont_clk_mode Enables the slave clock lane to maintain HS reception state during continuous clock mode operation. [0] – Disabled [1] – Enabled

*__Note__: These bits must be set to the indicated value when writing to this register. Otherwise, the IP may malfunction.

6. Core Generation, Simulation, and Validation

This chapter provides information on how to generate and synthesize D-PHY Rx IP Core using Lattice Radiant software, as well as on how to run simulation. For more on Radiant software, refer to the Lattice Radiant Software User Guide and relevant Lattice tutorials.

6.1. Generation and Synthesis

Lattice Radiant software allows you to generate and customize modules and IPs and integrate them into the device architecture.

To generate D-PHY Rx IP Core in Lattice Radiant software:

1. In the **Module/IP Block Wizard**, create a new Lattice Radiant software project for the D-PHY Rx module.
2. In the dialog box of the **Module/IP Block Wizard** window, configure D-PHY Rx module according to custom specifications, using drop-down menus and check boxes. As a sample configuration, see Figure 6.1. For configuration options, see Table 4.1.

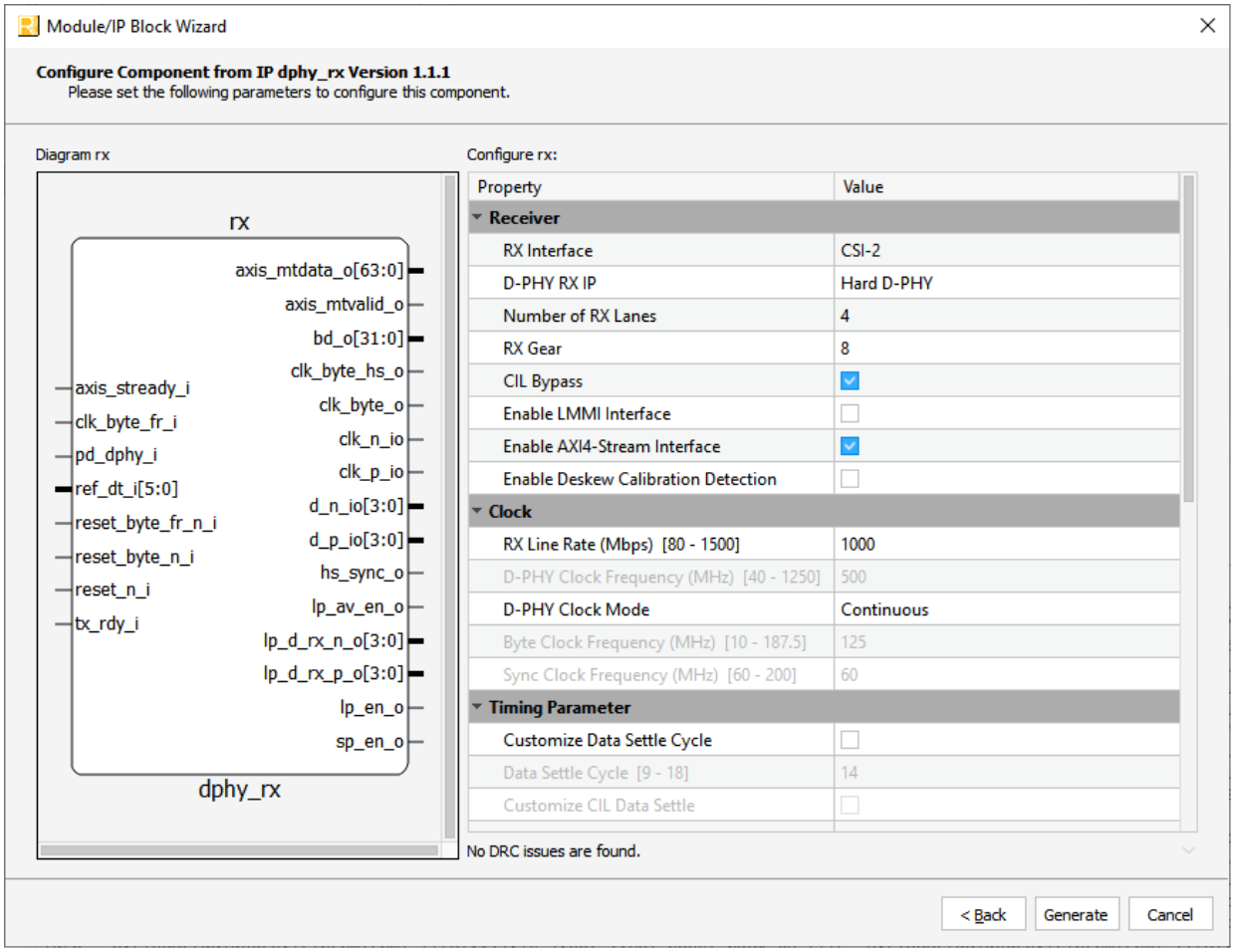

Figure 6.1. Configure Block of D-PHY Rx

3. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results as shown in Figure 6.2.

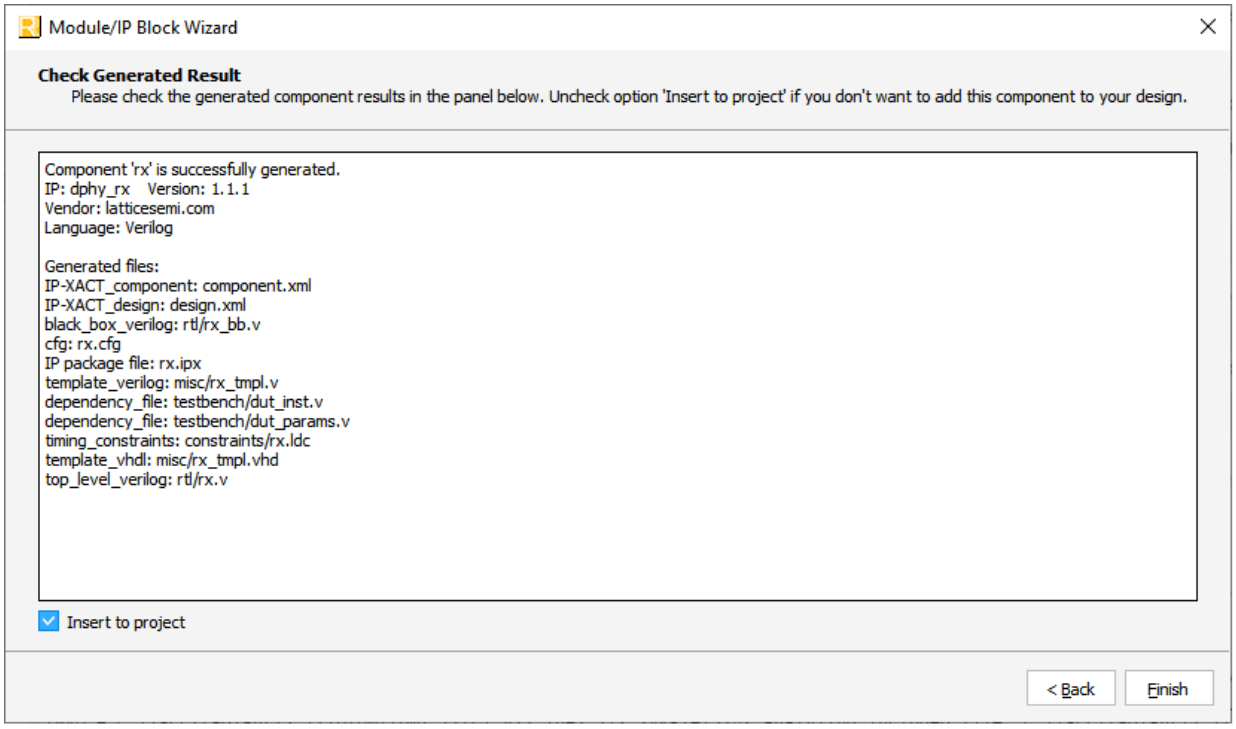

Figure 6.2. Check Generating Result

4. Click the **Finish** button to generate the Verilog file.

   Upon generating desired design, you can synthesize it by clicking **Synthesize Design** located at the top left corner of the screen, as shown in Figure 6.3.

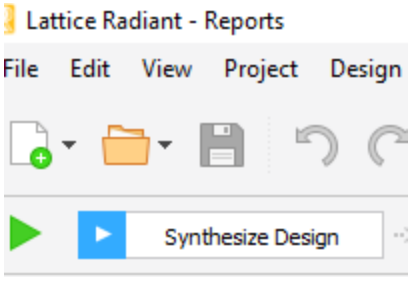

Figure 6.3. Synthesizing Design

6.2. Functional Simulation

To run Verilog simulation:

1. Right-click on the active implementation (*impl_1* by default), then click **Add > Existing Simulation File**, select *tb_top.v* located in *<ip_name>/testbench/*.
2. Click the  button located on the **Toolbar** to initiate the Simulation Wizard shown in Figure 6.4.

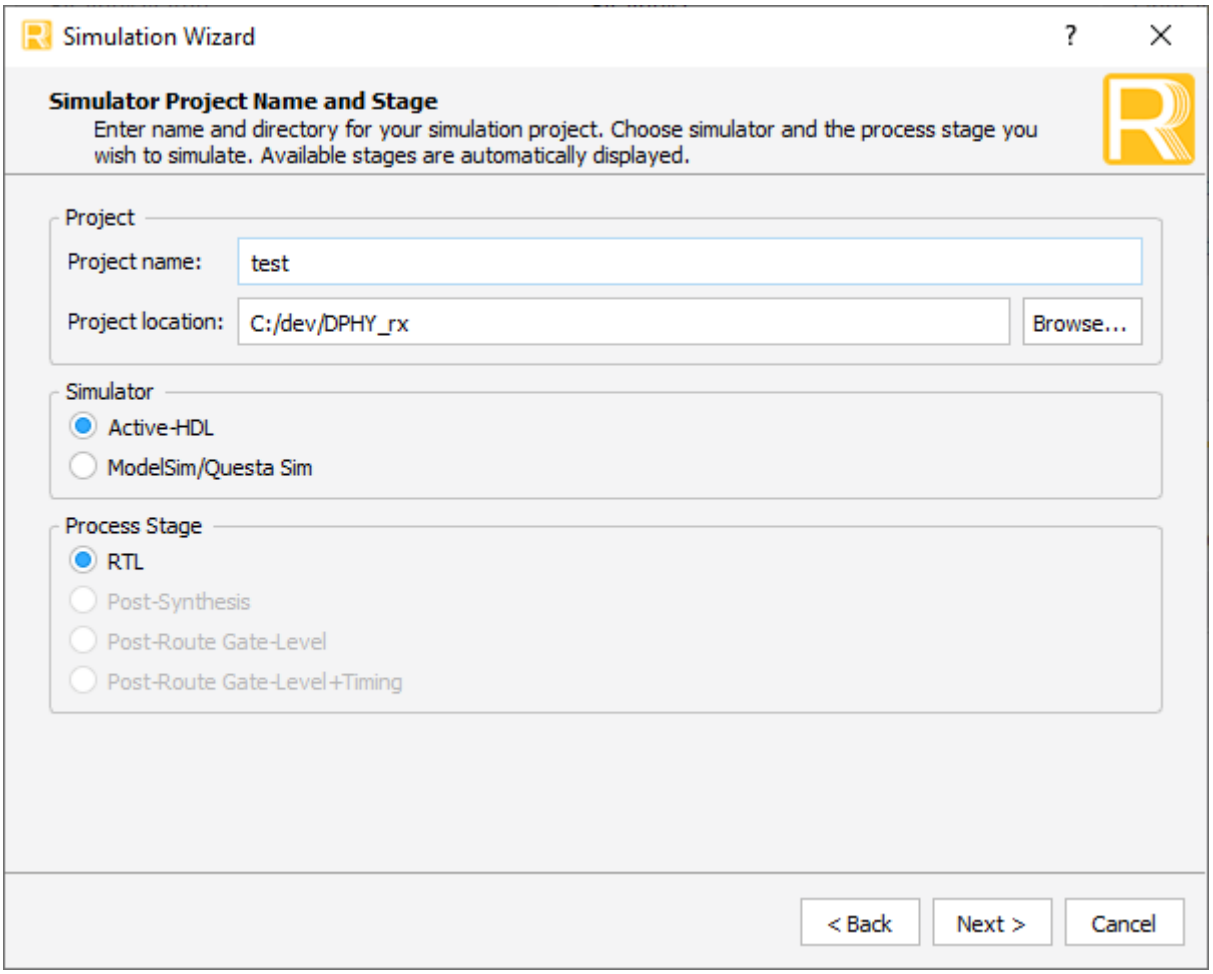

Figure 6.4. Simulation Wizard

3. Double-click **Next** to open the **Add and Reorder Source** window as shown in Figure 6.5.

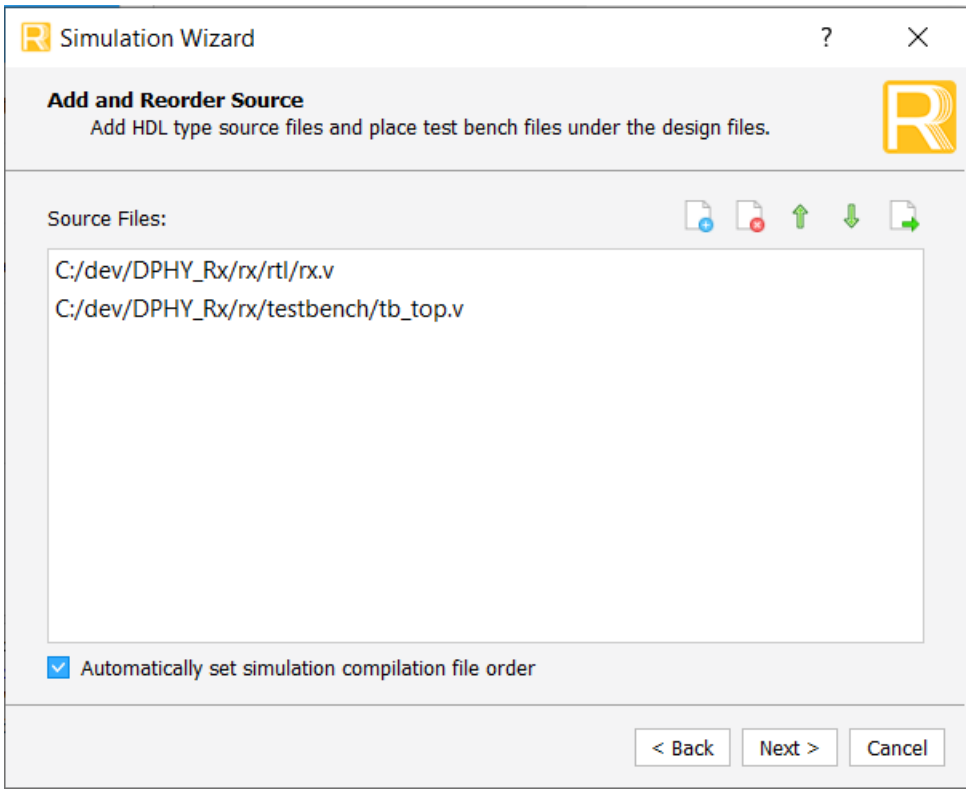

Figure 6.5. Adding and Reordering Source

4. Click **Next** to run simulation.

6.3. Core Validation

The functionality of the D-PHY Rx IP core is verified through simulation using Lattice's in-house testbench environment and hardware validation.

7. Licensing and Evaluation

7.1. Licensing the IP

An IP core-specific license string is required fully enable the CSI/DSI D-PHY-Rx IP Core in a complete, top-level design. In CrossLink-NX and Certus-NX devices, you can fully evaluate the IP core through functional simulation and implementation (synthesis, map, place, and route) without an IP license string. This IP core supports Lattice's IP hardware evaluation capability, which makes it possible to create versions of the IP core, and evaluate in the device for a limited time (approximately four hours) without the need of an IP license string. See Hardware Evaluation section for further details. A license string is required to enable timing simulation, and generation of the bitstream file, not limited by the hardware timeout.

7.2. Hardware Evaluation

There is no restriction on the hardware evaluation of this IP core.

8. Ordering Part Number

The Ordering Part Number (OPN) for this IP Core are the following:

- D-PHY-RX-CNX-U – CSI-2/DSI D-PHY Receiver for CrossLink-NX - Single Design License
- D-PHY-RX-CNX-UT – CSI-2/DSI D-PHY Receiver for CrossLink-NX - Site License
- D-PHY-RX-CTNX-U – CSI-2/DSI D-PHY Receiver for Certus-NX - Single Design License
- D-PHY-RX-CTNX-UT – CSI-2/DSI D-PHY Receiver for Certus-NX - Site License

Appendix A. Resource Utilization

Table A.1 and Table A.2 show the maximum frequency and resource utilization for a certain IP configuration.

Table A.1. Device and Tool Tested

	Value
Diamond Software Version	Radiant 2.1 production build
Device Used	LIFCL-40-BCG400
Performance Grade	9_High-Performance_1.0V
Synthesis Tool	Synplify Pro (R) Q-2020.03LR, Build 134R, May 8 2020

Table A.2. Resource Utilization[1]

Lane (Gear)	RX Interface Type	IP Type	Bit Rate (Lane)	Parser	AXI Bus	LMMI bus	Registers	LUT[2]	EBR	High Speed I/O resources
4(8)	CSI-2	Hard D-PHY[4]	1000 Mbps	EN	EN	DIS	629	699	2	1 x Hard D-PHY
4(8)	CSI-2	Soft D-PHY	1000 Mbps	EN	EN	DIS	706	1212	2	4 x IDDRX4, 1 x ECLKDIV, 1 x ECLKSYNC
4(16)[3]	CSI-2	Hard D-PHY[4]	2500 Mbps	EN	EN	DIS	852	991	4	1 x Hard D-PHY
4(8)[3]	CSI-2	Soft D-PHY	1500 Mbps	EN	EN	DIS	706	1270	2	4 x IDDRX4, 1 x ECLKDIV, 1 x ECLKSYNC
4(16)	DSI	Hard D-PHY[4]	2000 Mbps	EN	EN	EN	1006	1520	4	1 x Hard D-PHY
4(16)	DSI	Hard D-PHY[5]	2000 Mbps	EN	EN	EN	1006	1520	4	1 x Hard D-PHY
4(8)	DSI	Hard D-PHY[4]	1200 Mbps	EN	EN	DIS	682	843	2	1 x Hard D-PHY
2 (8)	DSI	Hard D-PHY[4]	800 Mbps	EN	DIS	DIS	448	566	2	1 x Hard D-PHY
4(16)[3]	CSI-2	Hard D-PHY[4]	2500 Mbps	EN	EN	EN	870	1041	4	1 x Hard D-PHY
4(8)[3]	CSI-2	Hard D-PHY[4]	1500 Mbps	EN	DIS	EN	585	747	2	1 x Hard D-PHY
2(8)	CSI-2	Hard D-PHY[4]	800 Mbps	EN	DIS	DIS	447	554	2	1 x Hard D-PHY

Notes:

1. All other settings are default.
2. The *distributed RAM* utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among *logic*, *distributed RAM*, and *ripple logic*.
3. Data Settle settings were changed in these configurations to match their target Bit Rate per Lane.
4. Hard D-PHY – CIL Bypassed
5. Hard D-PHY – CIL Enabled

For more information regarding a specific configuration, you can generate the IP, run synthesis and MAP, and check the MAP reports for resource utilization.

References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Radiant Software User Guide.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.3, November 2020

Section	Change Summary

Introduction	• Updated Table 1.1. CSI-2/DSI D-PHY Rx IP Core Quick Facts.
	  • Updated Lattice Implementation.
	  • Updated reference to the Lattice Radiant Software User Guide.
	• Added support for optional periodic deskew detection to the Features section.

Functional Description	• Added contents to the RX_FIFO section. • Added skewcal_det_o and skewcal_done_o output ports to Figure 2.1, Figure 2.2, Figure 2.9, Figure 2.10, and Figure 2.12. • Updated Figure 2.6. • Updated heading to Word Aligner and Optional Lane Aligner. • Removed Figure 2.18.
Signal Description	• Added skewcal_det_o and skewcal_done_o output ports to Table 3.1. D-PHY Rx Port Description.
Attribute Summary	• Added Enable Deskew Calibration Detection to Table 4.1. Attributes Table.
Core Generation, Simulation, and Validation	• Updated reference to the Lattice Radiant Software User Guide • Updated Figure 6.1. Configure Block of D-PHY Rx. • Updated Figure 6.2. Check Generating Result.
References	Updated reference to the Lattice Radiant Software User Guide

Revision 1.2, August 2020

Section	Change Summary
Acronyms in This Document	Updated content.
Introduction	• Updated Table 1.1. • Updated content of Hard CSI-2/DSI D-PHY Rx IP Core Features and Soft CSI-2/DSI D-PHY Rx IP Core Features section.

Functional Description	• Updated content of D-PHY Rx Common Interface Wrapper, RX_FIFO, Global Operations Controller, Word Aligner and Optional Line Aligner, AXI4-Stream Device Master, and LMMI Device section.
	• Updated the following figures:
	  • Figure 2.1
	  • Figure 2.2
	  • Figure 2.9
	  • Figure 2.10
	  • Figure 2.12
	  • Figure 2.13
	  • Figure 2.14
	  • Figure 2.15
	  • Figure 2.16

Signal Description	Updated Table 3.1.
Attribute Summary	Updated Table 4.1..
Internal Registers	Updated Table 5.2.
Core Generation, Simulation, and Validation	Updated step 1 in Functional Simulation section.
Ordering Part Number	Updated section content.
Appendix A. Resource Utilization	Updated Table A.2.

Revision 1.1, February 2020

Section	Change Summary
Attribute Summary	Updated Table 4.1. Attributes Table.
Port Description	Updated Table 3.1. D-PHY Rx Port Description.
Functional Description	Added RX_FIFO section.

Revision 1.0, December 2019

Section	Change Summary
All	Initial release.

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