CSI-2/DSI D-PHY Tx IP Core - Lattice Radiant Software

User Guide

FPGA-IPUG-02080-1.3

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AXI	Advance eXtensible Interface
CSI-2	Camera Serial Interface-2
DSI	Digital Serial Interface
EoTP	End of Transmission Packet
FPGA	Field-Programmable Gate Array
LMMI	Lattice Memory Mapped Interface
LP	Low Power

1. Introduction

The Lattice Semiconductor CSI-2/DSI D-PHY Transmitter IP Core converts data bytes from a requestor to either DSI or CSI-2 data format for Lattice Semiconductor CrossLink™-NX and Certus™-NX family devices as indicated in the dark gray boxes in Figure 1.1.

The CSI-2/DSI D-PHY Transmitter Submodule IP is intended for use in applications that require a D-PHY transmitter in the FPGA logic.

This IP supports both high-speed and low power modes. The payload data uses the high-speed mode whereas the control and status information are sent in low power mode.

The number of D-PHY data lanes to be used for the transmission of data is configurable and supports 1, 2, 3, or 4 data lanes.

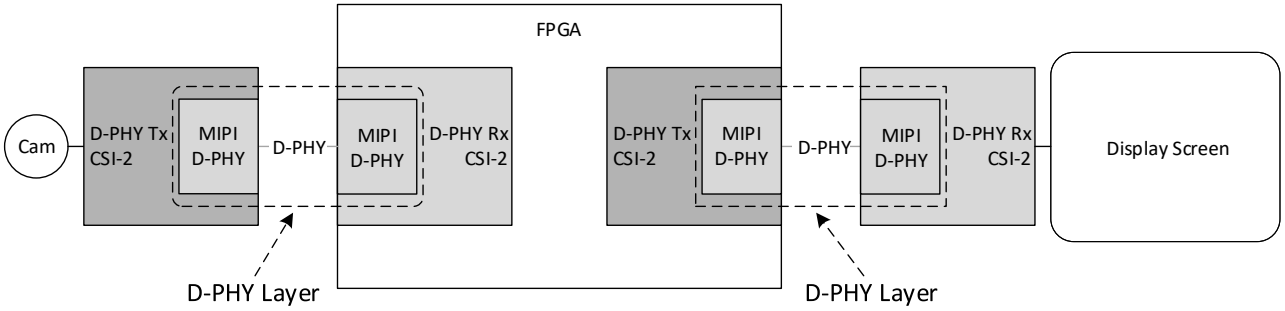

Figure 1.1 D-PHY Tx IP

1.1. Quick Facts

Table 1.1 presents a summary of the CSI-2/DSI DPHY Tx IP Core.

Table 1.1. CSI-2/DSI DPHY Tx IP Core Quick Facts

IP Requirements	Supported FPGA Families	CrossLink-NX, Certus-NX
Resource Utilization	Targeted Devices	LIFCL-40, LIFCL-17, LFD2NX-40
	Supported User Interfaces	LMMI/LINTR/AXI4-Stream Interface/ADC IP Core Native Interface
	Resource	See Table A.2. Resource Utilization1
Design Tool Support	Lattice Implementation	IP Core v1.0.x – Lattice Radiant® Software 2.0 IP Core v1.1.x – Lattice Radiant Software 2.1 or later
	Synthesis	Lattice Synthesis Engine (LSE)
		Synopsys® Synplify Pro® for Lattice
	Simulation	For a list of supported simulators, see the Lattice Radiant Software User Guide.

1.2. Features

- Compliant with MIPI D-PHY v2.1, MIPI DSI v1.3 and MIPI CSI-2 v1.2 Specifications.
- Supports MIPI DSI and MIPI CSI-2 interfacing up to 6 Gb/s for Soft D-PHY and up to 10 Gb/s for Hard D-PHY
- Supports 1, 2, 3, or 4 MIPI D-PHY data lanes
- Supports DSI burst mode and non-burst mode with sync events only
- Supports low-power (LP) mode during vertical and horizontal blanking
- Supports periodic deskew calibration
- Option for AXI4-Stream Interface
- Hard D-PHY is supported on Crosslink-NX devices only
- Soft D-PHY is supported on Crosslink-NX and Certus-NX devices.

1.2.1. Hard MIPI D-PHY Tx IP Core Features

- Maximum rate up to 2500 Mbps per lane
- Supported gearing: 8x, 16x
- Option to use the dedicated D-PHY TX PLL or an external clock source
- Internal PLL configurable through LMMI bus
- Option to bypass the Control and Interface Logic (CIL)
- Reference Frequency for the internal PLL from 24 MHz to 200 MHz
- Internal PLL output Frequency from 80 MHz to 1250 MHz

1.2.2. Soft MIPI D-PHY Tx IP Core Features

- Maximum rate up to 1500Mbps per lane
- Supported gearing: 8x
- External clock source

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal names that end with:

- *_n* are active low (asserted when value is logic 0)
- *_i* are input signals
- *_o* are output signals

2. Functional Description

The CSI-2/DSI D-PHY Transmitter IP Core consists of the Global Operation Module, the D-PHY Tx Wrapper Module, an optional Packet Formatter Module, an optional AXI4 Stream Device Slave, and an optional LMMI Slave Module. Figure 2.1 shows the D-PHY Tx IP block with both LMMI Device and AXI4 Stream Device enabled. Figure 2.2 shows the D-PHY Tx IP block with AXI4 Stream Device enabled and LMMI Device disabled. Figure 2.3 shows the D-PHY Tx IP block with AXI4 Stream Device disabled and LMMI Device enabled. Figure 2.4 shows the D-PHY Tx IP block with both AXI4 Stream Device and LMMI Device disabled.

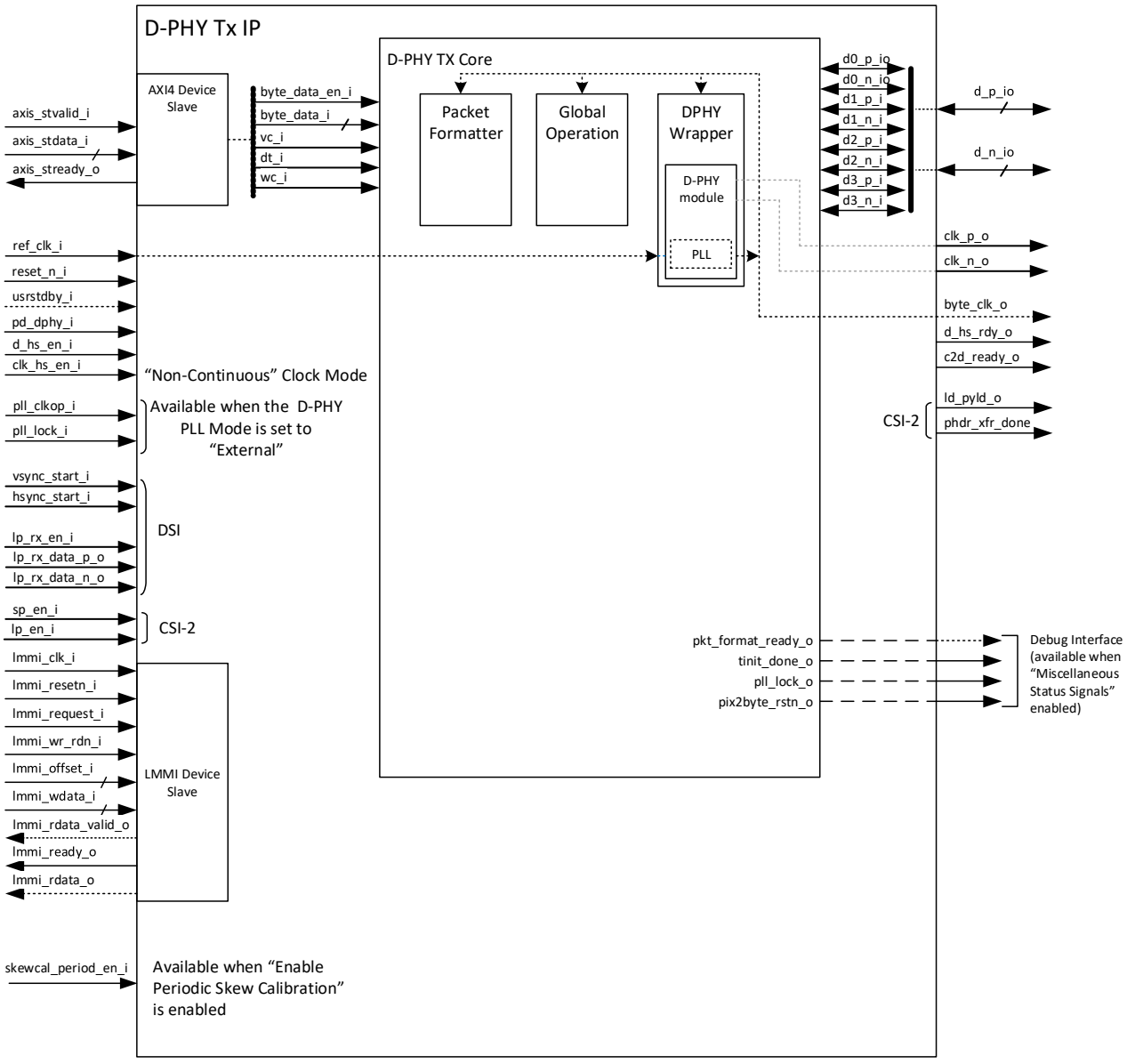

Figure 2.1. D-PHY Tx IP Block Diagram with Both AXI4-Stream and LMMI Enabled

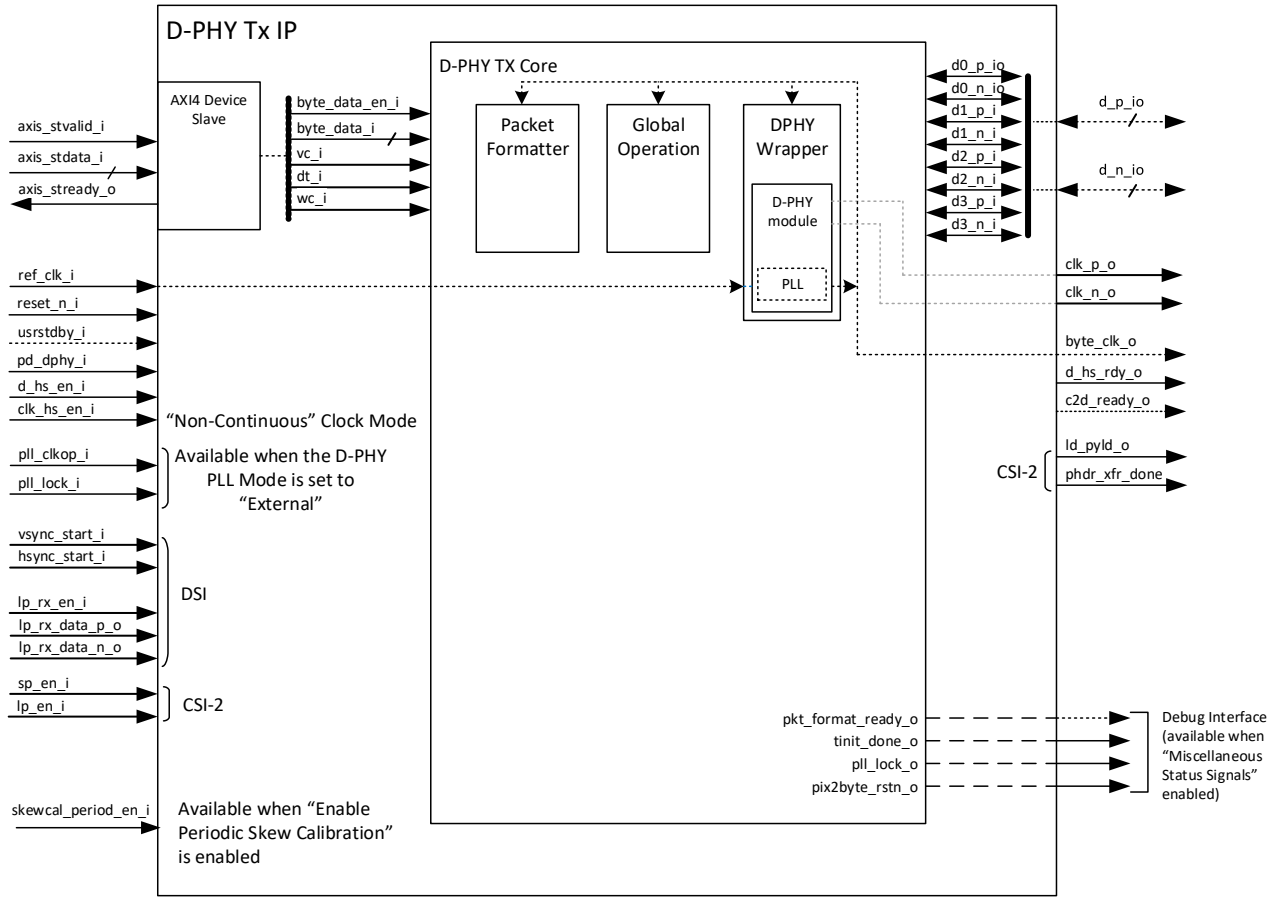

Figure 2.2. D-PHY Tx IP Block Diagram with AXI4-Stream Enabled and LMMI Disabled

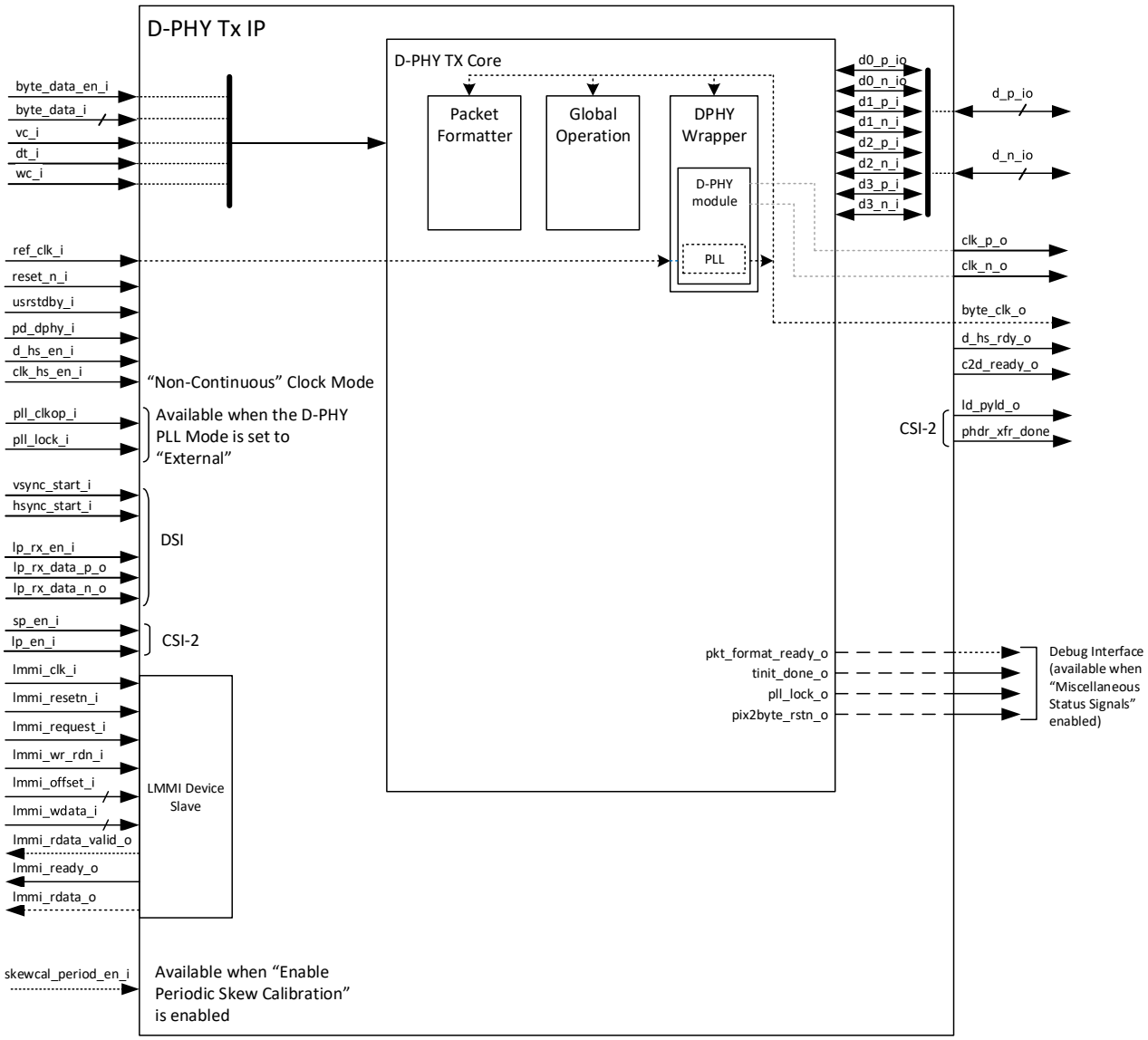

Figure 2.3. D-PHY Tx IP Block Diagram with AXI4-Stream Disabled and LMMI Enabled

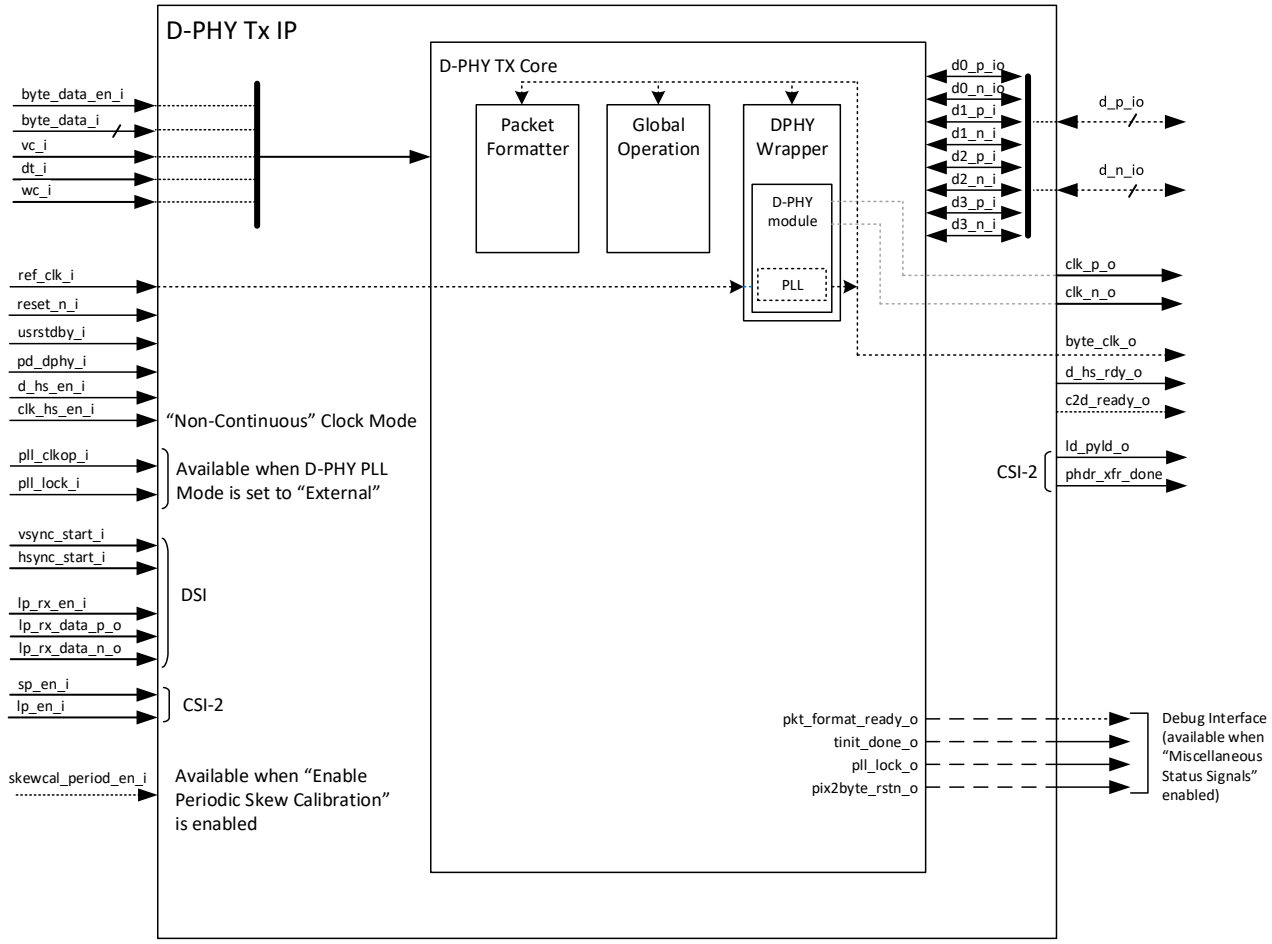

Figure 2.4. D-PHY Tx IP Block Diagram with Both AXI4-Stream and LMMI Disabled

2.1. Module Descriptions

2.1.1. Wrapper Module

The D-PHY Tx Wrapper Module instantiates the PHY block. It may be configured to instantiate either a hardened D-PHY block or a soft logic implementation of the MIPI D-PHY.

Additional logic in the Wrapper Module is used to configure the connection between the PHY and the higher protocol layers.

2.1.1.1. D-PHY Module

The D-PHY Module provides the MIPI D-PHY physical serial data communication layer on which the protocols CSI-2 or DSI runs. This may be a hardened block or a soft logic implementation of the D-PHY using special IOs.

When the hardened block is used, a dedicated D-PHY PLL may be used to generate the byte clock and the high-speed clock for the D-PHY clock lanes. This PLL may be reconfigured by accessing the hard D-PHY registers through the LMMI bus. If the LMMI is disabled, the PLL registers take on the value corresponding to the Reference Clock Frequency and the TX Line Rate per Lane attributes set in the user interface.

External PLL

When PLL Mode is External, two signals become available for users: pll_clkop_i and pll_lock_i. The pll_lock_i is a D-PHY PLL lock signal that is in effect a reset signal for D-PHY. The pll_clkop_i is an external clock source, which is generated by the user and must meet a few requirements, depending on whether the D-PHY is Soft or Hard. In case of Soft D-PHY, this clock must have the same frequency as DPHY Clock Frequency in the user interface. In case of Hard D-PHY, this clock must be exactly twice the DPHY Clock Frequency in the user interface. When the PLL Mode is External, the frequency can be changed by changing pll_clkop_i frequency while resetting pll_lock_i.

Internal PLL

The CSI-2/DSI D-PHY Transmitter IP contains its own PLL to generate the D-PHY clock lanes and the byteclock. The block diagram of the PLL is shown in Figure 2.5.

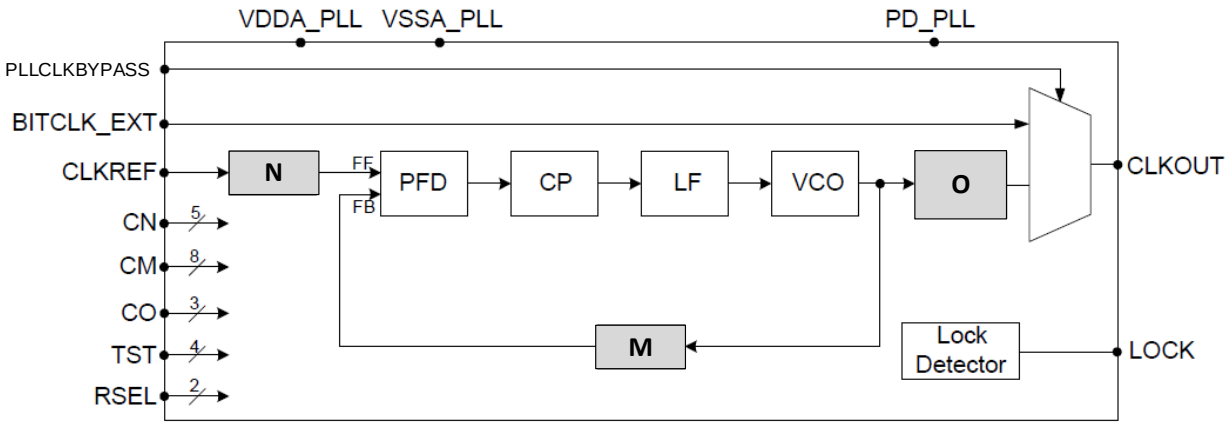

Figure 2.5. Internal PLL Block Diagram

The internal PLL multiplies the input frequency by (M/(N*O)), where N is the input divider, M is the feedback divider, and O is the output divider. The CLKOUT frequency is twice the D-PHY clock lane frequency.

The valid CLKREF of the D-PHY PLL, connected to the signal refclk_i, ranges from 24 MHz up to 200 MHz. The input divider, N, has to be programmed such that the frequency FF after the input divider is within 24 MHz and 50 MHz. The VCO output, which is also the input to the O divider, must be between 1250 MHz and 2500 MHz.

When PLL Mode is Internal, the frequency can be changed by reconfiguring the LMMI control registers CM, CN, CO, and the protocol timing parameters. See Table 2.4. for details on register offsets and corresponding values.

The data rate can be computed using this equation:

$$TX\ data\ rate = \left(\frac{CLKREF}{N}\right) * \left(\frac{M}{O}\right)$$

You can update the data rate without reprogramming the FPGA by following the steps below:

1. Set user standby input High. Keep it High at all time while registers CM, CN, and CO are written through LMMI write command.
2. Perform LMMI write command to the CM, CN, and CO register addresses with the values for the desired PLL frequency. See Table 2.5 and Table 2.6 for the conversion of the Control registers CM, CN, and CO to their respective M, N, and O values.
3. Adjust the protocol timing registers for the new data rate.
4. Set user standby input to Low.
5. Wait for the pll_lock_o to assert.

2.1.2. Packet Formatter Module

The Packet Formatter Module includes the Packet Header and Packet Footer modules.

The Packet Header module generates the 32-bit header, including the ECC, for the DSI or the CSI-2 packet based on the input information. For CSI-2 configured IP whose frame and line number information are not available, there is an internal line and frame counter logic than can be enabled through the IP user interface.

The Packet Footer module appends the CRC checksum at the end of the payload. It also generates the End-of-Transmit packet (EoTP) for DSI when it is enabled.

2.1.3. Global Operation Module

The Global Operation Module contains the FSM for controlling the HS and LP transitions for high-speed transmission. This also contains counters for the D-PHY protocol timing requirements. These timing parameters are also listed in Table 2.3.

Figure 2.6 shows the LP-to-HS transition flow diagram for data lanes.

Only the sequences from the Stop State to the high-speed state and vice versa are supported; the LP-request, escape mode and turnaround path are not supported.

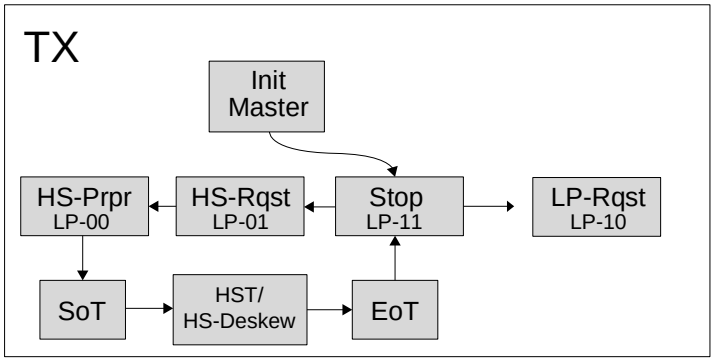

Figure 2.6. MIPI D-PHY Tx LP to HS Transition Flow Diagram on Data Lanes

During normal operation a Data Lane is either in Control or in High-Speed mode.

For sending payload data (the image data), the transmitter drives a particular sequence on data lanes to enter the receiver from the low power mode to high-speed mode.

As part of the initialization of D-PHY, initially all the lanes are held at LP11 state for a specified time. This LP11 state is also known as the Stop State. For sending the image data in high-speed, the transmitter drives the D-PHY lanes a particular LP sequence before it enters high-speed mode. The high-speed entry sequence (see Figure 2.7) consists of driving LP11->LP01->LP00 (LP->HS transition) on the lanes. On successful reception of this sequence, the high-speed receiver module enables its termination to receive the high-speed differential data.

After LP-to-HS transition, the transmitter sends HS Zeros (V(Dn)>V(Dp)) for a specified amount of time to make sure that the receiver is enabled properly before any payload data is transmitted.

Before the payload data of every HS burst on each lane, the transmitting D-PHY inserts a sync sequence (00011101). This sync sequence is used by the data lanes of the receiving D-PHY to establish synchronization with the high-speed payload data.

The LP11 state brings back the data lane from high-speed mode to low power mode.

After every HS burst, the data lanes go to LP11 state. A single HS burst represents the image data corresponding to one of the horizontal lines of an image and the LP11 state in-between the HS bursts represents the blanking periods.

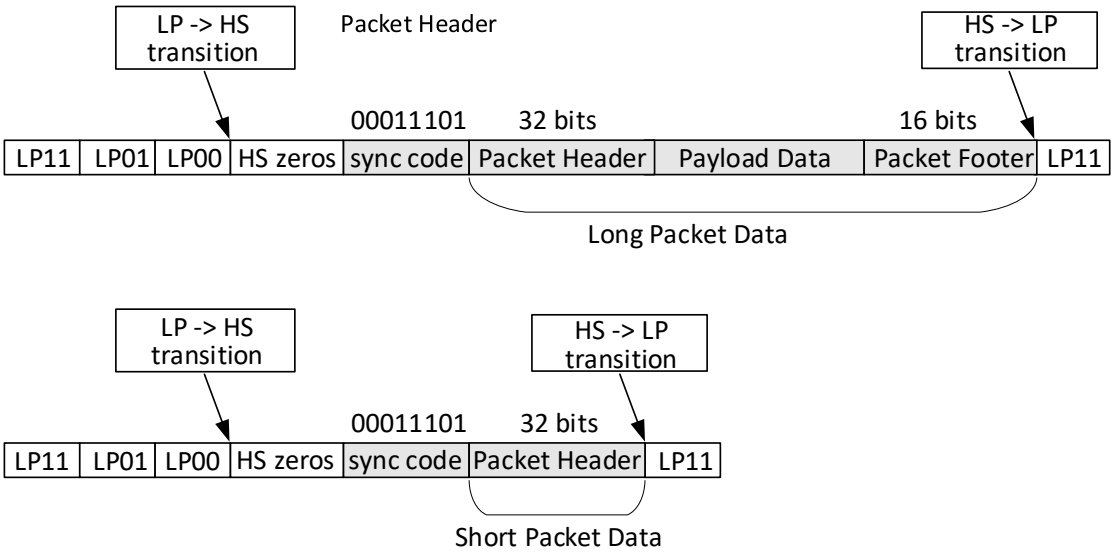

Figure 2.7. High-Speed Entry Sequence and Payload Data Transmission Cycle on Data Lanes

Receiver deskew is initiated by the transmitter for the DUTs supporting > 1.5 Gbps. The transmitter sends a special deskew burst, as shown in Figure 2.8. When operating above 1.5 Gbps or changing to any rate above 1.5 Gbps, an initial deskew sequence is transmitted before High-Speed Data Transmission in normal operation. When operating at or below 1.5 Gbps, the transmission of the initial deskew sequence is optional. Periodic deskew is optional irrespective of data rate.

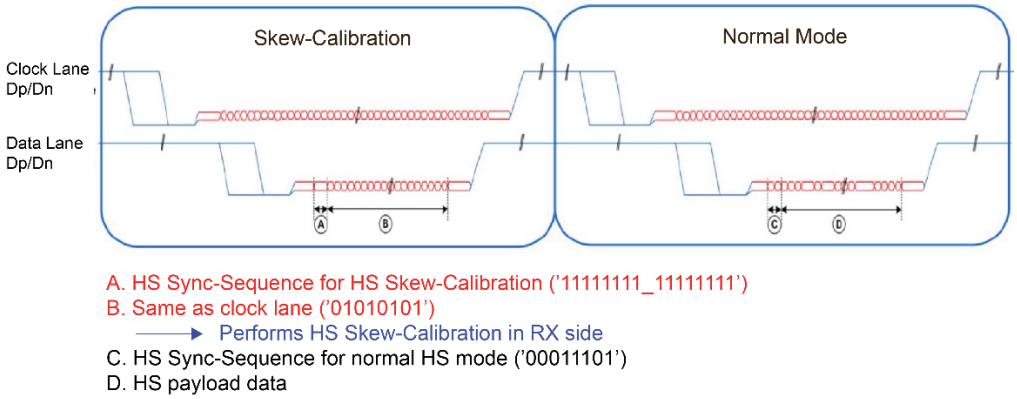

Figure 2.8. High-Speed Data Transmission in Skew Calibration

2.1.4. LMMI Device Slave

The LMMI (Lattice Memory Mapped Interface) Device Slave Module is used for configuring the control registers of the D-PHY Tx IP.

For more information on LMMI, see Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039).

If the LMMI bus is not enabled, the Hard D-PHY configuration registers take on the corresponding values based on the IP configuration set in the user interface. See the Internal Registers section for the list of the configuration registers.

An example of how the $T_{HS-TRAIL}$ Timing Parameter changes depending on u_PRG_HS_TRAIL[5:0] register is given in Table 2.1.

Table 2.1. High-Speed Trail Timer for Different Data Rates

Data Rate	Min (ns)	Max (ns)	u_PRG_HS_TRAIL [5:0]	THS-TRAIL (ns)
2.5 Gbps	61.6	109.8	011000	76.8
1.5 Gbps	62.67	113	001111	80
1.0 Gbps	64	117	001100	96
500 Mbps	68	129	000110	96
250 Mbps	79	153	000100	128
80 Mbps	110	255	000010	200

The other Timing Parameters can be changed by changing corresponding registers following the same logic.

2.2. Signal Description

Table 2.2 shows the D-PHY Tx IP Core top-level Input and Output signals.

Table 2.2. D-PHY Tx IP Core Signal Description

Port Name	Direction	Mode/Configuration	Description
LMMI			
lmmi_clk_i	In	—	LMMI Interface clock
lmmi_resetn_i	In	—	Active low signal to reset the configuration registers
lmmi_wdata_i[LDW[1] – 1:0]	In	—	Write data
lmmi_wr_rdn_i	In	—	Write = HIGH, Read = LOW
lmmi_offset_i[LOW[2] – 1:0]	In	—	Register offset, starting at offset 0
lmmi_request_i	In	—	Start transaction
lmmi_ready_o	Out	—	Ready to start a new transaction
lmmi_rdata_o[LDW[1] – 1:0]	Out	—	Read data
lmmi_rdata_valid_o	Out	—	lmmi_rdata[3:0] contains valid data
AXI4-Stream Slave			
axis_stvalid_i	In	—	Source indicates that data to be transmitted is valid
axis_stdata_i[ADW[3] – 1:0]	In	—	Payload data receiving channel (Byte Data or Packet Data with Virtual Channel and Data Type and Word Count)
axis_stready_o	Out	—	Indicates that AXI4-Stream is ready to accept the data
D-PHY Tx			
clk_p_io, clk_n_io	Out	—	MIPI D-PHY clock lane
d_p_io[BUS_WIDTH[4]– 1:0], d_n_io[BUS_WIDTH[4] – 1:0]	In/Out	—	MIPI D-PHY data lanes
ref_clk_i	In	—	If the PLL mode is internal, this is used as the reference clock for the internal PLL. The frequency must be between 24-200 MHz. If the PLL mode is external and the hardened CIL is enabled, this clock is used as the escape mode clock. In this case, the minimum frequency should be 60 MHz. If using the Soft PHY implementation, this clock is used to clock the gddr_sync primitive.
reset_n_i	In	—	Synchronous active low system reset
usrstdby_i	In	—	Active high puts the hard D-PHY block to standby mode
pd_dphy_i	In	D-PHY TX IP = "Hard D-PHY"	Active high powers down the hard D-PHY block, including the internal PLL
byte_or_pkt_data_i[DW[5] – 1:0]	In	AXI4 Stream - disabled	Byte data or Packet data
byte_or_pkt_data_en_i	In	AXI4 Stream - disabled	indicates valid data on the byte_or_pkt_data_i bus
vc_i [1:0]	In	AXI4 Stream - disabled Bypass Packet Formatter - unchecked	2-bit virtual channel ID of the packet This is used only when the Packet Formatter is enabled.
dt_i [5:0]	In	AXI4 Stream - disabled Bypass Packet Formatter - unchecked	CSI-2 or DSI 6-bit data type field This is used only when the Packet Formatter is enabled.
wc_i [15:0]	In	AXI4 Stream – disabled Bypass Packet Formatter - unchecked	16-bit Word Count field This denotes the number of bytes in the payload of a long packet. In a short packet, this contains a 2-byte data. This is used only when the Packet Formatter is enabled.

Port Name	Direction	Mode/Configuration	Description
clk_hs_en_i	In	DPHY Clock Mode – Non continuous	Active high pulse going to the Tx Global Operation This triggers the IP to start HS entry sequence on the clock lane. Enabled for non-continuous clock mode.
d_hs_en_i	In	—	Active high pulse going to the Tx Global Operation This triggers the IP to start HS entry sequence on the data lanes.
pll_clkop_i	In	DPHY PLL Mode - External	External PLL clock source For Hard PHY implementation, the frequency of this clock should be twice that of the D-PHY clock lanes. For Soft PHY, the frequency of this clock should be the same as the frequency of the D-PHY clock lanes.
pll_lock_i	In	DPHY PLL Mode - External	D-PHY PLL lock signal
sp_en_i	In	Tx Interface Type - CSI-2 Bypass Packet Formatter - unchecked	Short packet enable (frame or line packet) This high active pulse triggers the IP to transmit a CSI-2 short packet.
lp_en_i	In	Tx Interface Type - CSI-2 Bypass Packet Formatter - unchecked	This high active pulse is used to trigger the packet formatter to prepare the 32-bit packet header for the CSI-2 long packet. The IP expects the payload to arrive 4 cycles after the assertion of the lp_en_i.
vsync_start_i	In	Tx Interface Type - DSI Bypass Packet Formatter - unchecked	This high active pulse triggers the IP to transmit a vsync_start packet.
hsync_start_i	In	Tx Interface Type - DSI Bypass Packet Formatter - unchecked	This high active pulse triggers the IP to transmit an hsync_start packet.
lp_rx_en_i	In	Tx Interface Type - DSI	Low Power Rx Enable signal
lp_rx_data_p_o	Out	Tx Interface Type - DSI	Low Power Rx Positive data
lp_rx_data_n_o	Out	Tx Interface Type - DSI	Low Power Rx Negative data
d_hs_rdy_o	Out	—	Active high signal to indicate data lane is ready for transmission.
byte_clk_o	Out	—	Byte clock generated by D-PHY PLL.
c2d_ready_o	Out	—	Indicates that CMOS2DPHY is ready to receive data
phdr_xfr_done_o	Out	Tx Interface Type – CSI-2 Bypass Packet Formatter - unchecked	Single cycle pulse to indicate that the packet information, along with the payload and CRC, are sent out to the Tx Global Operation (available when PKT_FORMAT = ON).
ld_pyld_o	Out	Tx Interface Type – CSI-2 Bypass Packet Formatter - unchecked	When high, the packet formatter is ready to receive data for packing (available when PKT_FORMAT = ON).
skewcal_period_en_i	In	Enable Periodic Skew Calibration = ‘checked’	Initiates periodic deskew calibration when set from low to high.
Debug Interface			
tinit_done_o	Out	Miscellaneous – enabled	tINIT done signal generated from IP
pll_lock_o	Out	Miscellaneous – enabled	D-PHY PLL lock signal
pix2byte_rstn_o	Out	Miscellaneous – enabled Bypass Packet Formatter – unchecked Tx Interface Type – CSI-2	Resets signal for pixel2byte FIFOs

Port Name	Direction	Mode/Configuration	Description
pkt_format_ready_o	Out	Miscellaneous – enabled Bypass Packet Formatter – unchecked Tx Interface Type – CSI-2 AXI4 Stream – disabled	Indicates the state of Packet Formatter This is available when PKT_FORMAT = ON and AXI4 Stream = OFF and Tx Interface Type = CSI-2.

Notes:

1. LDW – LMMI Data Width
   - if CIL_BYPASS is unchecked, then LDW = 4
   - otherwise LDW = 8
2. LOW – LMMI Offset Width
   - if CIL_BYPASS is unchecked, then LOPW = 5
   - otherwise LOW = 7
3. ADW – AXI4 Stream Data Width
   - if (Bypass Packet Formatter is unchecked) AND (LMMI is unchecked) then ADW = GEAR * NUM_TX_LANE + 24
   - otherwise ADW = GEAR * NUM_TX_LANE
4. BUS_WIDTH – Number of D-PHY Lanes, 1 to 4 (available on the user interface)
5. DW – Byte or Packet Data Width
   DW = GEAR * NUM_TX_LANE

2.3. Attribute Summary

The D-PHY Tx IP attributes summary is shown in Table 2.3. All attributes can be configured from the General tab of the Lattice Radiant Software user interface.

Table 2.3. Attributes Table

Attribute Name	Values	Default	Description
General Settings			
Transmitter			
TX Interface Type	"DSI", "CSI-2"	"CSI-2"	DPHY-Tx Interface Type
D-PHY TX IP	"Hard D-PHY", "Soft D-PHY"	"Hard D-PHY"	Implementation of the PHY layer of the D-PHY Tx For Certus-NX devices, only *Soft D-PHY* is available.
Number of TX Lanes	1, 2, 3, 4	4	Number of active D-PHY Tx data lanes The 3-lane configuration is only available when *Bypass Packet Formatter* is unchecked.
TX Gear	8, 16	8	Gearing ratio between the ports in fabric and the high-speed I/O *TX Gear = 16* is available only on *D-PHY TX IP = 'Hard D-PHY'*.
Interleaved Input Data	'checked','unchecked'	'unchecked'	When this option is checked, the input parallel data is already interleaved across the lanes. See Table 3.1. Available only when *TX Gear = 16*.
CIL Bypass	'checked','unchecked'	'checked'	When using *D-PHY TX IP = Hard D-PHY*, this option bypasses the built in Control Interface Logic of the Hard D-PHY.
Bypass Packet Formatter	'checked','unchecked'	'unchecked'	Bypasses the Packet Formatter module. The data input to the IP should already be in packet format and the bytes are interleaved across the active data lanes. Editable only if *TX Interface Type = 'CSI-2'*.
Enable Frame Number Increment in Packet Formatter	'checked','unchecked'	'unchecked'	Enables the Frame Number Increment in the Packet Formatter Editable only if *Bypass Packet Formatter* is unchecked.
Frame Number MAX Value Increment in Packet Formatter	1–255	1	Maximum frame number used in packet formatter This option is editable only if *Enable Frame Number Increment in Packet Formatter* is checked.
Enable Line Number Increment in Packet Formatter	'checked','unchecked'	'unchecked'	Enables the line number increment feature for the Packet Formatter This option is editable only if *Bypass Packet Formatter* is unchecked.
EoTp Enable	'checked','unchecked'	'unchecked'	When checked, the IP appends an end-of-transmit packet at the end of a high-speed transmission. This option is enabled only if *TX Interface Type = 'DSI'*.
Enable LMMI Interface	'checked','unchecked'	'unchecked'	Enables the LMMI bus
Enable AXI4-Stream Interface	'checked','unchecked'	'unchecked'	Enables the AXI4-Stream bus
Enable Periodic Skew Calibration	'checked', 'unchecked'	'unchecked'	When this option is checked, there is an option to perform periodic skew calibration through the port 'skewcal_period_en_i'.

Attribute Name	Values	Default	Description
Clock			
Target TX Line Rate (Mbps per Lane)	160–2500	1000	Maximum bandwidth per lane for TX Gear = 16
	160–1500	1000	Maximum bandwidth per lane for TX Gear = 8
Target TX Data Rate (Mbps)	160–10000	4000	Target total bandwidth of the D-PHY TX channel. Not editable. For information only.
Target TX D-PHY Clock Frequency (MHz)	80–1250	1250	Target frequency of the D-PHY clock lane. Not editable. For information only.
Target TX Byte Clock Frequency (MHz)	10–187.5	125	Target operating frequency of the internal clock byte_clock_o. The value is (line_rate_per_lane / gearing) Not editable. For information only.
D-PHY Clock Mode	Continuous, Non-continuous	Non-Continuous	Determines the clock mode of the PHY layer Continuous – if the clock lane is always in high speed mode Non-continuous – the clock lane goes to low-power mode in between high speed transactions
D-PHY PLL Mode	“Internal”, “External”	“Internal”	Enables or disables the internal PLL when TX Interface = Hard D-PHY For Soft D-PHY, only external PLL sources are supported.
Reference Clock Frequency (MHz)	24–200	24	Operating frequency of the components interfaced with the fabric
Actual TX Data Rate (Mbps)	160–10000	4000	Actual D-PHY TX data rate based on the PLL settings and Reference Clock Frequency. Not editable. For information only.
Actual TX Line Rate (Mbps per Lane)	160–2500	1000	Actual data rate per lane based on the PLL settings and Reference Clock Frequency. Not editable. For information only.
Actual TX D-PHY Clock Frequency (MHz)	80–1250	1250	Actual D-PHY TX clock frequency based on the PLL settings and Reference Clock Frequency. Not editable. For information only.
Actual TX Byte Clock Frequency (MHz)	10–187.5	125	Actual operating frequency of the internal clock byte_clock_o. The inputs to the IP should be synchronized to this clock. Not editable. For information only.
Deviation from Target Data Rate	—	0	((target data rate - actual data rate)/ target data rate), in percent
Initialization			
tINIT Counter	‘checked’,’unchecked’	‘unchecked’	Enables the initialization counter
tINIT_SLAVE Value (Number of Byte Clock Cycles)	1–32768	1000	Maximum counter value; editable only if *tINIT Counter* is checked
tinit Value in ns	int	0	Equivalent value of *tINIT_SLAVE Value* in ns Not editable. For information only.

Attribute Name	Values	Default	Description
Miscellaneous Signals			
Enable Miscellaneous Status Signals	'checked','unchecked'	'unchecked'	Enables the other miscellaneous signals
Protocol Timing Parameters			
TX Global Operation Timing Parameters			
Customize TX Timing Parameter Values	'checked','unchecked'	'unchecked'	Enables customization of the timing parameters
t_LPX 50ns minimum	1–63	4	Duration of any Low-Power state
t_HS-PREPARE (40 ns + 4 UI) to (85 ns + 6 UI)	1–63	3	Duration of the LP-00 Line state before the HS-0 Line state
t_HS_ZERO (t_HS_PREPARE + t_HS_ZERO) >= (145 ns + 10 UI)	1–63	7	Delay from the LP-00 State to the assertion of the d_hs_rdy_o signal The actual HS-ZERO on the D-PHY data lanes still depend on these three factors: • The delay between the d_hs_rdy_o assertion and the time the requestor sends the payload of a long packet • The number of cycles the packet header (if enabled) can create the sync pattern and the 32-bit header. This varies with the number of lanes and gearing. • The serializer delay. The timing from parallel data input to the serialized output data differs between soft and hard D-PHY implementation.
t_HS_TRAIL	1–63	8	Duration of the flipped bit after the last payload data bit of an HS transmission burst
t_HS_EXIT 100 ns minimum	1–63	7	Duration of the data LP-11 state following an HS transmission burst
t_CLK-PREPARE 38 ns to 95 ns	1–63	3	Duration of the LP-00 clock state immediately before the HS-0 clock state in the LP-to-HS sequence
t_CLK-ZERO (t_CLK-PREPARE + t_CLK_ZERO) >= 300 ns	1–63	17	Duration of the clock HS-0 state prior to starting the actual toggling of the high-speed clock
t_CLK-PRE 8UI minimum	1–63	2	Duration of the HS clock prior to the start of the LP-to-HS sequence of the data lanes.
T_CLK_POST (60ns + 52UI) minimum	1–63	8	Duration of the HS clock after the last associated Data Lane has transitioned to LP Mode. The interval is defined as the period from the end of tHS-TRAIL to the beginning of tCLK-TRAIL.
t_CLK-TRAIL 60 ns minimum	1–63	19	Duration of the HS-0 state after the last clock bit of an HS transmission burst.
t_CLK-EXIT 100 ns minimum	1–63	32	Duration of the clock LP-11 state following an HS transmission burst
t_SKEWCAL-INIT	21^5 UI –100 us	1874	Duration of initial Skew Calibration
t_SKEWCAL-PERIOD	21^5 UI –100 us	1874	Duration of periodic Skew Calibration

Note: The duration of the timing parameter is equal to the (byteclock period) * (attribute value).

The timing parameters are in number of byteclock cycles. This is computed automatically to ensure the design meets the required minimum and maximum timing ranges. The numbers set in the user interface and the actual duration in the D-PHY lanes might vary due to the serialization and register delays within the design.

2.4. Internal Registers

For both hard and soft configurations of D-PHY Tx IP, the Configuration Registers are available when LMMI is enabled. All D-PHY Tx IP Configuration Registers are controlled through the LMMI bus. If the LMMI feature is not enabled, then the Hard D-PHY configuration registers (MIPI programmable bits) are set to their default values and the general registers become not actual and, instead, turn to top level input signals.

2.4.1. Hard Configured D-PHY Tx IP Configuration Registers (MIPI Programmable Bits)

(Available when *DPHY TX IP = Hard D-PHY*)

Table 2.4. Hard Configured D-PHY Tx Configuration Registers (MIPI Programmable Bits)

ADDR [5:0]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x00	HSEL RX High Speed Select. [0] – Less than <=1.5 Gbps [1] – Higher than 1.5 Gbps	AUTO_PD_EN Powers down inactive lanes. [0] – lanes are kept powered up and at LP11. [1] – lanes powered down.	MASTER_SLAVE Selects the PHY IP Configuration. [0] – Slave [1] – Master	DSI_CSI Selects the PHY IP Application. [0] – CSI2 [1] – DSI
0x01	RXCDRP[1:0] LP-CD threshold voltage. Default is 2'b01. Min – 200 mV, Max – 450 mV		2'b00*	
0x02	EN_CIL Enables or disables CIL. [0] – CIL Bypassed. [1] – CIL Enabled	RXLPRP[2:0] Adjust the threshold voltage and hysteresis of LP-RX, default setting 2'b001		
0x03	0*	PLLCLKBYPASS Bypasses the internal PLL. [0] – PLL Enabled. [1] – PLL Bypassed	LOCK_BYP When clock lane exits from ULPS, this input determines if the PLL LOCK signal is used to gate the TxWordClkHS [0] PLL LOCK gates TxWordClkHS. [1] PLL LOCK signal does not gate TxWordClkHS clock.	—
0x04	CN[0]	3'b000*		
0x05	CN[4:1] The N parameter of the internal PLL in the equation: Output = M/(N*O). See Table 2.5 for values.			
0x06	CM[3:0] LSB of the M parameter of the internal PLL in the equation: Output = M/(N*O). See Table 2.5 for values.			
0x07	CM[7:4] MSB of the M parameter of the internal PLL in the equation: Output = M/(N*O). See Table 2.5 for values.			
0x08	TxDataWidthHS[0] LSB High-Speed Transmit Byte Clock.	CO[2:0] The O parameter of the internal PLL in the equation: Output = M/(N*O). See Table 2.5 for values.		
0x09	Lane0_sel[0] LSB of Lane0_Sel	RxDataWidthHS[1:0] High-Speed Receive Data Width Select. 2'b00 – 1/8 the HS bit rate 2'b01 – 1/16 the HS bit rate 2'b10 – 1/32 the HS bit rate		TxDataWidthHS[1] MSB High-Speed Transmit Byte Clock. 2'b00 – 1/8 the HS bit rate 2'b01 – 1/16 the HS bit rate 2'b10 – 1/32 the HS bit rate

ADDR [5:0]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x0A	0*	cfg_num_lanes[1:0] Sets the number of active lanes Value from 0 to 3		Lane0_sel[1] MSB of Lane0_Sel. This determines which lane acts as data lane0 in HS Operation mode. Value from 0 to 3.
0x0C	uc_PRG_HS_ZERO[1:0]		uc_PRG_HS_PREPARE T_CLK_PREPARE time in the beginning of high-speed transmission mode. For clock pin. 0 – Tperiod of sync_clk_i 1 – 1.5*Tperiod of sync_clk_i	0*
0x0D	uc_PRG_HS_ZERO[5:2] Bits used to program T_CLK_ZERO time in the beginning of high-speed transmission mode. For clock pin. T_CLK_ZERO = (uc_PRG_HS_ZERO+ 4) * (ByteClk Period)			
0x0E	uc_PRG_HS_TRAIL[2:0] Bits used to program T_HS_TRAIL time in the end of high-speed transmission mode. For clock pin. T_HS_TRAIL = (uc_PRG_HS_TRAIL) * (ByteClk Period)			uc_PRG_HS_ZERO[6]
0x0F	2'b00*		uc_PRG_HS_TRAIL[4:3]	
0x11	u_PRG_HS_ZERO[1:0] *(See MSB below)*		u_PRG_HS_PREPARE[1:0] T_HS_PREPARE time in the beginning of high-speed transmission mode. For data pins. 0 – Tperiod of sync_clk_i 1 – 1.5*Tperiod of sync_clk_i 2 – 2*Tperiod of sync_clk_i 3 – 2.5*Tperiod of sync_clk_i	
0x12	u_PRG_HS_ZERO[5:2] Bits used to program T_HS_ZERO time in the beginning of high-speed transmission mode. For data pins. T_HS_ZERO =(u_PRG_HS_ZERO + 5 +2M) * (ByteClk Period), where M is the interface width: 0 – Single Interface 1 – Double Interface 2 – Quad Interface			
0x13	u_PRG_HS_TRAIL[3:0] Bits used to program T_HS_TRAIL time in the end of high-speed transmission mode. For clock pin. T_HS_TRAIL = (uc_PRG_HS_TRAIL) * (ByteClk Period)			
0x14	TEST_ENBL[1:0] *(See MSB above)*		u_PRG_HS_TRAIL[5:4] *(See LSB above)*	
0x15	TEST_ENBL[5:2] Six-bit signal that enables the testing modes.			
0x16	TEST_PATTERN[3:0]			
0x17	TEST_PATTERN[7:4]			
0x18	TEST_PATTERN[11:8]			
0x19	TEST_PATTERN[15:12]			
0x1A	TEST_PATTERN[19:16]			
0x1B	TEST_PATTERN[23:20]			
0x1C	TEST_PATTERN[27:24]			
0x1D	TEST_PATTERN[31:28] TEST_PATTERN[31:0] is the programmable pattern used by BIST pattern generator and pattern matcher.			

ADDR [5:0]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x1E	—	—	0*	cont_clk_mode enables the slave clock lane to maintain HS reception state during continuous clock mode operation. [0] – disabled [1] – enabled

***Note:** This bit must be tied to 0 when programming this register. Otherwise, the IP may malfunction.

Table 2.5. CN and CO Table of Values

CO		CN			
Control O Value	Actual O Value	Control N Value	Actual N Value	Control N Value	Actual N Value
000	1	11111	1	11010	17
001	2	00000	2	11101	18
010	4	10000	3	11110	19
011	8	11000	4	01111	20
111	16	11100	5	10111	21
—	—	01110	6	11011	22
—	—	00111	7	01101	23
—	—	10011	8	10110	24
—	—	01001	9	01011	25
—	—	00100	10	00101	26
—	—	00010	11	10010	27
—	—	10001	12	11001	28
—	—	01000	13	01100	29
—	—	10100	14	00110	30
—	—	01010	15	00011	31
—	—	10101	16	00001	32

Table 2.6. CM Table of Values

CM							
Control M Value	Actual M Value	Control M Value	Actual M Value	Control M Value	Actual M Value	Control M Value	Actual M Value
111X0000	16	10001100	76	00001000	136	01000100	196
111X0001	17	10001101	77	00001001	137	01000101	197
111X0010	18	10001110	78	00001010	138	01000110	198
111X0011	19	10001111	79	00001011	139	01000111	199
111X0100	20	10010000	80	00001100	140	01001000	200
111X0101	21	10010001	81	00001101	141	01001001	201
111X0110	22	10010010	82	00001110	142	01001010	202
111X0111	23	10010011	83	00001111	143	01001011	203
111X1000	24	10010100	84	00010000	144	01001100	204
111X1001	25	10010101	85	00010001	145	01001101	205
111X1010	26	10010110	86	00010010	146	01001110	206
111X1011	27	10010111	87	00010011	147	01001111	207
111X1100	28	10011000	88	00010100	148	01010000	208
111X1101	29	10011001	89	00010101	149	01010001	209
111X1110	30	10011010	90	00010110	150	01010010	210
111X1111	31	10011011	91	00010111	151	01010011	211

CM							
Control M Value	Actual M Value	Control M Value	Actual M Value	Control M Value	Actual M Value	Control M Value	Actual M Value
11000000	32	10011100	92	00011000	152	01010100	212
11000001	33	10011101	93	00011001	153	01010101	213
11000010	34	10011110	94	00011010	154	01010110	214
11000011	35	10011111	95	00011011	155	01010111	215
11000100	36	10100000	96	00011100	156	01011000	216
11000101	37	10100001	97	00011101	157	01011001	217
11000110	38	10100010	98	00011110	158	01011010	218
11000111	39	10100011	99	00011111	159	01011011	219
11001000	40	10100100	100	00100000	160	01011100	220
11001001	41	10100101	101	00100001	161	01011101	221
11001010	42	10100110	102	00100010	162	01011110	222
11001011	43	10100111	103	00100011	163	01011111	223
11001100	44	10101000	104	00100100	164	01100000	224
11001101	45	10101001	105	00100101	165	01100001	225
11001110	46	10101010	106	00100110	166	01100010	226
11001111	47	10101011	107	00100111	167	01100011	227
11010000	48	10101100	108	00101000	168	01100100	228
11010001	49	10101101	109	00101001	169	01100101	229
11010010	50	10101110	110	00101010	170	01100110	230
11010011	51	10101111	111	00101011	171	01100111	231
11010100	52	10110000	112	00101100	172	01101000	232
11010101	53	10110001	113	00101101	173	01101001	233
11010110	54	10110010	114	00101110	174	01101010	234
11010111	55	10110011	115	00101111	175	01101011	235
11011000	56	10110100	116	00110000	176	01101100	236
11011001	57	10110101	117	00110001	177	01101101	237
11011010	58	10110110	118	00110010	178	01101110	238
11011011	59	10110111	119	00110011	179	01101111	239
11011100	60	10111000	120	00110100	180	01110000	240
11011101	61	10111001	121	00110101	181	01110001	241
11011110	62	10111010	122	00110110	182	01110010	242
11011111	63	10111011	123	00110111	183	01110011	243
10000000	64	10111100	124	00111000	184	01110100	244
10000001	65	10111101	125	00111001	185	01110101	245
10000010	66	10111110	126	00111010	186	01110110	246
10000011	67	10111111	127	00111011	187	01110111	247
10000100	68	00000000	128	00111100	188	01111000	248
10000101	69	00000001	129	00111101	189	01111001	249
10000110	70	00000010	130	00111110	190	01111010	250
10000111	71	00000011	131	00111111	191	01111011	251
10001000	72	00000100	132	01000000	192	01111100	252
10001001	73	00000101	133	01000001	193	01111101	253
10001010	74	00000110	134	01000010	194	01111110	254
10001011	75	00000111	135	01000011	195	01111111	255

2.4.2. D-PHY Tx IP Configuration Registers for Timing Parameters

In the case of D-PHY Tx IP Hard Configuration, also the CIL Bypass option must be set for the Configuration Registers for Timing Parameters to be available.

Table 2.7. D-PHY Tx Configuration Registers for Timing Parameters

Offset (6 Bits)	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x1F	Reserved		tLPX[5:0] Duration of any Low-Power state					
0x20	Reserved		tCLK-PREP[5:0] Duration of the LP-00 clock state immediately before the HS-0 clock state in the LP-to-HS sequence					
0x21	Reserved		tCLK_HSZERO[5:0] Duration of the clock HS-0 state prior to starting the actual toggling of the high-speed clock					
0x22	Reserved		tCLKPRE[5:0] Duration of the LP-00 clock state immediately before the HS-0 clock state in the LP-to-HS sequence					
0x23	Reserved		tCLKPOST[5:0] Duration of the HS clock after the last associated Data Lane has transitioned to LP Mode The interval is defined as the period from the end of tHS-TRAIL to the beginning of tCLK-TRAIL					
0x24	Reserved		tCLKTRAIL[5:0] Duration of the HS-0 state after the last clock bit of an HS transmission burst					
0x25	Reserved		tCLKEXIT[5:0] Duration of the clock LP-11 state following an HS transmission burst					
0x26	Reserved		tDATPREP[5:0] Duration of the LP-00 Line state before the HS-0 Line state					
0x27	Reserved		tDAT_HSZERO[5:0] Delay from the LP-00 State to the assertion of the d_hs_rdy_o signal The actual HS-ZERO on the D-PHY data lanes still depends on these three factors: • The delay between the d_hs_rdy_o assertion and the time the requestor sends the payload of a long packet • The number of cycles the packet header (if enabled) can create the sync pattern and the 32-bit header. This varies with the number of lanes and gearing. • The serializer delay. The timing from parallel data input to the serialized output data differs between soft and hard D-PHY implementation.					
0x28	Reserved		tDATTRAIL[5:0] Duration of the flipped bit after the last payload data bit of an HS transmission burst					
0x29	Reserved		tDATEXIT[5:0] Duration of the data LP-11 state following an HS transmission burst					
0x2D	Reserved		tSKEWCAL_INIT[5:0] Duration of Initial Skew Calibration					
0x2E	Reserved		tSKEWCAL_INIT [9:6] Duration of Initial Skew Calibration					
0x2F	Reserved		tSKEWCAL_PERIOD[5:0] Duration of Periodic Skew Calibration					
0x30	Reserved		tSKEWCAL_PERIOD[9:6] Duration of Periodic Skew Calibration					

2.4.3. D-PHY Tx IP Packet Formatter Registers

These registers store the header information of the last packet transmission request received by the IP. These are only available when the Packet Formatter is enabled.

Table 2.8. D-PHY Tx Status Registers for Timing Parameters

Offset (6 Bits)	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x2A	vc_id[1:0]		data_type[5:0]					
0x2B	word_count[15:8]							
0x2C	word_count[7:0]							

vc_id[1:0] - 2-bit virtual channel ID of the received packet

data_type[5:0] - 6-bit CSI-2 or DSI data type field

word_count[15:0] - 16-bit Word Count field. This denotes the number of bytes in the payload of a long packet. In a short packet, this contains a 2-byte data

3. Timing Diagrams

In the configurations without the AXI4-Stream, the requestor should wait for the c2d_ready_o signal to ensure the CSI-2/DSI D-PHY Transmitter IP is not busy from a previous transmit request, and that the data lanes (and also the clock lane, in the case of non-continuous clock mode) have completed the required tHS-EXIT.

The d_hs_rdy_o signal signifies the clock and data lanes have performed the LP-HS request sequence, including sending out the necessary tHS-ZERO and are in high-speed mode. The requestor can then send out the information of the packet to be transmitted, along with the payload. The c2d_ready_o signal goes back to high only after the completion of the tHS-EXIT.

The phdr_xfr_done_o indicates the Packet Header FSM has sent out the packet header and payload, including the CRC, to the Tx Global Operation module.

See the subsections below for more information on the required handshake timing.

3.1. Short Packet Transmission in CSI-2/DSI Interfaces

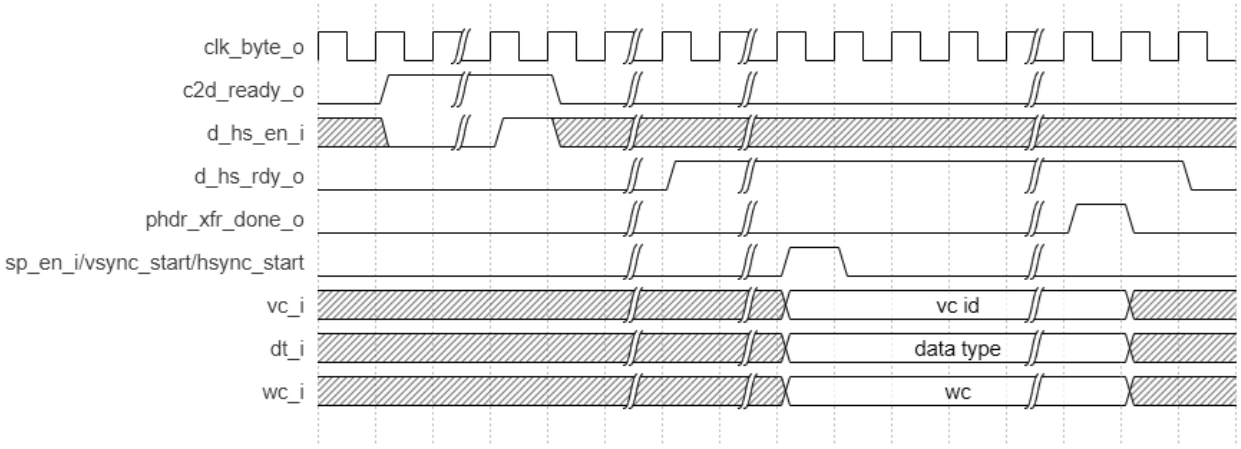

Figure 3.1. D-PHY Tx Input Bus for Short Packet Transmission in CSI-2/DSI Interfaces

3.2. Long Packet Transmission in CSI-2/DSI Interface

When the protocol type selected is CSI-2, there is no internal buffer to save the incoming payload data before the creation of the header packet. Because of this, the IP requires 3 cycles from the assertion of the ld_pyld_o to the arrival of the valid payload data. The ld_pyld_o asserts the next cycle after the detection of the lp_en_i.

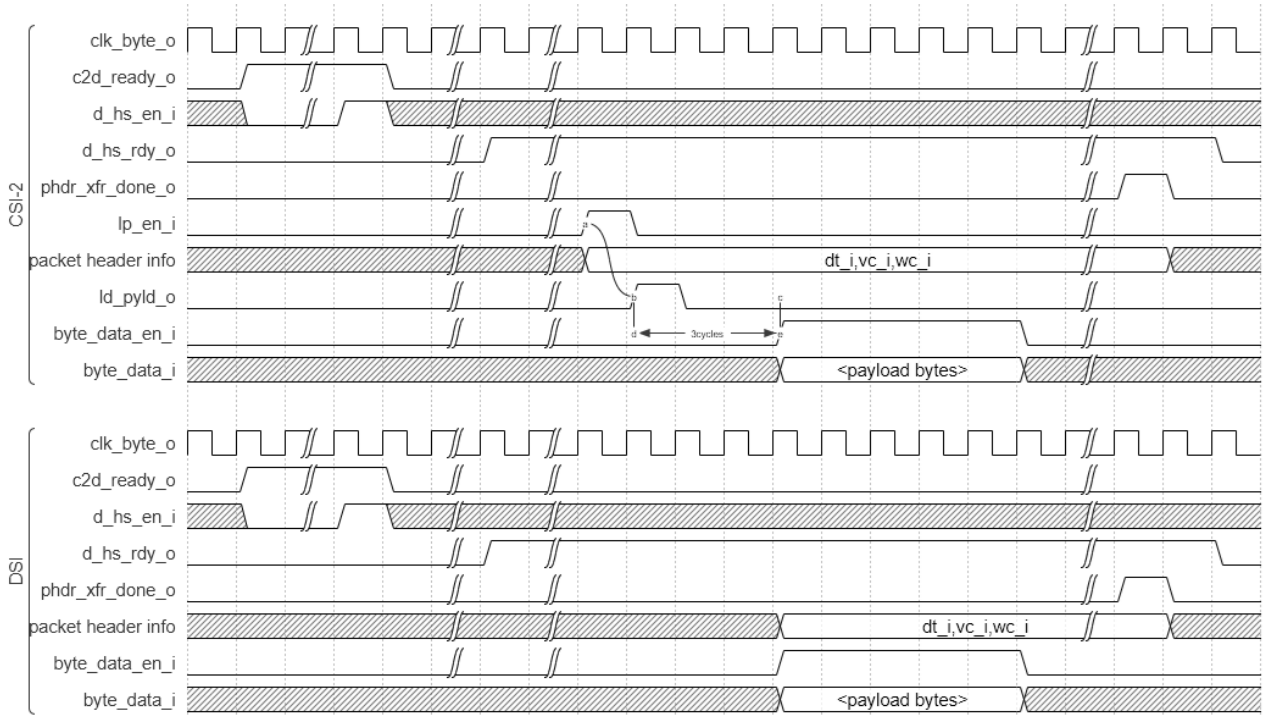

Figure 3.2. D-PHY Tx Input Bus for Long Packet Transmission in CSI-2/DSI Interface

3.3. Long Packet Transmission in CSI-2/DSI Interface without Packet Formatter

The Packet Parser module appends the sync code before the packet header. If the packet parser is disabled, the requestor interfaces directly to the Global Operations Control module, therefore the byte_Data_i should already contain the sync code B8 for each lanes. The Global Operations Control module is not aware of the boundary of the actual valid bits, therefore it cannot flip the last valid bit to create the trail. The last word is treated as pure trail bits, and is sent out to the data lanes until the tHS-TRAIL is met.

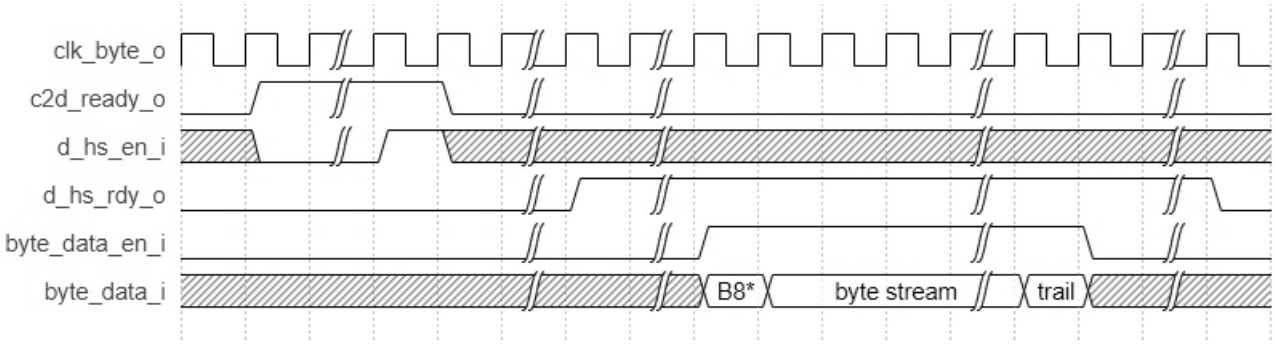

Figure 3.3. D-PHY Tx Input Bus for LP Transmission in CSI-2/DSI Interface without Packet Formatter

3.4. Enable Periodic Skew Calibration

A low-to-high transition of skewcal_period_en_i initiates the periodic skew calibration. The signal, skewcal_period_en_i, is only available when the attribute Enable Periodic Skew Calibration is enabled. c2d_ready_o should be high when before initiating periodic skew calibration.

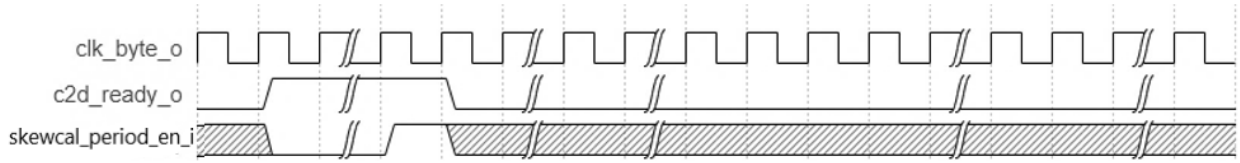

Figure 3.4. D-PHY Tx Input Bus to Enable Periodic Slew Calibration

3.5. AXI4-Stream Device Slave

AXI4-STREAM Device Slave provides an interface for receiving payload data (Byte Data or Packet Data with Virtual Channel and Data Type and Word Count). Figure 3.5 shows data format when AXI4-Stream is ON.

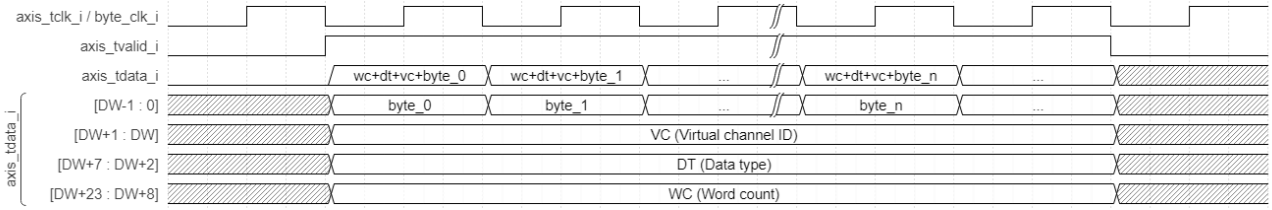

Figure 3.5. AXI4-Stream Enabled and LMMI Disabled Data Format and Packet Formatter Enabled

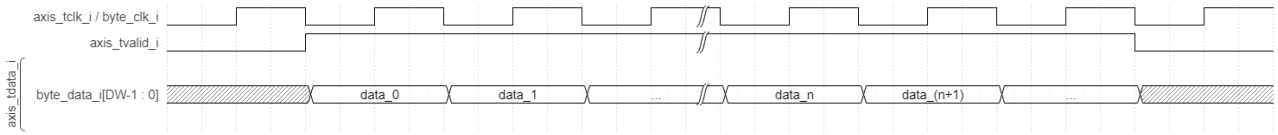

Figure 3.6. AXI4-Stream Enabled and Packet Formatter Disabled Data Format

If the AXI4-Stream Device is not enabled, then the internal signals listed below turn to top level input signals.

- byte_data_en_i,
- byte_data_i[…]
- vc_i,
- dt_i,
- wc_i

3.6. Byte Data Arrangement

The CSI-2/DSI D-PHY Transmitter IP, when in gear 16, have an option to take the parallel data arranged in sequential byte order, or in lane interleaved arrangement. This is configurable through the Interleaved Input Data attribute in the user interface. See Table 3.1.

Table 3.1. Interleaved vs. Sequential Byte Data Input

byte_data_i	4-Lane		2-Lane		1-Lane	
	Interleaved	Sequential	Interleaved	Sequential	Interleaved	Sequential
[7:0]	Byte 0	Byte 0	Byte 0	Byte 0	Byte 0	Byte 0
[15:8]	Byte 4	Byte 1	Byte 2	Byte 1	Byte 1	Byte 1
[23:16]	Byte 1	Byte 2	Byte 1	Byte 2	—	—
[31:24]	Byte 5	Byte 3	Byte 3	Byte 3	—	—
[39:32]	Byte 2	Byte 4	—	—	—	—
[47:40]	Byte 6	Byte 5	—	—	—	—
[55:48]	Byte 3	Byte 6	—	—	—	—
[63:56]	Byte 7	Byte 7	—	—	—	—

4. Core Generation, Simulation, and Validation

This chapter provides information on how to generate and synthesize CSI-2/DSI D-PHY Tx IP Core using Lattice Radiant Software, as well as on how to run simulation. For more on Lattice Radiant Software, refer to the Lattice Radiant Software User Guide and relevant Lattice tutorials.

4.1. Generation and Synthesis

Lattice Radiant Software allows you to generate and customize modules and IPs and integrate them into the device architecture.

To generate the CSI-2/DSI D-PHY Tx IP Core in Lattice Radiant Software:

1. In the **Module/IP Block Wizard** create a new Lattice Radiant Software project for CSI-2/DSI D-PHY Tx IP Core.
2. In the dialog box of the **Module/IP Block Wizard** window, configure CSI-2/DSI D-PHY Tx IP Core according to custom specifications, using drop-down menus and check boxes. As a sample configuration, see Figure 4.1. For configuration options, see Table 2.3.

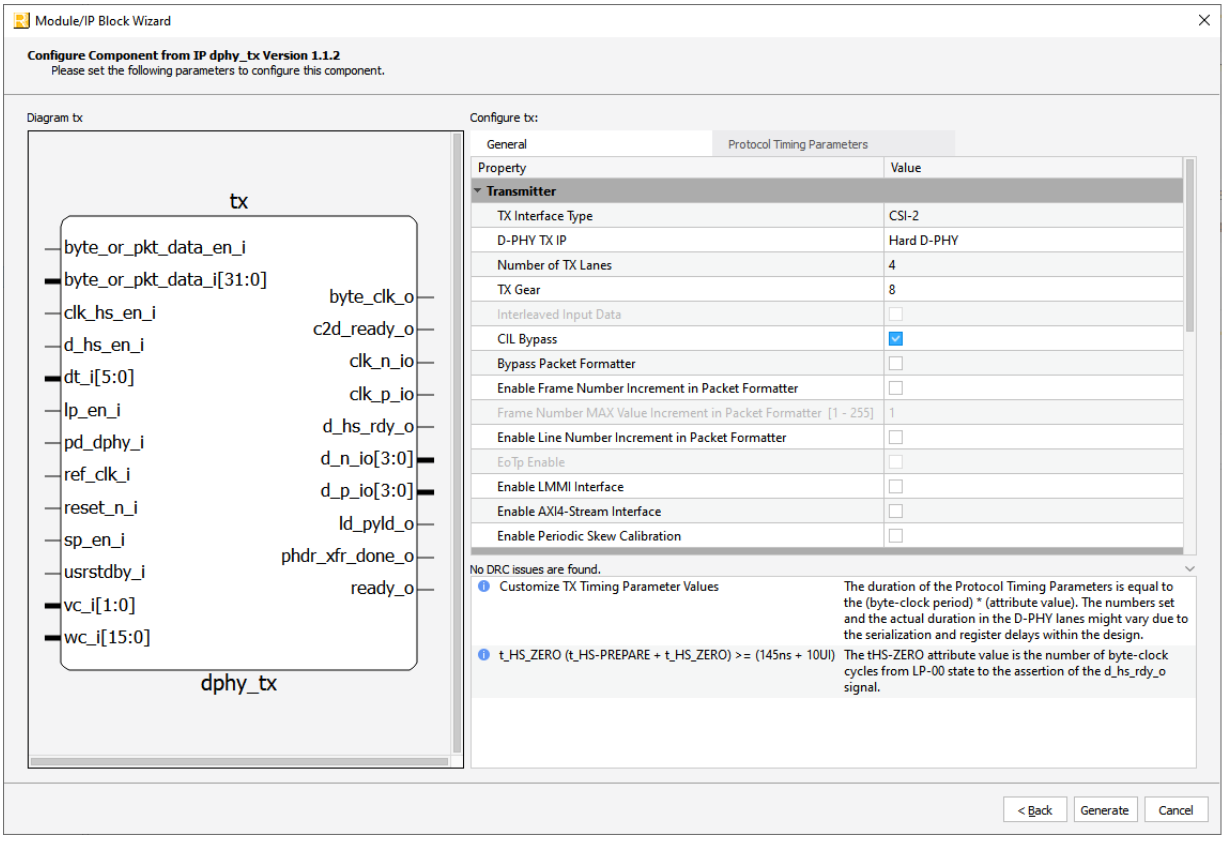

Figure 4.1. Configure Block of D-PHY Tx

3. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results as shown in Figure 4.2.

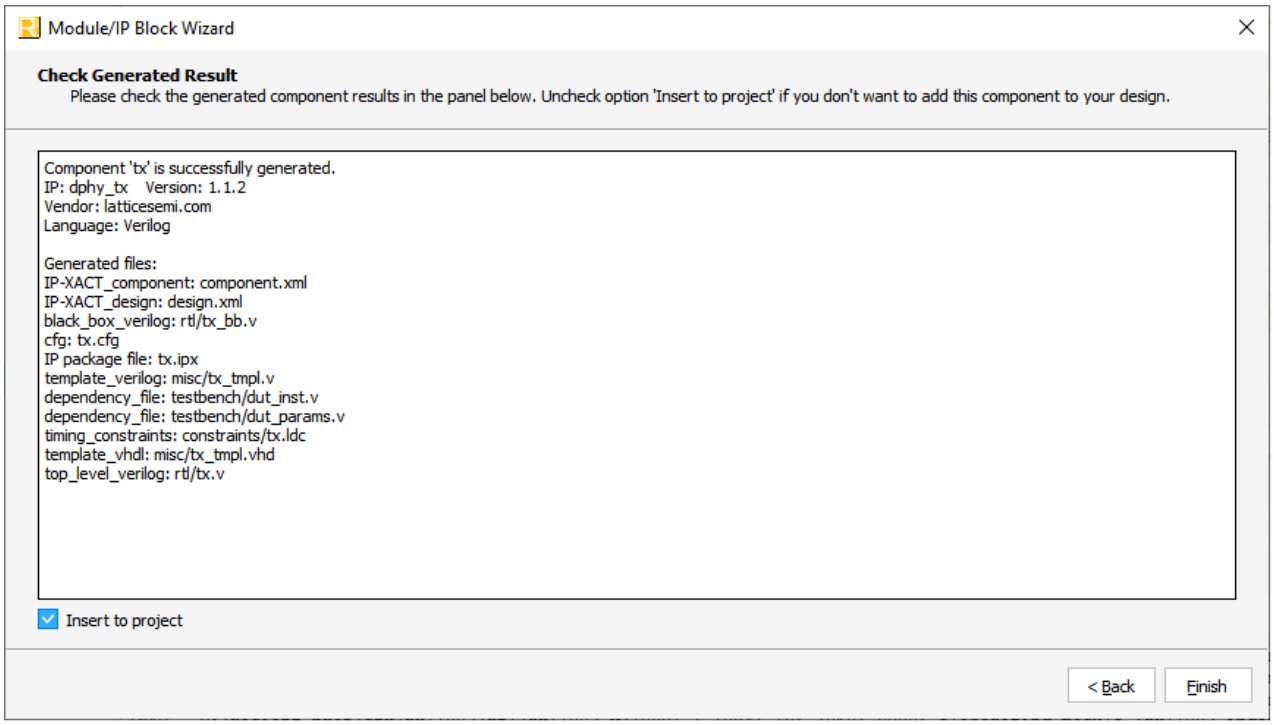

Figure 4.2. Check Generating Result

4. Click the **Finish** button to generate the Verilog file.

   Upon generating desired design, you can synthesize it by clicking **Synthesize Design** located in the top left corner of the screen, as shown in Figure 4.3.

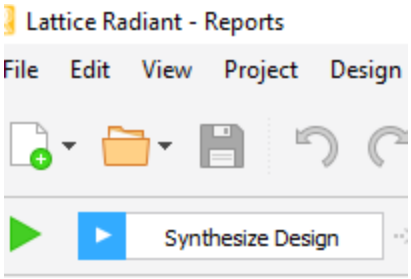

Figure 4.3. Synthesizing Design

4.2. Functional Simulation

To run Verilog simulation:

1. Using the Lattice Radiant Software tcl console, go to the newly created *testbench* directory and run the command *source create Defines.tcl* to generate Verilog defines file.
2. Click the  button located on the **Toolbar** to initiate the Simulation Wizard shown in Figure 4.4.

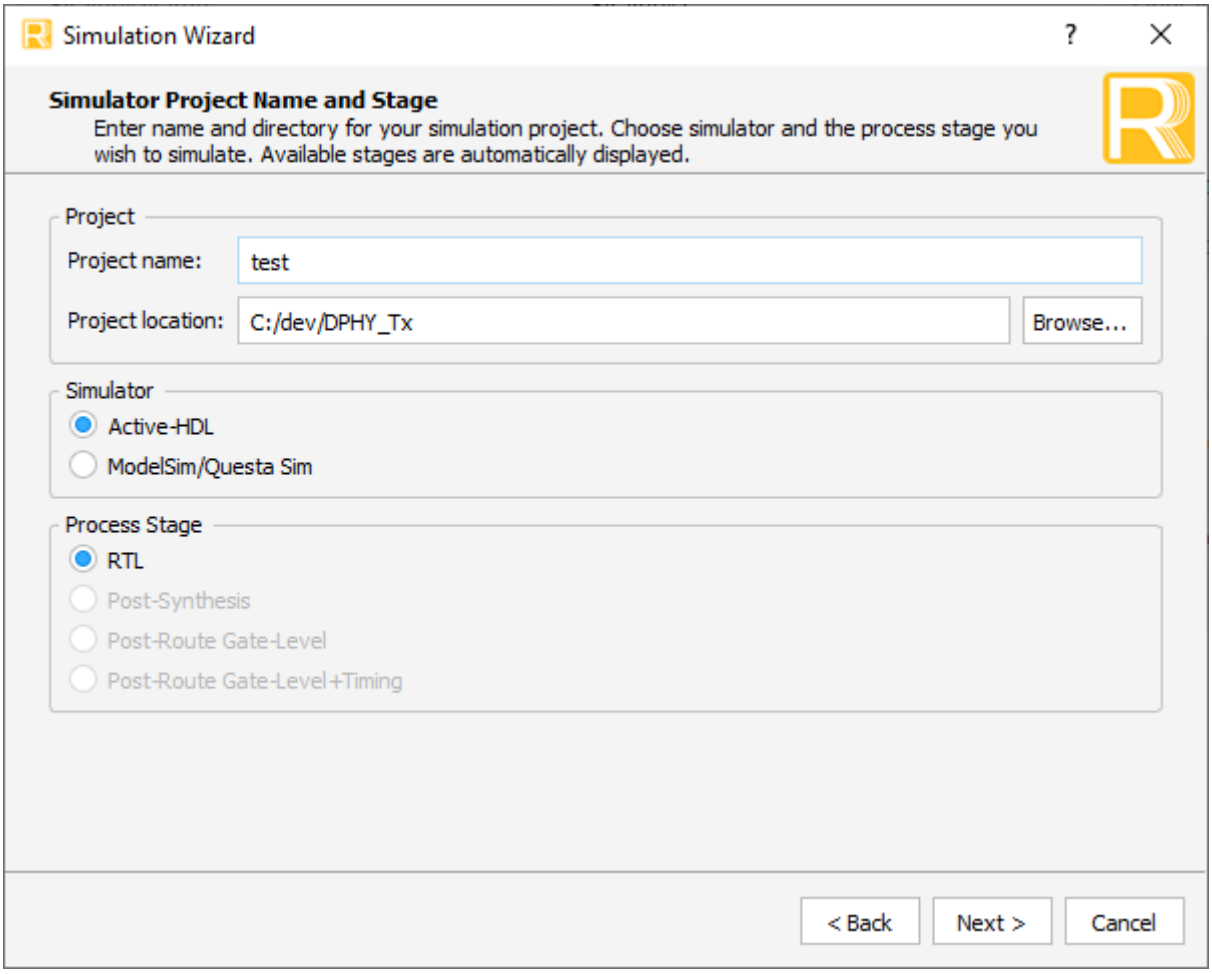

Figure 4.4. Simulation Wizard

3. Click **Next** twice to open the **Add and Reorder Source** window as shown in Figure 4.5.

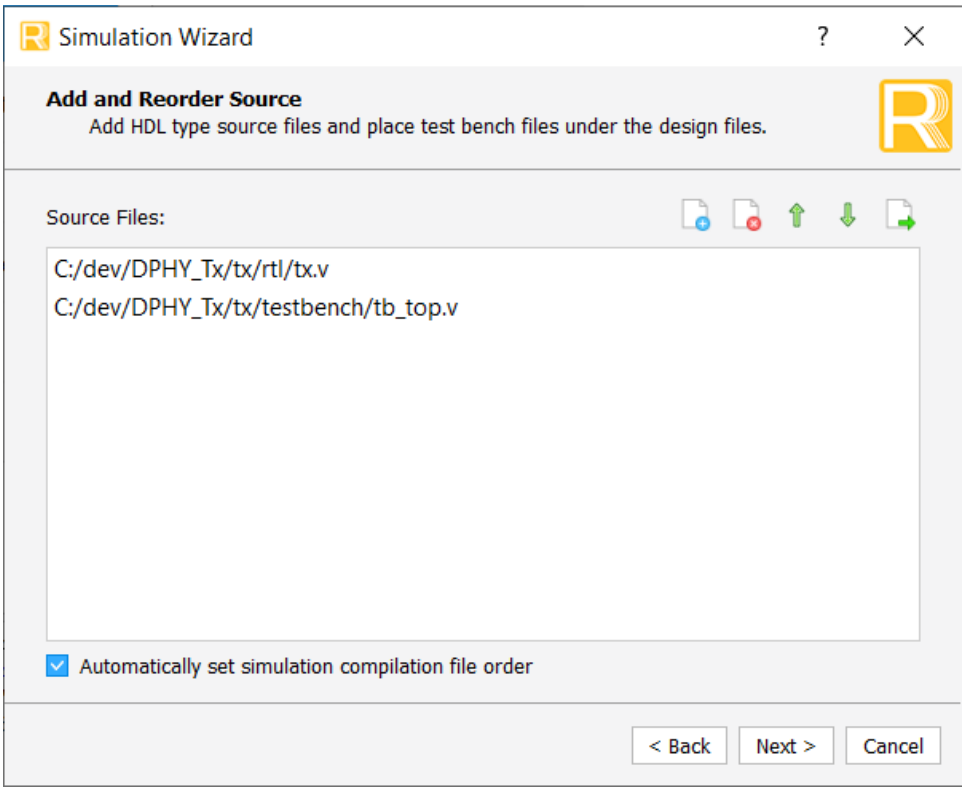

Figure 4.5. Adding and Reordering Source.

4. Click **Next** to run simulation.

4.3. Core Validation

The functionality of the CSI-2/DSI D-PHY Transmitter IP core is verified through simulation using Lattice's in-house testbench environment and hardware validation.

5. Licensing and Evaluation

5.1. Licensing the IP

An IP core-specific license string is required fully enable the CSI-2/DSI DPHY Tx IP Core in a complete, top-level design. In CrossLink-NX and Certus-NX devices, you can fully evaluate the IP core through functional simulation and implementation (synthesis, map, place and route) without an IP license string. This IP core supports Lattice's IP hardware evaluation capability, which makes it possible to create versions of the IP core, and evaluate in the device for a limited time (approximately four hours) without the need of an IP license string. See Hardware Evaluation section for further details. A license string is required to enable timing simulation, and generation of the bitstream file, not limited by the hardware timeout.

5.2. Hardware Evaluation

There is no restriction on the hardware evaluation of this IP core.

6. Ordering Part Number

The Ordering Part Number (OPN) for this IP Core are the following:

- DPHY-TX-CNX-U – CSI-2/DSI DPHY Transmitter for CrossLink-NX - Single Design License
- DPHY-TX-CNX-UT – CSI-2/DSI DPHY Transmitter for CrossLink-NX - Site License
- DPHY-TX-CTNX-U – CSI-2/DSI DPHY Transmitter for Certus-NX - Single Design License
- DPHY-TX-CTNX-UT – CSI-2/DSI DPHY Transmitter for Certus-NX - Site License

Appendix A. Resource Utilization

Table A.1 and Table A.2 show the maximum frequency and resource utilization for a certain IP configuration.

Table A.1. Device and Tool Tested

	Value
Diamond Software Version	Radiant 2.1 production build
Device Used	LIFCL-40-BCG400
Performance Grade	9_High-Performance_1.0V
Synthesis Tool	Synplify Pro (R) Q-2020.03LR, Build 134R, May 8 2020

Table A.2. Resource Utilization[1]

Number of Lanes (Gear)	IP Type	Bit Rate Lane	Bypass Packet Formatter	LMMI	AXI	EBR	Registers	LUT[2]	High-Speed I/O Interfaces
4 (8)	Hard DPHY	1000 Mbps	DIS	DIS	EN	0	294	549	1 x Hard D-PHY
4 (8)	Soft DPHY	1000 Mbps	DIS	DIS	EN	0	330	575	5 x ODDRX4, 1 x ECLKDIV, 1 x ECLKSYNC
4 (16)	Hard DPHY	2500 Mbps	DIS	DIS	EN	0	399	1226	1 x Hard D-PHY
4 (8)	Soft DPHY	1500 Mbps	DIS	DIS	EN	0	330	583	5 x ODDRX4, 1 x ECLKDIV, 1 x ECLKSYNC
4 (16)	Hard DPHY	2500 Mbps	DIS	EN	EN	0	530	1522	1 x Hard D-PHY
4 (8)	Soft DPHY	1500 Mbps	DIS	DIS	DIS	0	330	639	5 x ODDRX4, 1 x ECLKDIV, 1 x ECLKSYNC
4 (16)	Hard DPHY	2500 Mbps	EN	EN	EN	0	362	388	1 x Hard D-PHY
4 (8)	Soft DPHY	1500 Mbps	EN	DIS	DIS	0	182	188	5 x ODDRX4, 1 x ECLKDIV, 1 x ECLKSYNC

Notes:

1. All other settings are default.
2. The *distributed RAM* utilization is accounted for in the total LUT4s utilization. The actual LUT4 utilization is distribution among *logic*, *distributed RAM*, and *ripple logic*.

Appendix B. Limitations

Synthesis may fail when LSE is selected as the synthesis tool and the IP is configured with the *Enable LMMI interface* option checked.

References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Radiant Software User Guide.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.3, November 2020

Section	Change Summary

Introduction	• Updated Table 1.1. CSI-2/DSI DPHY Tx IP Core Quick Facts.
	  • Updated Lattice Implementation.
	  • Updated reference to the Lattice Radiant Software User Guide.
	• Added support for periodic deskew calibration to the Features section.

Functional Description	• Added skewcal_period_en_i input port to Figure 2.1, Figure 2.2, Figure 2.3, and Figure 2.4.
	• Updated Figure 2.6 and added contents to the Global Operation Module section.
	• Added the skewcal_period_en_i signal under D-PHY Tx and updated axis_stready_o description in Table 2.2. D-PHY Tx IP Core Signal Description.
	• Updated Table 2.3. Attributes Table.
	  • Added Tansmitter attributes.
	  • Added TX Global Operation Timing Parameters attributes.
	  • Updated Clock attributes.
	• Removed 0x03 Bit[0] data from Table 2.4. Hard Configured D-PHY Tx Configuration Registers (MIPI Programmable Bits).
	• Updated Table 2.7. D-PHY Tx Configuration Registers for Timing Parameters.

Timing Diagrams	• Added the Enable Periodic Skew Calibration section. • Removed Figure 3.6 and Figure 3.7. • Added bullets to internal signals in AXI4-Stream Device Slave section.
Core Generation, Simulation, and Validation	• Updated reference to the Lattice Radiant Software User Guide. • Updated Figure 4.1. Configure Block of D-PHY Tx. • Updated Figure 4.2. Check Generating Result.
References	Updated reference to the Lattice Radiant Software User Guide.

Revision 1.2, August 2020

Section	Change Summary
Introduction	• Updated Table 1.1.. • Updated the Hard MIPI D-PHY Tx IP Core Features and Soft MIPI D-PHY Tx IP Core Features sections.
Functional Description	General update to this section.
Signal Description	Updated Table 2.2. D-PHY Tx IP Core Signal Description.
Attribute Summary	Updated Table 2.3. Attributes Table.
Internal Registers	Removed this section.
Core Generation, Simulation, and Validation	Updated figures in procedures.
Ordering Part Number	Added part numbers.
Appendix A. Resource Utilization	Added this section.
Appendix B. Limitations	Added this section.

Revision 1.1, February 2020

Section	Change Summary
Introduction	• Updated Table 1.1 to add LIFCL-17 as targeted device. • Updated Hard MIPI D-PHY Tx IP Core Features and Soft MIPI D-PHY Tx IP Core Features sections.
Attributes Table	Updated Table 2.1. Attributes Table.

Revision 1.0, December 2019

Section	Change Summary
All	Initial release.

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