SGMII and Gb Ethernet PCS IP Core - Lattice Radiant Software

User Guide

FPGA-IPUG-02077-1.2

June 2020

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS and with all faults, and all risk associated with such information is entirely with Buyer. Buyer shall not rely on any data and performance specifications or parameters provided herein. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. No Lattice products should be used in conjunction with mission- or safety-critical or any other application in which the failure of Lattice's product could create a situation where personal injury, death, severe property or environmental damage may occur. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Contents

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Figures

Tables

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CTC	Clock Tolerance Compensation
FIFO	First In First Out
LMMI	Lattice Memory Mapped Interface
RTL	Register Transfer Language
SGMII	Serial Gigabit Media Independent Interface

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

1. Introduction

The Serial Gigabit Media Independent Interface (SGMII) connects Ethernet Media Access Controllers (MACs) and Physical Layer Devices (PHYs). This IP core may be used in bridging applications and/or PHY implementations. It is widely used as an interface for a discrete Ethernet PHY chip.

Table 1.1 presents a summary of SGMII IP.

1.1. Quick Facts

Table 1.1 presents a summary of the SGMII IP.

Table 1.1. SGMII IP Quick Facts

IP Requirements	Supported FPGA Families	CrossLink™-NX; Certus™-NX
Resource Utilization	Targeted Devices	LIFCL-40, LIFCL-17, LFD2NX-40
	Supported User Interface	(G)MII
	Resources	See Table A.1. Resource Utilization.
Design Tool Support	Lattice Implementation	IP Core v1.0.x – Lattice Radiant® Software 2.1
	Synthesis	Lattice Synthesis Engine
		Synopsys® Synplify Pro for Lattice
	Simulation	For a list of supported simulators, see the Lattice Radiant Software 2.1 User Guide.

1.2. Features

The key features of the SGMII IP include:

- Physical Coding Sublayer (PCS) functions of the Cisco SGMII Specification, Revision 1.8
- PCS functions for IEEE 802.3z (1000BaseX)
- Dynamic selection of SGMII/1000BaseX PCS operation
- Support for MAC or PHY mode for SGMII auto-negotiation
- Support for (G)MII data rates of 1 Gbps, 100 Mbps, 10 Mbps
- Easy Connect option for seamless integration with Lattice Semiconductor's Tri-Speed MAC (TSMAC) IP core
- Management Interface Port for control and maintenance

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal names that end with:

- _*n* are active low (asserted when value is logic 0)
- _*i* are input signals
- _*o* are output signals

1.3.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2. Functional Descriptions

2.1. Overview

SGMII/Gb Ethernet PCS IP core converts GMII frames into 8-bit code groups in both transmit and receive directions and performs auto-negotiation with a link partner as described in the Cisco SGMII and IEEE 802.3z specifications. SGMII IP is a connection bus for MACs and PHYs and is often used in bridging applications and/or PHY implementations. It is particularly widely used as an interface for a discrete Ethernet PHY chip.

Top-level block diagram of the SGMII IP CORE is shown in Figure 2.1.

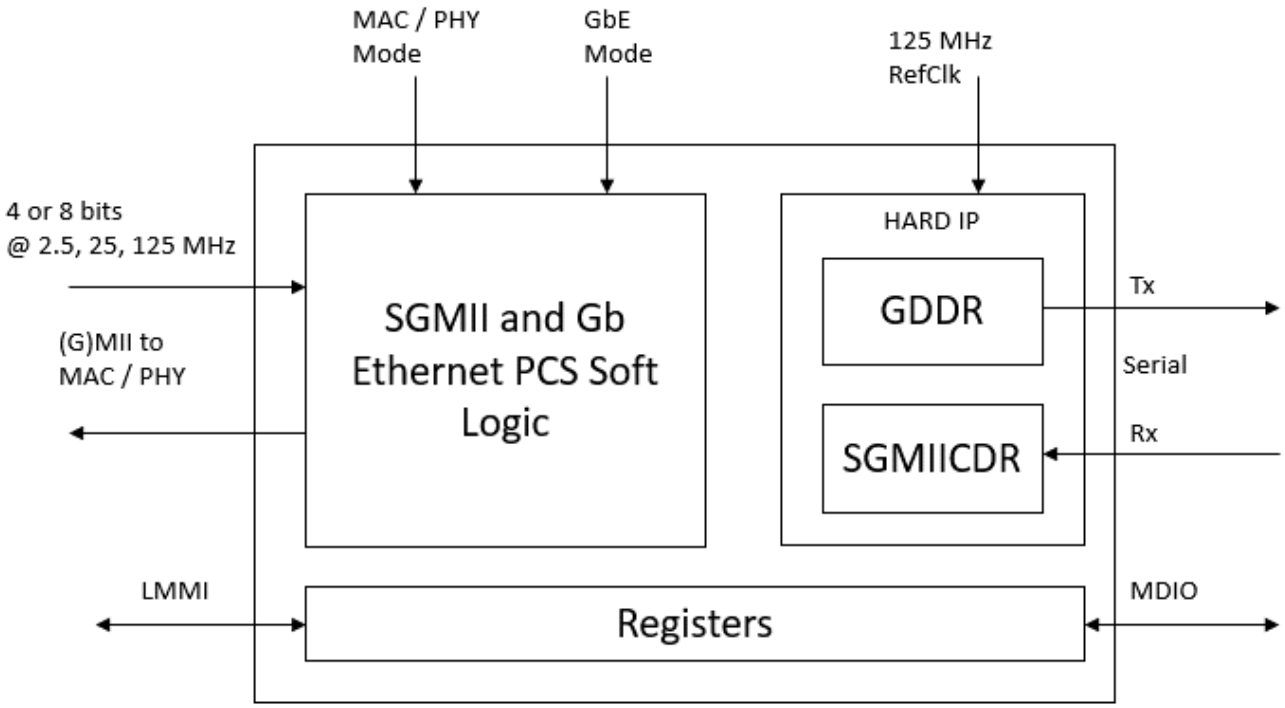

Figure 2.1. SGMII/Gb Ethernet PCS IP Top-Level Block Diagram

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.2. Signal Description

Table 2.1. SGMII IP Core Signal Description

Port Name	I/O	Width	Description
Clock and Reset			
tx_clk_125_i	In	1	Transmit 125 MHz Clock – 125 MHz clock for transmit state machine. Incoming data from the transmit rate adaptation block data is sampled on the rising edge of this clock. Outgoing 10-bit code group transmit data is launched on the rising edge of this clock.
tx_clk_mii_i	In	1	Transmit MII Clock – 125 MHz, 25 MHz, or 2.5 MHz clock for incoming (G)MII transmit data. Data is sampled on the rising edge of this clock. Note that this port is only present when the IP core is generated using the *Classic* (G)MII option.
tx_clock_enable_source_o[1]	Out	1	Transmit Clock Enable Source – This signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option. This signal is used in combination with the transmit 125 MHz clock to regulate the flow of transmit (G)MII data. The signal is generated by the transmit rate adaptation block. This clock enable should be tied to the transmit section of the MAC that sends transmit Ethernet frames to the SGMII and Gb Ethernet PCS IP core. This clock enable should also be tied to the clock enable *sink* of the SGMII and Gb Ethernet PCS IP core. This clock enable's behavior is controlled by the setting of the operational rate pins of the IP core. For 1 Gbps operation, the clock enable is constantly high. For 100 Mbps operation, the clock enable is high for one-out-of-ten 125 MHz clock cycles. For 10 Mbps operation, the clock enable is high for one-out-of-one-hundred 125 MHz clock cycles.[1]
tx_clock_enable_sink_i[1]	In	1	Transmit Clock Enable Sink – This signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option. This signal is used in combination with the transmit 125 MHz clock to regulate the flow of transmit (G)MII data. When the clock enable is high and the transmit clock edge rises, (G)MII data is sampled.[1]
rx_clk_125_i	In	1	Receive 125MHz Clock – 125 MHz clock for synchronization and receive state machines. Incoming code groups from the receive CTC block data are sampled on rising edge of this clock. Outgoing GMII data is launched on the rising edge of this clock.
rx_clk_mii_i	In	1	Receive MII Clock – 125 MHz, 25 MHz, or 2.5 MHz clock for outgoing (G)MII receive data. Data is launched on the rising edge of this clock. Note, this port is only present when the IP core is generated using the *Classic* (G)MII option.
rx_clock_enable_source_o[2]	Out	1	Receive Clock Enable Source – This signal is similar to the tx_clock_enable_source described above, except that it is used for the receive data path. Note that this signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option.[2]
rx_clock_enable_sink_i[2]	In	1	Receive Clock Enable Sink – This signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option. This signal is used in combination with the receive 125 MHz clock to regulate the flow of receive (G)MII data. When the clock enable is high and the receive clock edge rises, (G)MII data is launched.[2]
serdes_recovered_clk_i	In	1	SERDES Recovered Clock – 125 MHz clock recovered from receive side of SERDES. This signal is synchronous with the 10-bit code groups received by the SERDES and should be used to clock receive data between the SERDES and the IP core. The IP core samples incoming 10-bit code groups on the rising edge of this clock.
rst_n_i	In	1	Reset – Active low global reset.

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Port Name	I/O	Width	Description
GMII			
tx_d_i	In	8	Transmit Data – Incoming (G)MII data. Note that this port's behavior varies depending on the (G)MII option used when generating the IP core. For *Classic* mode, when the (G)MII data rate is 1 Gbps, all 8 bits of tx_d_i are valid. However, for 100 Mbps and 10 Mbps, only bits 3:0 of tx_d_i are valid. For the *TSMAC Easy Connect* mode all 8 bits of tx_d_i are valid for all (G)MII data rates (1 Gbps, 100 Mbps, 10 Mbps).
tx_en_i	In	1	Transmit Enable – Active high signal; asserts when incoming data is valid.
tx_er_i	In	1	Transmit Error – Active high signal used to denote transmission errors and carrier extension on incoming (G)MII data port.
rx_d_o	Out	8	Receive Data – Outgoing (G)MII data. Note that this port's behavior varies depending on the (G)MII option used when generating the IP core. For *Classic* mode, when the (G)MII data rate is 1Gbps, all 8 bits of rx_d_o are valid. However, for 100 Mbps and 10 Mbps, only bits 3:0 of rx_d_o are valid. For the *TSMAC Easy Connect* mode all 8 bits of rx_d_o are valid for all (G)MII data rates (1Gbps, 100 Mbps, 10 Mbps).
rx_dv_o	Out	1	Receive Data Valid – Active high signal, asserts when outgoing data is valid.
rx_er_o	Out	1	Receive Error – Active high signal used to denote transmission errors and carrier extension on outgoing (G)MII data port.
col_o	Out	1	Collision Detect – Active high signal, asserts when tx_en_i and rx_dv_o are active at the same time.
crs_o	Out	1	Carrier Sense Detect – Active high signal, asserts when rx_dv_o is high.
Interrupt Port			
int_o	Out	1	Interrupt signal.
Management			
mr_adv_ability_i[15:0]	In	1	Advertised Ability – Configuration status transmitted by PCS during auto-negotiation process.
mr_an_enable_i	In	1	Auto-Negotiation Enable – Active high signal that enables auto-negotiation state machine to function.
mr_main_reset_i	In	1	Main Reset – Active high signal that forces all PCS state machines to reset.
mr_restart_an_i	In	1	Auto-Negotiation Restart – Active high signal that forces auto-negotiation process to restart.
mr_an_complete_o	Out	1	Auto-Negotiation Complete – Active high signal that indicates that the auto-negotiation process is completed.
mr_lp_adv_ability_o	Out	16	Link Partner Advertised Ability – Configuration status received from partner PCS entity during the auto-negotiation process. The bit definitions are the same as described above for the mr_adv_ability_i port.
mr_page_rx_o	Out	1	Auto-Negotiation Page Received – Active high signal that asserts while the auto-negotiation state machine is in the *Complete_Acknowledge* state.
force_isolate_i	In	1	Force PCS Isolate – Active high signal that isolates the PCS. When asserted, the RX direction forces the (G)MII port to all zeros, regardless of the condition of the incoming 1.25 Gbps serial data stream. In the TX direction, the condition of the incoming (G)MII port is ignored. The TX PCS behaves as though the (G)MII TX input port was forced to all zeros. Note, however, that the isolate function does not produce any electrical isolation – such as tri-stating of the (G)MII RX outputs of the IP core. When the signal is de-asserted (low), the PCS isolation functions are deactivated. The use of this signal is optional. If the user chooses not to use the isolate function, then this signal should be tied low.
force_loopback_i	In	1	Force PCS Loopback – Active high signal that activates the PCS loopback function. When asserted, the 10-bit code-group output of the transmit state machine is looped back to the 10-bit code-group input of the receive state machine. When de-asserted, the loopback function is deactivated. The use of this signal is optional. If the user chooses not to use the loopback function, then this signal should be tied low.

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Port Name	I/O	Width	Description
force_unidir_i	In	1	Force PCS Unidirectional Mode – Active high signal that activates the PCS unidirectional mode. When asserted, the transmit state machine path between the TX (G)MII input and the TX 10-bit code-group output will remain operational, regardless of what happens on the RX data path. (Normally RX loss of sync, invalid code-group reception, auto-negotiation restarts can force the transmit state machine to temporarily ignore inputs from the TX (G)MII port). When de-asserted, the unidirectional mode is deactivated. The use of this signal is optional. If the user chooses not to use the unidirectional function, then this signal should be tied low.
an_link_ok_o	Out	1	Auto-Negotiation Link Status OK – Active high signal that indicates that the link is ok. The signal is driven by the auto-negotiation state machine. When auto-negotiation is enabled, the signal asserts when the state machine is in the LINK_OK state. If auto-negotiation is disabled, the signal asserts when the state machine is in the AN_DISABLE_LINK_OK state (see IEEE 802.3 figure 37-6). This signal is intended to be used to produce the *Link Status* signal as required by IEEE 802.3, Status Register 1, Bit D2 (see IEEE 802.3 paragraph 22.2.4.2.13)
soft_plol_o	Out	1	Tx PLL Loss of Lock output to the user logic
LMMI			
lmmi_request_i	In	1	Start transaction.
lmmi_wr_rdn_i	In	1	Write = 1'b1, Read = 1'b0
lmmi_offset_i	In	6	Register offset, starting at offset 0
lmmi_wdata_i	In	16	Output data bus
lmmi_rdata_o	Out	16	Input data bus
lmmi_rdata_valid_o	Out	1	Read transaction is complete and lmmi_rdata_o contains valid data.
lmmi_ready_o	Out	1	IP is ready to receive a new transaction. This is always asserted (tied to 1'b1).
Miscellaneous			
sgmii_mode_i	In	1	SGMII Mode – Controls the behavior of the auto-negotiation process when the core is operating in SGMII mode. 0 = operates as MAC-side entity, 1 = operates as PHY-side entity.
gbe_mode_i	In	1	Gigabit Ethernet Mode – Controls the core's PCS function. 0 = operates as SGMII PCS, 1 = operates as Gigabit Ethernet PCS (1000BaseX)
operational_rate_i	In	2	Operational Rate – When the core operates in SGMII PCS mode, this port controls the regulation rate of the rate adaptation circuit blocks as follows: 10 = 1G bps Rate 01 = 100 Mbps Rate 00 = 10 Mbps Rate Note in Gigabit Ethernet PCS mode, the rate adaptation blocks always operates at the 1Gbps rate, regardless of the settings on the operational_rate_i control pins.
debug_link_timer_short_i	In	1	Debug Link Timer Mode – Active high signal that forces the auto-negotiation link timer to run much faster than normal. This mode is provided for debug purposes (e.g., allowing simulations to run through the auto-negotiation process much faster than normal).

Notes:

1. Connect tx_clock_enable_sink_i to tx_clock_enable_source_o. Relationships between TX-side signals are shown in Figure 2.2.
2. Connect rx_clock_enable_sink_i to rx_clock_enable_source_o. Relationships between RX-side signals are shown in Figure 2.3.

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

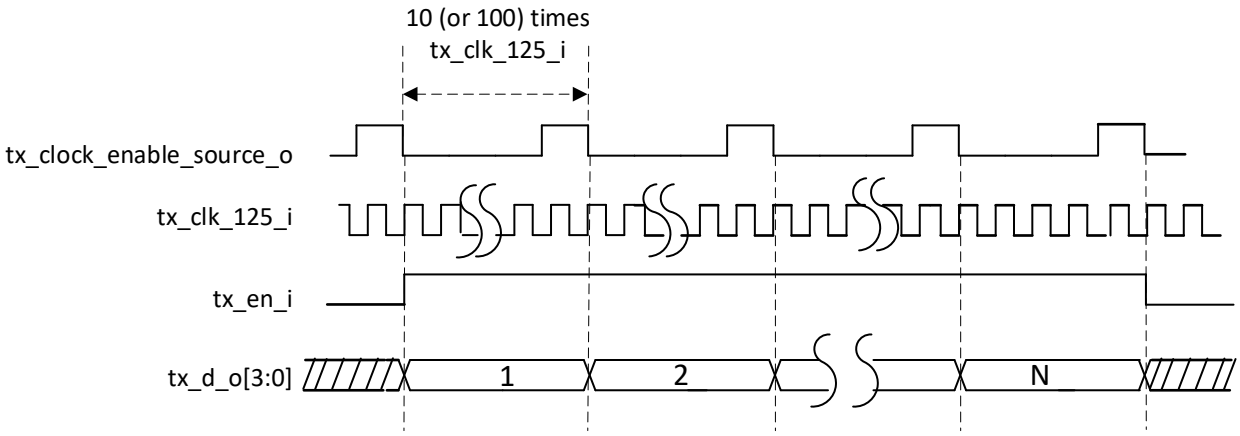

Figure 2.2. SGMII TX-Side Signals Relationship

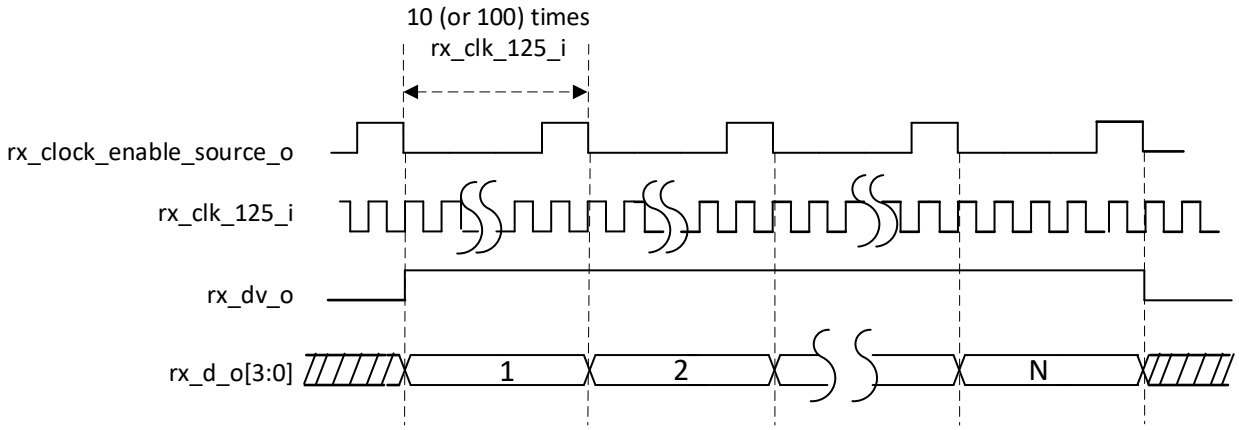

Figure 2.3. SGMII RX-Side Signals Relationship

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.3. Attribute Summary

The configurable attributes of the SGMII IP Core are shown in Table 2.2 and are described in Table 2.3. The attributes can be configured through the IP Catalog's Module/IP wizard of the Lattice Radiant Software.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
General			
(G)MII Interface	Classic, TSMAC	Classic	—
CTC Mode	Static, Dynamic, None	Dynamic	—
Static Low FIFO Threshold	3 - 1010	16	—
Static High FIFO Threshold	13 - 1020	32	—

Table 2.3. Attributes Descriptions

Attribute	Description
General	
(G)MII Interface	This attribute affects the behavior and implementation of the (G)MII port. In *Classic* mode, the (G)MII data port is 8 bits wide. All 8 bits are used for 1Gbps operation. Only the lower 4 bits are used for 100Mbs and 10 Mbps operation. A separate MII clock is used to synchronize the (G)MII data. The MII clock frequency varies with the (G)MII data rate: 125 MHz for 1 Gbps, 25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps. For the *TSMAC Easy Connect* mode, the (G)MII data port is 8 bits wide; and all 8 bits are used, regardless of the (G)MII data rate. A single 125 MHz clock is used to synchronize (G)MII data; and a clock enable is used to regulate the (G)MII data rate.
CTC Mode	This attribute controls the behavior of the CTC block. In dynamic mode, the CTC FIFO thresholds are automatically changed, based upon the current operational rate of the rate adaptation blocks. Optimal thresholds are internally chosen for the three data rates (1Gbps, 100 Mbps, 10 Mbps). In static mode, the user manually chooses the CTC FIFO thresholds, and these thresholds remain fixed. In *none* mode, the CTC function is replaced by a shallow FIFO that facilitates clock domain crossing between the recovered SERDES clock and the local IP core receive-side 125 MHz clock.
Static Low FIFO Threshold	When Static CTC mode is chosen, this attribute specifies FIFO low (almost empty) threshold.
Static High FIFO Threshold	When Static CTC mode is chosen, this attribute specifies FIFO high (almost full) threshold.

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.4. Register Description

This section provides detailed descriptions of SGMII data registers. Note that registers that are not available to users are highlighted in gray.

The register address map, shown in Table 2.4, specifies the available IP Core registers.

Table 2.4. Register Address Map

Offset	Register Name	Description
0x000	Control Register	These are five of the management registers specified in IEEE 802.3, Clause 37 – Control, Status, Auto Negotiation Advertisement, Link Partner Ability, Auto Negotiation Expansion, and Extended Status. The register set is read/written through the LMMI interface.
0x001	Status Register	
0x004	Advertised Ability	
0x005	Link Partner Ability	
0x006	Auto Negotiation Expansion Register	
0x00F	Extended Status Register	
0x00E	Configuration Source Control Register	Switches between SGMII Core management ports and internal configuration registers
0x008	Interrupt Status Register	Status register for IP core events.
0x009	Interrupt Enable Register	Enables the corresponding interrupt status bit.
0x00A	Interrupt Set Register	For debugging/testing purposes. This is used to set the interrupt status register.
0x010 – 0x01C	CDR Control/Status Registers	Registers for configuring the CDR block.
0x100	PCS Control Register 0	PCS Debugging Control Register 0
0x101	PCS Control Register 1	PCS Debugging Control Register 1
0x109	PCS Status Register 9	Rx, Tx and CTC FIFO Status
0x10A	PCS Control Register 10.	PCS Debugging Control Register 10
0x10B	PCS Control Register 11.	PCS Debugging Control Register 11

The behavior of registers to write and read access is defined by its access type, which is defined in Table 2.5.

Table 2.5. Access Type Definition

Access Type	Behavior on Read Access	Behavior on Write Access
RO	Returns register value	Ignores write access
RW	Returns register value	Updates register value
RSVD	Returns 0	Ignores write access

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.4.1. Control Register

Table 2.6. Control Register

Bit Field	Name	Access	Width	Description
15	Reset	RW	1	1=Reset (self-clearing), 0=normal
14	Loopback	RW	1	1=Loopback, 0= normal
13	Speed Selection[0]	RW	1	Combined with bit[6] to form 2-bit vector Speed Selection [1:0] = 11 = reserved Speed Selection [1:0] = 10 = 1Gbps Speed Selection [1:0] = 01 = 100Mbps Speed Selection [1:0] = 00 = 10Mbps In GbE Mode, Speed Selection [1:0] is stuck at *10* = 1Gbps. In SGMII Mode, the Speed Selection [1:0] bits can be written to any value. However, the specified speed only affects the (G)MII data rate when auto-negotiation is disabled. Otherwise, these control bits have no effect. The control of (G)MII data rate when auto-negotiation is enabled is managed by bits [11:10] of the advertised ability vector.
12	Auto Neg Enable	RW	1	1=Enable, 0=Disable
11	Power Down	RW	1	1=Power Down, 0=Power Up
10	Isolate	RW	1	1=Isolate, 0=Normal
9	Restart Auto Neg	RW	1	1=Restart (self-clearing), 0=Normal
8	Duplex Mode	RW	1	1=Full Duplex, 0=Half Duplex Note that the setting of this bit has no effect on the operation of the PCS channel. The PCS channel is always a 4-wire interface with separate TX and RX data paths.
7	Collision Test	RW	1	1=Enable Test, 0=Normal
6	Speed Selection[1]	RW	1	Combined with bit {13] to form the 2-bit vector Speed Selection [1:0]
5	Unidirectional	RW	1	1=Unidirectional, 0=Normal
4:0	—	RSVD	5	—

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.4.2. Status Register

Table 2.7. Status Register

Bit Field	Name	Access	Width	Description
15	100BASE-T4	RO	1	0=not supported
14	100BASE-X Full Duplex	RO	1	0=not supported
13	100BASE-X Half Duplex	RO	1	0=not supported
12	10 Mbps Full Duplex	RO	1	0=not supported
11	10 Mbps Half Duplex	RO	1	0=not supported
10	100BASE-T2 Full Duplex	RO	1	0=not supported
9	100BASE-T2 Half Duplex	RO	1	0=not supported
8	Extended Status	RO	1	1=supported
7	Unidirectional Capability	RO	1	1=supported, 0=not supported
6	MF Preamble Suppress	RO	1	0=not supported
5	Auto Neg Complete	RO	1	1=complete, 0=not complete
4	Remote Fault	RO	1	0=not supported
3	Auto Neg Ability	RO	1	1=supported
2	Link Status	RO	1	1=Link Up, 0=Link Down (Latch-on-zero, Clear-on-read)
1	Jabber Detect	RO	1	0=not supported
0	Extended Capability	RO	1	0=not supported

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.4.3. Advertised Ability Register

Table 2.8. For PCS=GbE

Bit Field	Name	Access	Width	Description
15	Next Page	RW	1	The Base Page and subsequent Next Pages may set the NP bit to a logic one to request Next Page transmission. Subsequent Next Pages may set the NP bit to a logic zero in order to communicate that there is no more Next Page information to be sent (see Clause 37.2.4.3 of IEEE 802.3). A device may implement Next Page ability and choose not to engage in a Next Page exchange by setting the NP bit to a logic zero.
14	Acknowledge	RW	1	The Ack bit is used by the Auto-Negotiation function to indicate that a device has successfully received its link partner's base or Next Page.
13:12	Remote Fault	RW	2	The Remote Fault function may indicate to the link partner that a fault or error condition has occurred. 0 – No error, link OK (default) 1 – Offline 2 – Link Failure 3 – Auto-Negotiation Error
11:9	—	RSVD	3	—
8:7	Pause	RW	2	Pause provides a pause capability exchange mechanism. 0 – No PAUSE 1 - Asymmetric PAUSE toward link partner 2 - Symmetric PAUSE 3 - Both Symmetric PAUSE and Asymmetric PAUSE toward local device
6	Half Duplex	RW	1	Half Duplex Capability.
5	Full Duplex	RW	1	Full Duplex Capability
4:0	—	RSVD	5	—

Table 2.9. For PCS=SGMII-PHY-Side

Bit Field	Name	Access	Width	Description
15	Link Status	RW	1	1=Link Up 0=Link Down
14	Acknowledge	RW	1	The Ack bit is used by the Auto-Negotiation function to indicate that a device has successfully received its link partner's base or Next Page.
13	—	RSVD	1	—
12	Duplex Mode	RW	1	1=Full Duplex 0=Half Duplex
11:10	Speed	RW	2	Speed = 11 = reserved Speed = 10 = 1Gbps Speed = 01 = 100Mbps Speed = 00 = 10Mbps
9:0	—	RO	10	Value=10'h001

Table 2.10. For PCS=SGMII-MAC-Side

Bit Field	Name	Access	Width	Description
15:0	—	RO	16	Value=16'h40001

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.4.4. Link Partner Ability

Table 2.11. For PCS=GbE

Bit Field	Name	Access	Width	Description
15	Next Page	RW	1	The Base Page and subsequent Next Pages may set the NP bit to a logic one to request Next Page transmission. Subsequent Next Pages may set the NP bit to a logic zero in order to communicate that there is no more Next Page information to be sent (see Clause 37.2.4.3 of IEEE 802.3). A device may implement Next Page ability and choose not to engage in a Next Page exchange by setting the NP bit to a logic zero.
14	Acknowledge	RW	1	The Ack bit is used by the Auto-Negotiation function to indicate that a device has successfully received its link partner's base or Next Page.
13:12	Remote Fault	RW	2	The Remote Fault function may indicate to the link partner that a fault or error condition has occurred. 0 – No error, link OK (default) 1 – Offline 2 – Link Failure 3 – Auto-Negotiation Error
11:9	—	RSVD	3	—
8:7	Pause	RW	2	Pause provides a pause capability exchange mechanism. 0 – No PAUSE 1 - Asymmetric PAUSE toward link partner 2 - Symmetric PAUSE 3 - Both Symmetric PAUSE and Asymmetric PAUSE toward local device
6	Half Duplex	RW	1	Half Duplex Capability.
5	Full Duplex	RW	1	Full Duplex Capability
4:0	—	RSVD	5	—

Table 2.12. For PCS=SGMII-PHY-Side

Bit Field	Name	Access	Width	Description
15	Link Status	RW	1	1=Link Up 0=Link Down
14	Acknowledge	RW	1	The Ack bit is used by the Auto-Negotiation function to indicate that a device has successfully received its link partner's base or Next Page.
13	—	RSVD	1	—
12	Duplex Mode	RW	1	1=Full Duplex 0=Half Duplex
11:10	Speed	RW	2	Speed = 11 = reserved Speed = 10 = 1Gbps Speed = 01 = 100Mbps Speed = 00 = 10Mbps
9:0	—	RO	10	Value=10'h001

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.4.5. Auto Negotiation Expansion Register

Table 2.13. Auto Negotiation Expansion Register

Bit Field	Name	Access	Width	Description
15:3	—	RSVD	13	—
2	Next Page Able	RO	1	0=not supported
1	Page Received	RO	1	1=received, 0=not received latch on 1, clear on read
0	—	RSVD	1	—

2.4.6. Extended Status Register

Table 2.14. Extended Status Register

Bit Field	Name	Access	Width	Description
15	1000BASE-X Full Duplex	RO	1	1=supported
14	1000BASE-X Half Duplex	RO	1	0=not supported
13	1000BASE-T Full Duplex	RO	1	0=not supported
12	1000BASE-T Half Duplex	RO	1	0=not supported
11:0	—	RSVD	12	—

2.4.7. Configuration Source Control Register

Table 2.15. Configuration Source Control Register

Bit Field	Name	Access	Width	Description
15:1	—	RSVD	14	—
0	config_source	RW	1	Select the Configuration Source. 0 – From Management Ports 1 – From Programmable Registers

2.4.8. PCS Control Register 0

Table 2.16. PCS Control Register 0

Bit Field	Name	Access	Width	Description
15	enable_cgalign	RW	1	Enable code group alignment. Must be enabled. (Default = 1)
14:13	—	RSVD	2	—
12	ge_an_enable	RW	1	Auto-negotiation enable. 1 – enables the feature, 0 – disables
11:0	—	RSVD	12	—

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.4.9. PCS Control Register 1

Table 2.17. PCS Control Register 1

Bit Field	Name	Access	Width	Description
15	—	RSVD	1	—
14	sb_bypass	RW	1	Always keep active (1). Deactivation breaks the link. For debugging. (Default = 1)
13	—	RSVD	1	—
11	enc_bypass	RW	1	Keep inactive (0). Activation will exclude the encoder from Tx path. (Default = 0)
10	—	RSVD	1	—
9	tx_gear_bypass	RW	1	Keep active (1). Deactivation breaks the link. For debugging. (Default = 1)
8	fb_loopback	RW	1	Activates Rx-Tx loopback. Loopback activation must be done at least 500 ns before tx_en activation and removed later than at least 500 ns after tx_en drop (or core tx-rx latency delay). This makes the transition from loopback to normal mode seamless. (Default = 0)
7	lsm_disable	RW	1	Selects alignment mode along with configuration PCS Control Register 10 bits [15:8]. Alignment must be always enabled (0x10A = 0x8000). (Default = 0)
6	signal_detect	RW	1	Signal detect imitation. (Default = 0)
5	rx_gear_bypass	RW	1	Keep active (1). Deactivation breaks the link. (Default = 1)
4	ctc_bypass	RW	1	Keep active (1), otherwise adds additional CTC into Rx path, which is necessary when SGMII is in the Gigabit Ethernet Mode. (Default = 1)
3	dec_bypass	RW	1	Keep inactive (0), otherwise breaks the link. For debugging. (Default = 0)
2	wa_bypass	RW	1	Keep inactive (0), otherwise breaks the link. For debugging. (Default = 0)
1:0	—	RSVD	2	—

2.4.10. PCS Control Register 9

Table 2.18. PCS Control Register 9

Bit Field	Name	Access	Width	Description
15	—	RSVD	1	—
14	cc_underrun	RO	1	CTC FIFO underrun (if enabled). Valid for GBE Mode only.
13	cc_overrun	RO	1	CTC FIFO overrun (if enabled). Valid for GBE Mode only.
12	rx_fifo_error	RO	1	Rx FIFO error.
11	tx_fifo_error	RO	1	Tx FIFO error.
10:7	align_status	RO	4	Word align status – number of bits that the input has been shifted.
6	ls_sync_status	RO	1	Synchronization status.
5	rstb_rxf	RO	1	Receiver reset pulse.
4	rstb_txf	RO	1	Transmitter reset pulse.
3	~cc_re	RO	1	Inversion of character inserted flag. Valid for GBE Mode only.
2	~cc_we	RO	1	Inversion of character deleted flag. Valid for GBE Mode only.
1	cc_re	RO	1	Character inserted flag. Valid for GBE Mode only.
0	cc_we	RO	1	Character deleted flag. Valid for GBE Mode only.

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.4.11. PCS Control Register 10

Table 2.19. PCS Control Register 10

Bit Field	Name	Access	Width	Description
15	lsm_eca	RW	1	Link status management. Enables code group alignment regardless of *lsm_disable* and *fc_mode*. (Default = 1)
14:13	—	RSVD	2	—
12	wa_mode	RW	1	Word alignment mode. 1- single slip. (Default = 0)
11:10	—	RSVD	2	—
9	fc_mode	RW	1	Fiber channel mode, data interpretation. (Default = 0)
8	uc_mode	RW	1	Data interpretation mode. (Default = 0)
7:0	—	RSVD	8	—

2.4.12. PCS Control Register 11

Table 2.20. PCS Control Register 11

Bit Field	Name	Access	Width	Description
15:8	—	RSVD	8	—
7	rst_pcs	RW	1	reset pcs module (Rx+Tx). (Default = 0)
6	rst_pcs_rx	RW	1	reset pcs Rx sub-module. (Default = 0)
5	rst_pcs_tx	RW	1	reset pcs Tx sub-module. (Default = 0)
4:0	—	RSVD	5	—

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

3. IP Generation and Evaluation

This section provides information on how to generate the SGMII IP Core using the Lattice Radiant Software and how to run synthesis and simulation. For more details on the Lattice Radiant Software, refer to the please refer to the Lattice Radiant Software 2.1 User Guide.

3.1. Licensing the IP

An IP core-specific license string is required to enable full use of the SGMII IP Core in a complete, top-level design.

The IP Core can be fully evaluated through functional simulation and implementation (synthesis, map, place and route) without an IP license string. This IP core supports Lattice's IP hardware evaluation capability, which makes it possible to create versions of the IP core, which operate in hardware for a limited time (approximately four hours) without requiring an IP license string. See Hardware Evaluation section for further details. However, a license string is required to enable timing simulation and to generate bitstream file that does not include the hardware evaluation timeout limitation.

3.2. Generation and Synthesis

The Lattice Radiant Software allows you to customize and generate modules and IPs and integrate them into the device's architecture. The procedure for generating the SGMII IP Core in Lattice Radiant Software is described below.

To generate the SGMII IP Core:

1. Create a new Lattice Radiant Software project or open an existing project.
2. In the **IP Catalog** tab, double-click on **SGMII and Gb Ethernet PCS** under **IP, Connectivity** category. The **Module/IP Block Wizard** opens as shown in Figure 3.1. Enter values in the **Instance name** and the **Create in** fields and click **Next**.

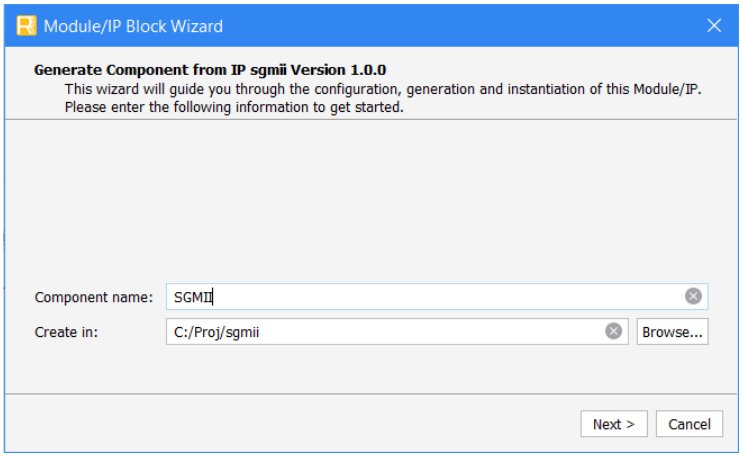

Figure 3.1. Module/IP Block Wizard

3. In the module's dialog box of the **Module/IP Block Wizard** window, customize the selected SGMII IP Core. As a sample configuration, see Figure 3-2. For configuration options, see the Attribute Summary section.

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

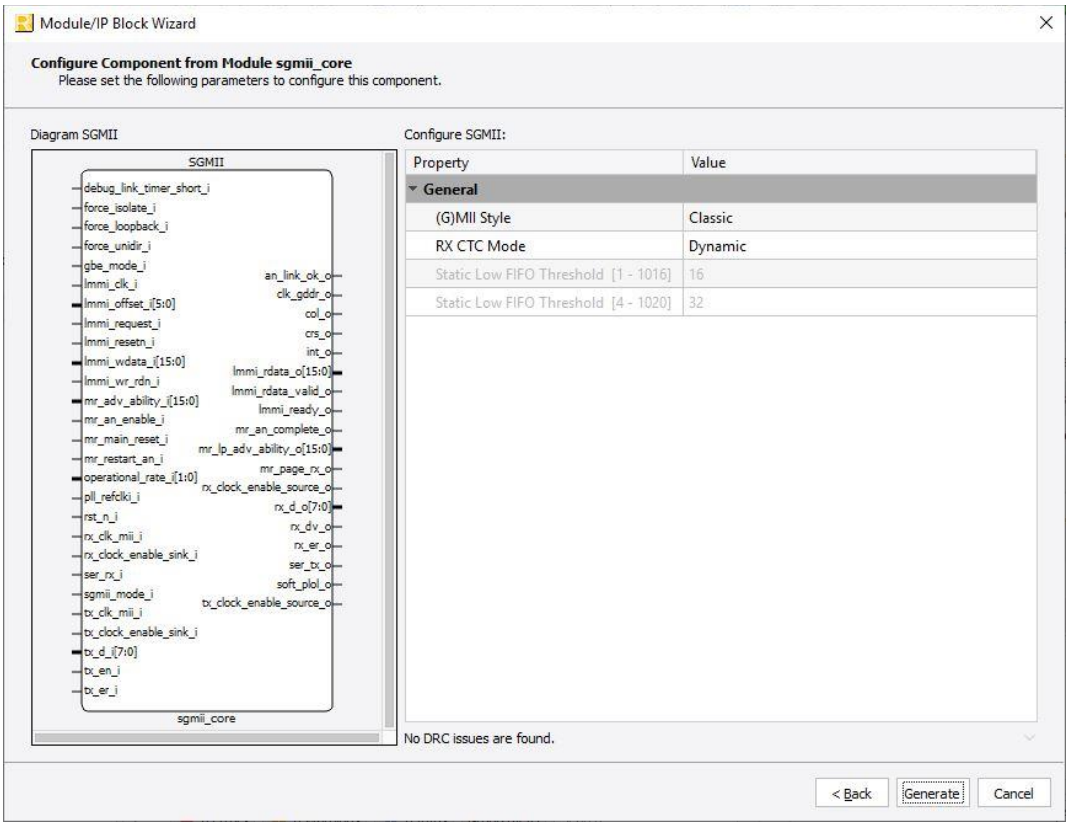

Figure 3.2. Configure User Interface of SGMII IP Core

4. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results as shown in Figure 3-3.

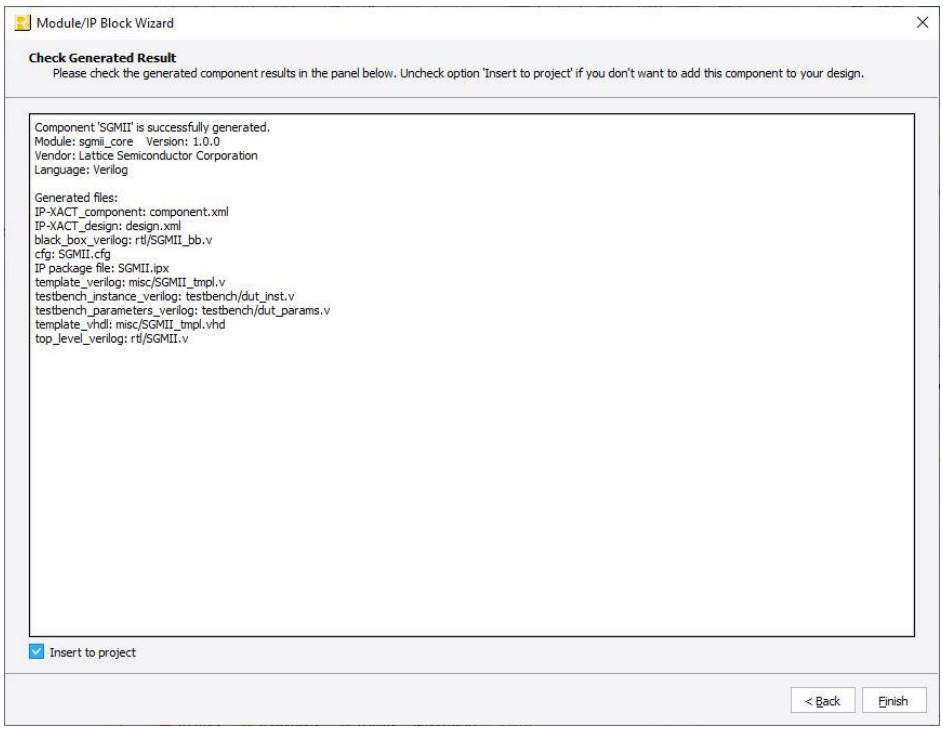

Figure 3.3. Check Generating Result

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

5. Click the **Finish** button. All the generated files are placed under the directory paths in the **Create in** and the **Instance name** fields shown in Figure 3-1.

The generated SGMII IP Core package includes the black box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the IP core is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated File List

Attribute	Description
<Instance Name>.ipx	This file contains the information on the files associated to the generated IP.
<Instance Name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an example RTL top file that instantiates the IP core.
rtl/<Instance Name>_bb.v	This file provides the synthesis black box.
misc/<Instance Name>_tmpl.v misc /<Instance Name>_tmpl.vhd	These files provide instance templates for the IP core.

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

3.3. Running Functional Simulation

Running functional simulation can be performed after the IP is generated.

To run Verilog simulation:

1. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in Figure 3.4.

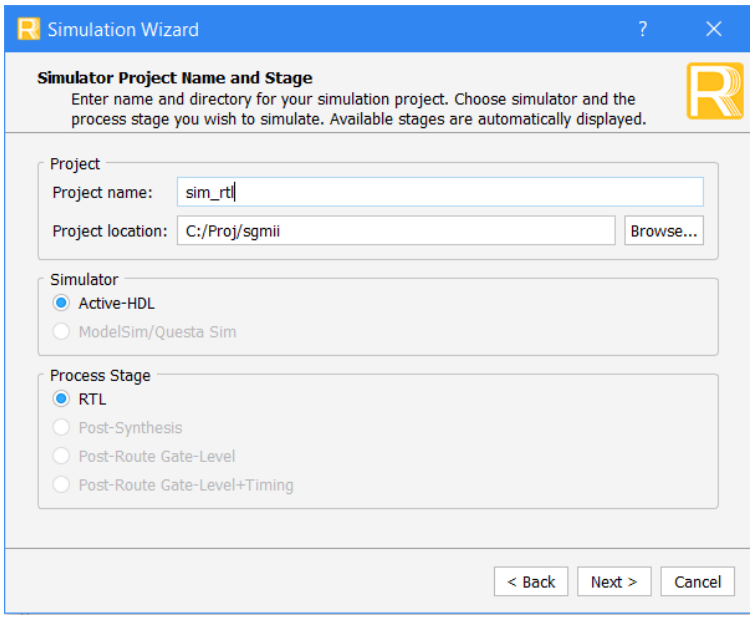

Figure 3.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window as shown in Figure 3.5.

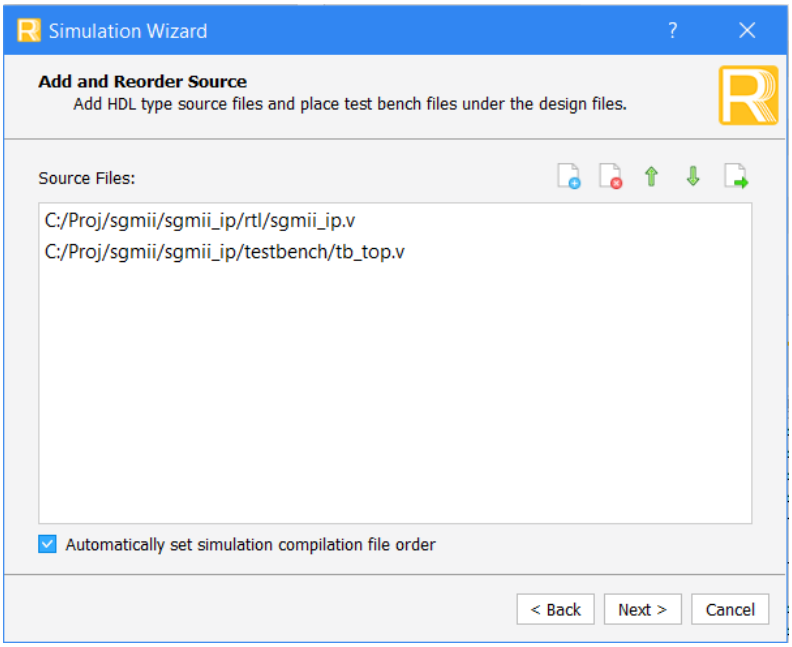

Figure 3.5. Adding and Reordering Source

3. Click **Next**. The **Summary** window is shown. Click **Finish** to run the simulation.

Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant Software Suite.

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

3.4. Hardware Evaluation

The SGMII IP Core supports Lattice's IP hardware evaluation capability when used with LIFCL devices. This makes it possible to create versions of the IP core that operate in hardware for a limited period of time (approximately four hours) without requiring the purchase of an IP license. It may also be used to evaluate the core in hardware in user-defined designs. The hardware evaluation capability may be enabled/disabled in the Strategy dialog box. It is enabled by default. To change this setting, go to Project > Active Strategy > LSE/Synplify Pro Settings.

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

4. Ordering Part Number

The Ordering Part Number (OPN) for this IP Core are the following:

- GBE-SGMII-CNX-U – SGMII and Gb Ethernet PCS for CrossLink-NX - Single Design License
- GBE-SGMII-CNX-UT – SGMII and Gb Ethernet PCS for CrossLink-NX - Site License
- GBE-SGMII-CTNX-U – SGMII and Gb Ethernet PCS for Certus-NX - Single Design License
- GBE-SGMII-CTNX-UT – SGMII and Gb Ethernet PCS for Certus-NX - Site License

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Appendix A. Resource Utilization

Table A.1 shows the resource utilization for the LIFCL-40-9BG400I using Lattice Radiant Software.

For more information on Lattice Radiant Software, visit the Lattice web site at www.latticesemi.com/Products/DesignSoftwareAndIP.

Table A.1. Resource Utilization

Configuration	Slice Registers	LUTs	EBRs
Default	2248	2812	3

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Radiant Software 2.1 User Guide.

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Revision History

Revision 1.2, June 2020

Section	Change Summary
Introduction	• Updated Table 1.1 to add Certus-NX and LFD2NX-40 as targeted device. • Updated Lattice Implementation to Lattice Radiant 2.1.
Ordering Part Number	Updated devices and part numbers.
Appendix A. Resource Utilization	Updated device to LIFCL-40-9BG400I and adjusted contents of Table A.1.
All	Updated references to Lattice Radiant Software 2.1 User Guide.

Revision 1.1, February 2020

Section	Change Summary
Introduction	Updated Table 1.1 to add LIFCL-17 as targeted device.

Revision 1.0, December 2019

Section	Change Summary
All	Initial release.

© 2019-2020 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

www.latticesemi.com

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Development Software ***category:***

Click to view products by Lattice ***manufacturer:***

Other Similar products are found below :

RAPPID-567XFSW SRP004001-01 SW163052 SYSWINEV21 WS01NCTF1E W128E13 SW89CN0-ZCC IPS-EMBEDDED IP-UART-16550 MPROG-PRO535E AFLCF-08-LX-CE060-R21 WS02-CFSC1-EV3-UP SYSMAC-STUDIO-EIPCPLR LIB-PL-PC-N-1YR-DISKID 1120270005 1120270006 MIKROBASIC PRO FOR FT90X (USB DONGLE) MIKROC PRO FOR FT90X (USB DONGLE) MIKROBASIC PRO FOR AVR (USB DONGLE LICEN MIKROBASIC PRO FOR FT90X MIKROC PRO FOR DSPIC30/33 (USB DONGLE LI MIKROPASCAL PRO FOR ARM (USB DONGLE LICE MIKROPASCAL PRO FOR FT90X MIKROPASCAL PRO FOR FT90X (USB DONGLE) MIKROPASCAL PRO FOR PIC32 (USB DONGLE LI SW006021-2H ATATMELSTUDIO 2400573 2702579 2988609 2702546 SW006022-DGL 2400303 2701356 VDSP-21XX-PCFLOAT VDSP-BLKFN-PC-FULL 88970111 DG-ACC-NET-CD 55195101-101 55195101-102 SW1A-W1C MDK-ARM SW006021-2NH SW006021-1H SW006021-2 SW006022-2 SW006023-2 SW007023 MIKROE-730 MIKROE-2401